

REDUNDANT ALSEP UPLINK SYSTEM

FINAL REPORT

The following ATM has been prepared in response to
Contract NAS 9-5829.

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1.0 INTRODUCTION

The present ALSEP uplink is single thread and therefore a single point failure can result in a complete loss of the uplink. Hence this study was initiated under Contract No. NAS 9-5829 to determine the optimum means for providing a redundant ALSEP uplink system. The study has resulted in a recommended approach plus the details of changes necessary to implement it. In addition, the results of tests performed on the ALSEP MSFN model to determine the source of anomalous uplink behavior are included. The results of these tests have led to recommended changes in the command decoder and demodulator. These changes are included with those required to achieve redundancy.

2.0 REDUNDANT UPLINK

A fully redundant uplink is shown in Figure 2-0. Two complete command signal channels are shown with dashed lines included to show points for possible cross-strapping.

Since the two signal paths are identical a command signal will be processed by both of the redundant channels and will be OR'ed at the output of the command decoding gates. Redundant channels cannot be carried beyond this point due to limitations of the command user. From a purely theoretical point, this design should have the highest achievable reliability however, the human factors related to mounting and aligning two antennas may degrade this figure. A disadvantage of this system is the requirement for mounting and accepting the weight of the two antennas, filters and interconnecting cables.

2.1 Minimum Redundant Uplink

The minimum redundancy considered for the uplink is shown in Figure 2-1. This design is identical to the present ALSEP uplink except for the inclusion of two receivers and demodulators. The single thread signal path then consists of the antenna, cables and filter. In addition, specific failures in the command decoder can affect more than one command. If an output gate driver fails low, approximately 6% of the command capability is lost. If it fails high, the affected commands will be falsely executed upon receipt of a valid command that differs only in the bit position controlled by the failed driver.

If a command enable gate fails low the effect is the same as the output gate driver failing high except that each of these gates controls approximately 25 commands.

The demodulator has received considerable attention on ALSEP and it is considered to be the prime suspect for the failure of the EASEP uplink. The addition of a redundant demodulator is therefore considered mandatory. The antenna, cables and filter are passive elements and, following deployment, are not subject to degradation; therefore use of non-redundant elements does not have a significant effect on reliability.

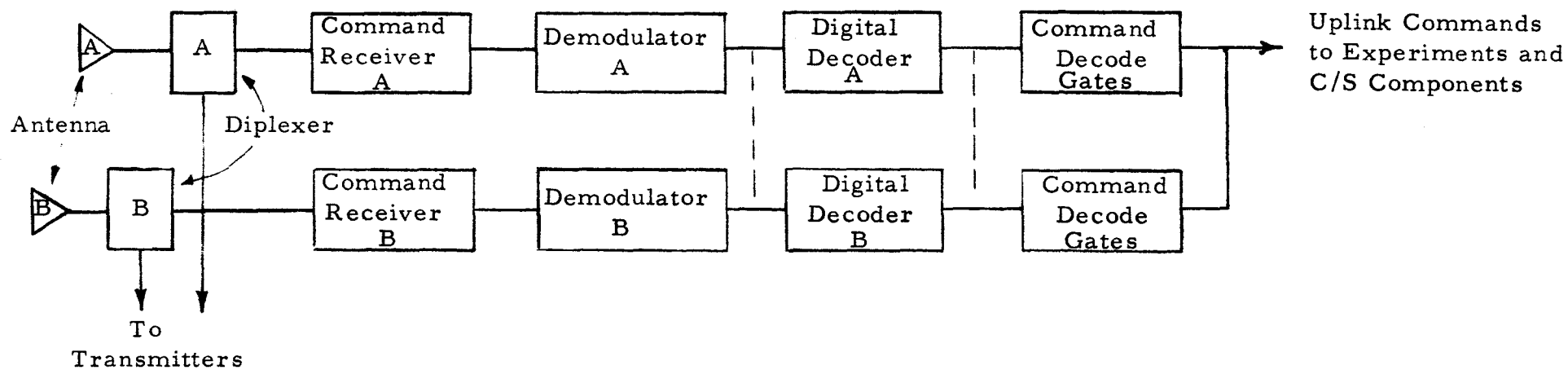


FIGURE 2-0 FULLY REDUNDANT UPLINK

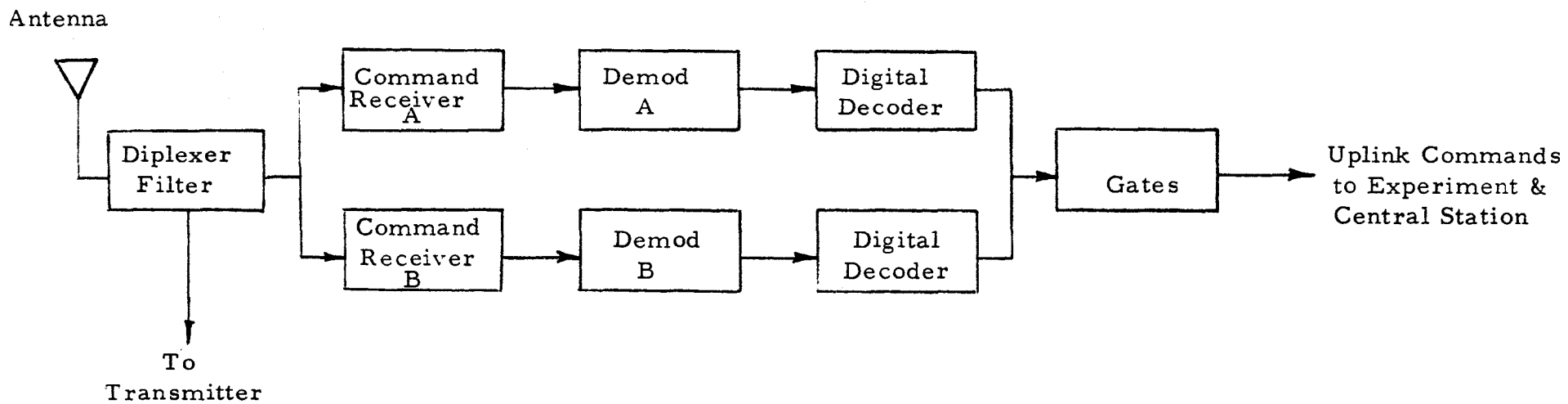


FIGURE 2-1 MINIMUM UPLINK REDUNDANCY



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2.2 Recommended Uplink Design

The recommended design for the uplink is shown in Figure 2-2. This design does not have all of the features of the fully redundant uplink as shown in Figure 2-0, but does provide full redundancy for all the active components associated with the uplink. Both of the redundant signal paths are powered and operating continuously.

The antenna, diplexer filter and cables are identical to those proven designs used at present, thus no new design or qualification costs are incurred. They are passive and not subject to the degradation of active components. Because of their passive operation, use of single thread signal path at this point in the uplink will have an insignificant affect on long term reliability.

The power splitter is actually a part of the command receiver: it is printed wiring on a circuit board and is therefore passive. The redundant command receiver to be used on Array D is presently in development. The "A or B output" which is an optional feature of the receiver, is not used but rather, each output is continuously fed to a demodulator.

The demodulators are fully redundant and drive the redundant digital decoders with NRZ-C signals when the uplink is on and modulated. Both the demodulator and digital decoders are improved designs which reject noise during periods of no uplink carrier, have improved security against false commands and do not issue false command verification words.

This recommended design also contains redundant sets of decoding gates for additional improvement in reliability. Potential points of cross-strapping are shown with dashed lines. Use of cross-strapping can result in reliability enhancement however care must be exercised so that the design is implemented with no single point failures. Cross-strapping has not been recommended because of the difficulty in the implementation of automatic devices in the event of loss of command capability. The output of the command decoding gates are wired OR'ed for application of the command signals to the user.

3.0 DIPLEXER FILTER

The diplexer filter interconnects the antenna, the receivers, and the transmitters. Its function is to route the received uplink RF energy from the antenna to the receiver, and also to route the transmitter downlink RF energy to the antenna. To accomplish these functions, the diplexer filter contains a transmit frequency bandpass filter, a receiver frequency band pass filter, and a command path lowpass filter. No changes are recommended for this component.

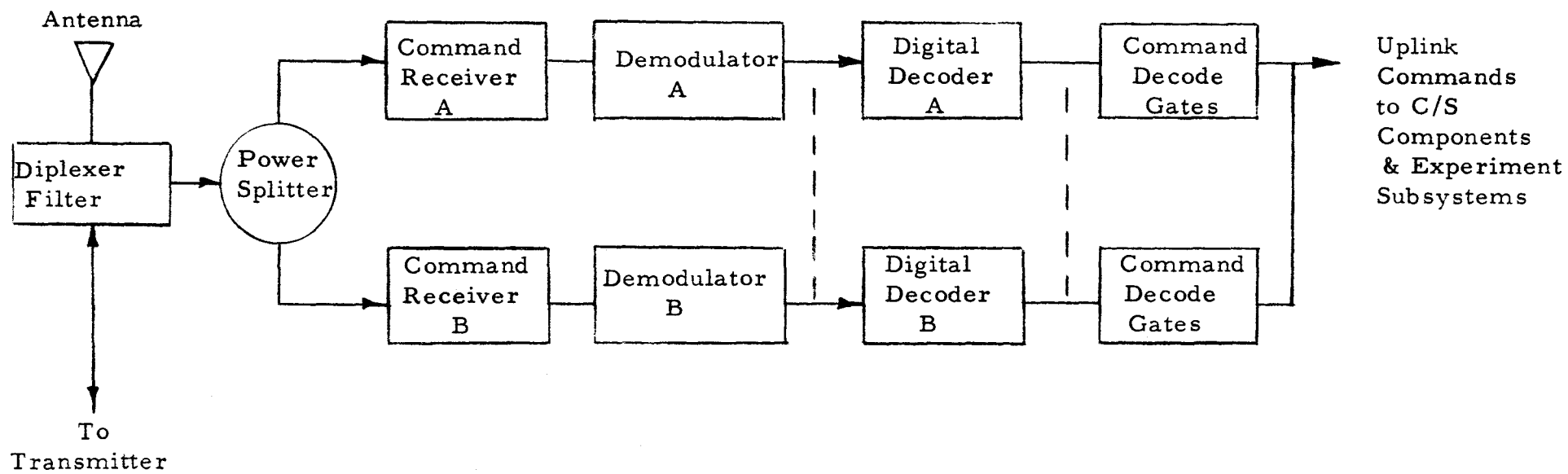


FIGURE 2-2 RECOMMENDED UPLINK DESIGN

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4.0 COMMAND RECEIVER

The command receiver unit includes an RF hybrid coupler which accepts RF energy from the output of the diplexer filter and divides it equally between the inputs to the two redundant receivers.

Each receiver is capable of detecting the signal which is phase modulating the uplink carrier. Additionally, they are capable by preflight selection of detecting the signal which is frequency modulating a 70 kHz subcarrier. This receiver is being developed for use on ALSEP Array D (Apollo 16) and represents a substantial improvement in reliability.

5.0 COMMAND DECODER

The Command Decoder, (1) accepts subcarrier modulated command information from the command receiver, (2) extracts and converts data and sync information into digital form, (3) recognizes and responds to its unique address, (4) provides basic timing, and (5) decodes command information and supplies commands to applicable users to control prescribed operations. In addition, the command decoder interfaces with the central station timer and provides for delayed command sequencing functions.

Functions (1) and (2) are performed in each demodulator, (3) and (4) are performed in redundant digital decoder sections and (5) provides a 100 discrete command decoding capability.

5.1 Demodulator Design Considerations

The present demodulator threshold circuit responds to a noisy receiver output when the uplink is off. The normal 1 kHz and 2 Kz composite signal from the receiver output is 4 to 6 volts peak to peak, whereas the noise output with uplink off is limiting to about 18 volts peak to peak. There is a tendency for increased threshold circuit on time in the presence of receiver noise for the following reasons.

- (1) There appears to be large noise components within the capture range of the Phase Lock Loop (approximately 700 Hz to 1300 Hz). The threshold circuit and P. L. L. are both looking for a signal within this frequency range and the P. L. L. is capable of locking within 20 ms max. (Initial design criteria.) Therefore, the P. L. L. can in effect phase track the noise signal, hence increasing the probability of switching the threshold circuit on noise.



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- (2) The threshold circuit is set to switch on about three cycles of phase coherent 1 kHz sync after phase-lock-loop lock on. This activation time is reduced with a larger amplitude signal again increasing the probability of switching the threshold circuit with large amplitude noise.
- (3) The existing threshold circuit consists of a 1 kHz chopper, analog integrator and a Schmitt trigger. The integrator output voltage builds up and passes through threshold with several in phase periods of 1 kHz sync and hence one or two out-of-phase periods of 1 kHz signal can pass through without dropping out the threshold detector. This threshold drop out condition worsens with larger in-phase signals and smaller out-of-phase signals.

It is recommended that the demodulator be redesigned with characteristics shown in Table 5-1. Note that the following advantages will be realized assuming that the VCO/PLL lock on-time is increased.

1. Decrease the bandwidth of the P. L. L. which would reduce the effect described in (1) above. This would increase the lock-on time but would reduce data modulation of the clock and hence reduce the phase jitter of the data detection circuits.
2. Threshold detect on the data (2 kHz) and not on the 1 kHz. This again would reduce the effect described in (1) above, since the 2 kHz noise is probably not phase coherent with the 1 kHz. In addition measurements show that the noise power at 2 kHz is approximately 6 db below the value at 1 kHz.
3. Use an eight bit shift register as an eight bit sliding window detector. Each data bit will be sampled and transferred into the shift register. Eight consecutive correct 2 kHz data bit decisions would allow the threshold to switch and pass data. One bit error would instantly shut off the threshold detector and require eight more correct samples. This would correct the problems described in (2) and (3) above as follows:
 - a) Each sample is independent of the previous sample.
 - b) Each sample is independent of amplitude.
 - c) It takes only one incorrect sample to turn off the threshold. (8-1 hysteresis)

TABLE 5-1 DEMODULATOR CHARACTERISTICS

	PRESENT	REDESIGN
Input Signal		
Phasing	Composite 1 kHz and 2 kHz	Same
Strength	5 VPP \pm 10%	Same
VCO/PLL		
Lock-on-time	Within 20 msec	Within 1 sec
Lock-on-frequency	1 kHz	Same
Bandwidth	558 Hz (type)	Significantly Less Than 500 Hz
Data Phase Detector and Int and Dump	Same	Same
Threshold Detector		
Lock-on-frequency	1 kHz	2 kHz
Lock-on-time	Within 3 msec after VCO/PLL lock-on	Within 8 msec after presence of phase coherent 2 kHz
Type	Analog integrator with level detection	Eight bit digital sliding window detec- tor with hysteresis turn on -8 correct samples; turn off -1 incorrect sample
Input Voltages	+12, +5, -6V	\pm 12, +5 V
Part Count Per Demodulator	142 (Actual)	26 (Typical)
Number of Demodulators per System	1	2

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A block diagram of the proposed demodulator is shown in Figure 5-1. A redesign of the demodulator would allow the use of more integrated circuits in place of existing discrete components and hence redundant demodulators could be packaged in the same volume as the present demodulator. Reliability can be increased with a reduction of components and redundancy. An estimate of the reduction in parts is shown in Table 5-2.

The increase in the PLL lock on time, i. e., narrower loop bandwidth, will require an increase in the preamble length over the present 20 msec. However, for normal uplink operation the uplink carrier is on, with a pattern of all ones, minutes prior to the transmission of an actual command. Thus in normal operation the command preamble is actually many times greater than 20 msec and therefore the advantages cited can be achieved with a minimum impact on uplink operation.

5.2 Digital Sections Design Considerations

The digital sections of the Command Decoder will be implemented with complete redundancy to improve reliability. The present uplink command format consists of 7 address bits, 7 command complement bits, 7 command bits, and a 20 bit pre and postamble. If this format is retained, it is necessary to use an address memory flip flop to inhibit the decoder not being addressed (see Figure 5-2), in order to prevent this decoder from detecting an address and possible command in the command or command complement of the addressed decoder. This requirement is documented in "Investigation of ALSEP Address Codes", ATM 843 .

The command decoders will continually interrogate the uplink data as received from the demodulators for their individually assigned addresses. Upon receipt of its address the responding command decoder section will immediately inhibit the opposite decoder section and perform the timing and control required to properly execute a discrete command. The timing and control functions are as follows:

1. Permit the command complement to enter the data shift register.
2. Test the command complement bits against the command bits for proper bit configuration.
- 3a. If bit configuration checks, allow command to be executed for 20 milliseconds and insert a logic "1" into the first bit position of the shift register.

FIGURE 5-1 DEMODULATOR BLOCK DIAGRAM

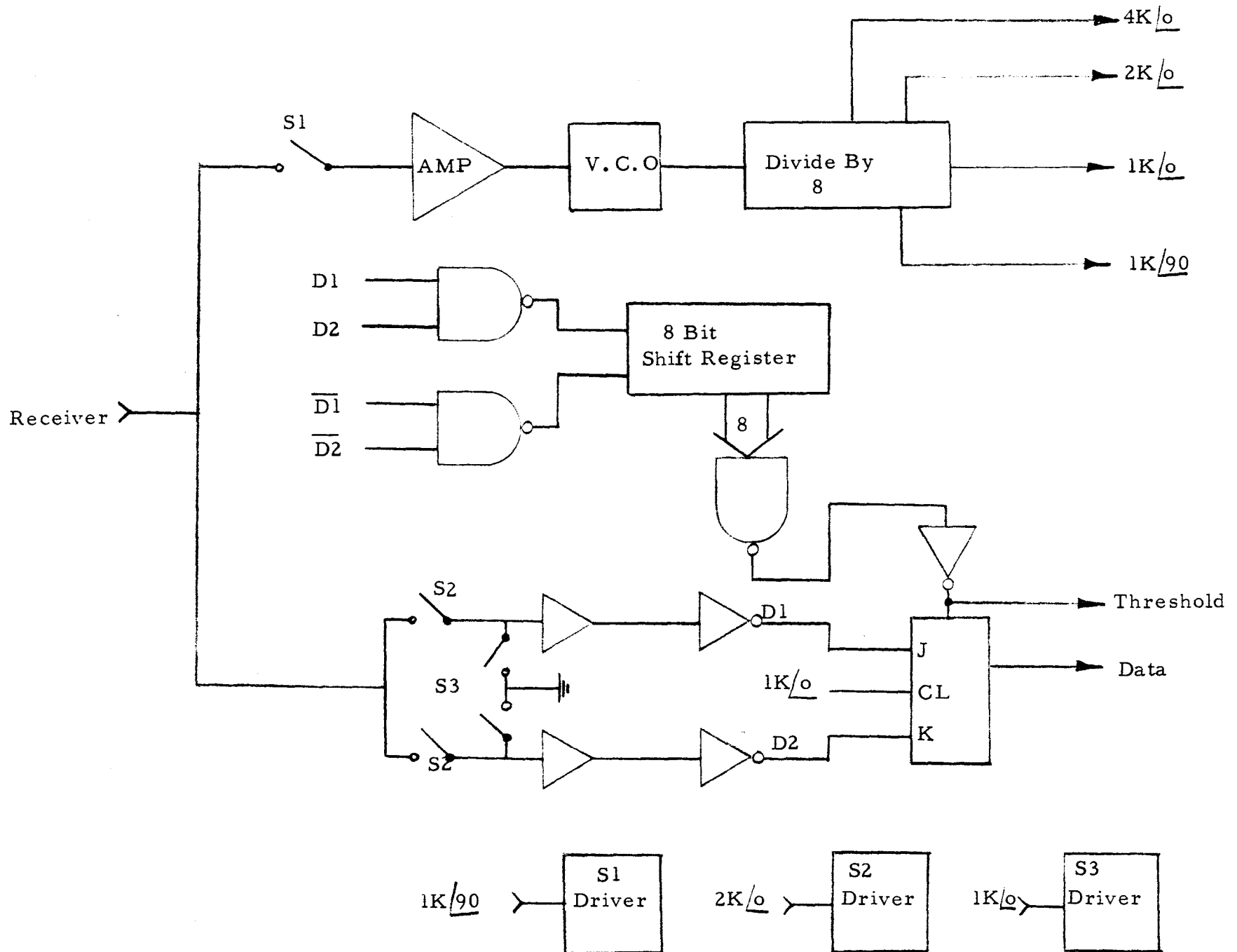


TABLE 5-2 ESTIMATED DEMODULATOR PARTS REDUCTION

	PRESENT DEMOD	REDESIGNED DEMOD
Resistors	76	12
Cap	22	6
Diodes	11	--
Transistors	24	--
Flat Packs	5	8
TO 5 Cans	4	1
	<hr/>	<hr/>
TOTAL	142	26

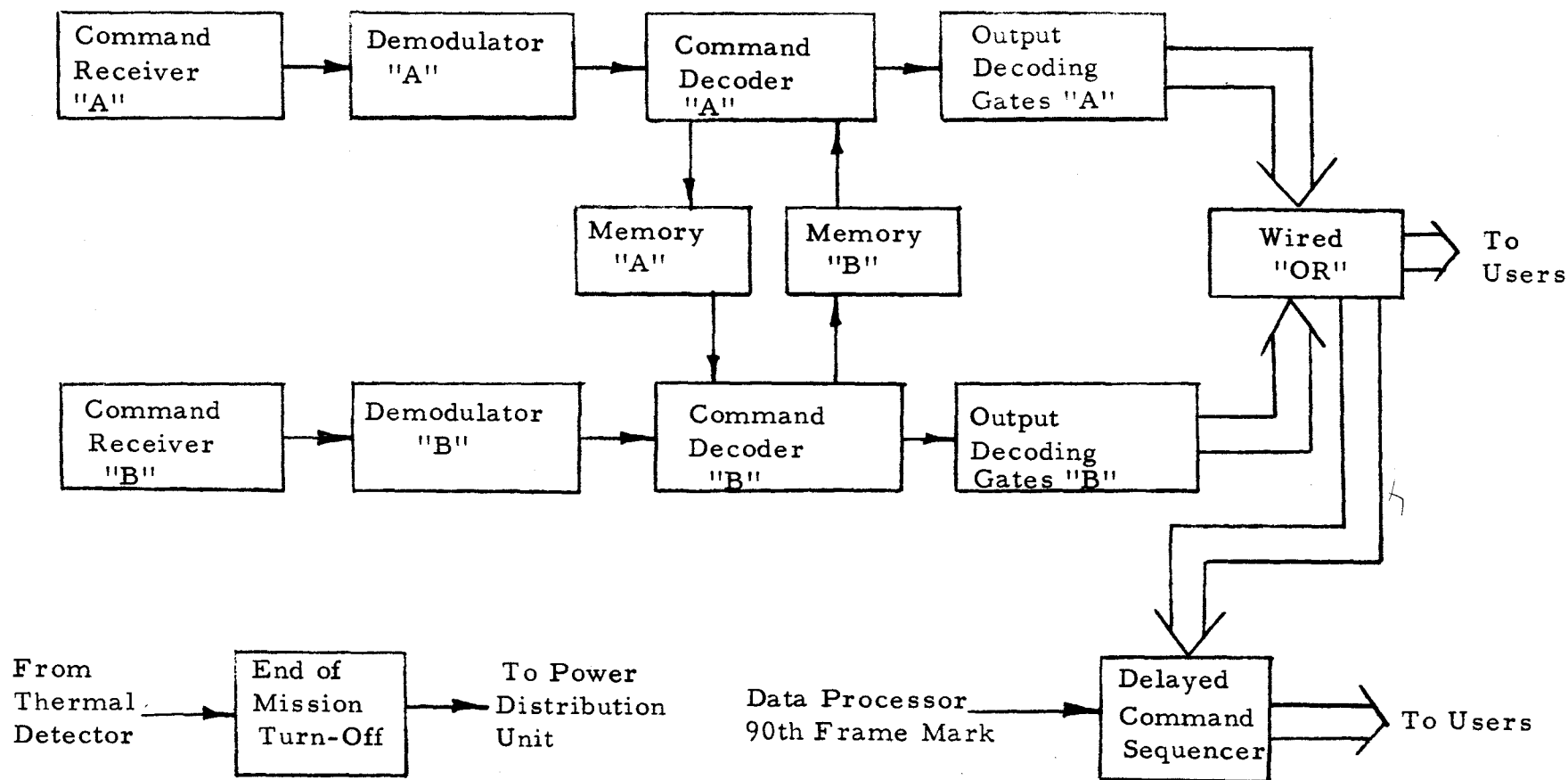


FIGURE 5-2 BLOCK DIAGRAM COMMAND DECODER



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- 3b. If bit configuration does not check, inhibit execution of the command and insert a logical "0" into the first bit position of the shift register.
4. Allow data demand from data processor to shift out command verification word for downlink transmission.
5. Reset, remove inhibit, and return both decoders to search mode operation.

The output gates will decode discrete commands. Only that decoder which has been addressed will perform the decoding function and the command executed will be routed from its decoding gate via a wired "or" to the appropriate user. Utilization of these pre-decoding techniques will permit simplified output decoding with 100% redundancy.

The address detection and inhibit memory flip flops will be a redundant system. Utilization of dual address gates, dual flip flops, dual lines and decision gating logic will eliminate a single point failure which exist in the present design (see Figure 5-3). The application of this technique will remove the possibility of a single failure, locking out a decoder and rendering the system inoperable.

Resetting of the command decoder will result from any one of the following conditions. A power on reset will be generated when initial power is applied or if a power dropout should occur. A reset pulse will occur upon completion of the transfer of command verification word to the data processor. In the event of a loss of data demand, reset will be accomplished after approximately two seconds by decoding the output of the programmer counter. Additionally, a reset will result if a loss of threshold should occur any time prior to execution of a command. Figure 5-4 shows the proposed reset control circuitry.

5.3 Implementation:

Table 5-3 shows the components by function required to implement redundant digital sections of the command decoder. The table is for one command decoder therefore all figures must be multiplied by two to arrive at a total configuration. Total flat-pack requirements would be approximately 240 as compared to the 350 presently required. A total power consumption of approximately 1.2 watts would be required for the new redundant system (digital only). The flat packs can be easily packaged on five 12-layer printed circuit cards.

Inhibit
A1

From
Shift
Register
"A"

Inhibit
A2

Inhibit
B1

From
Shift
Register
"B"

Inhibit
B2

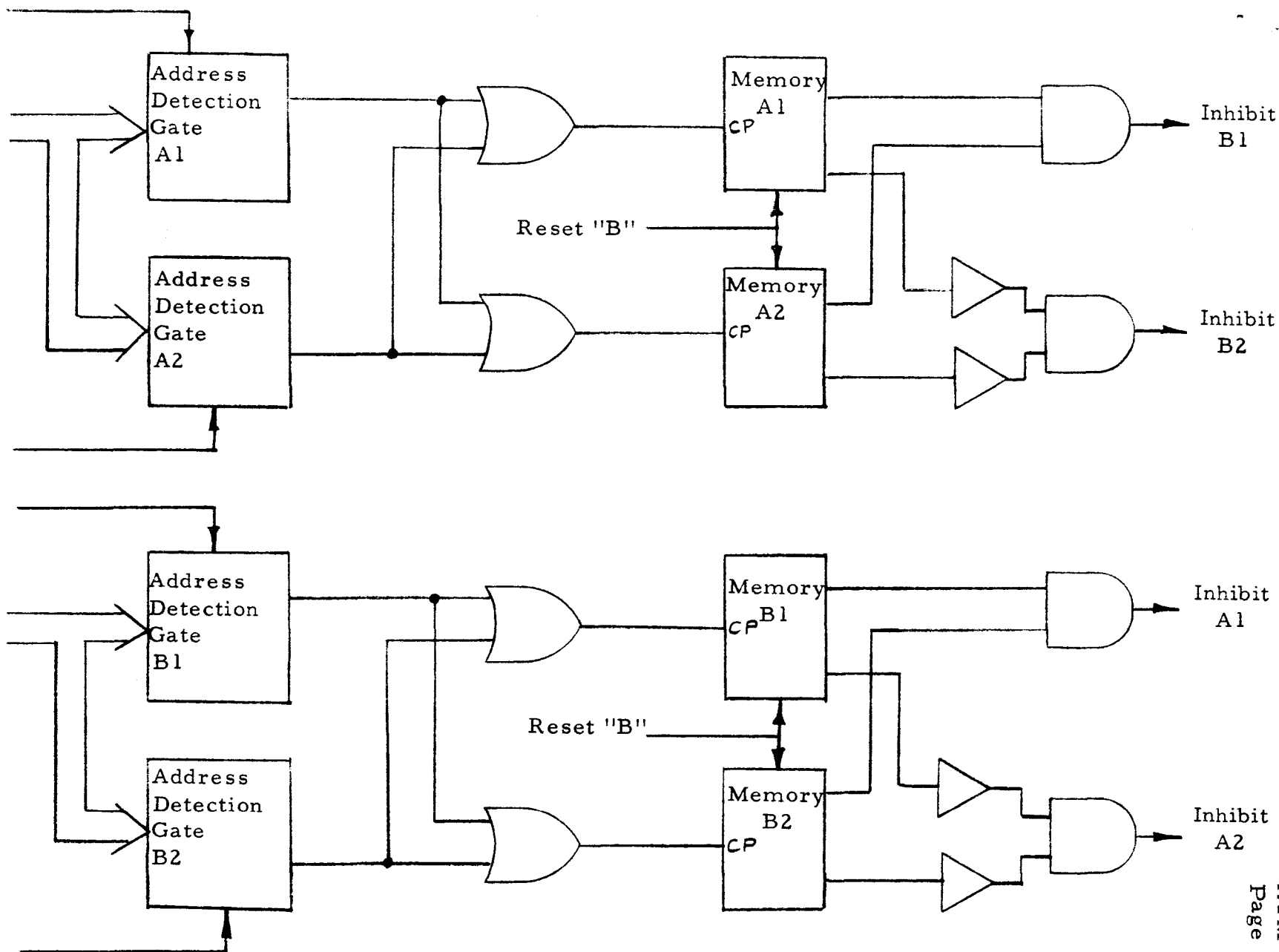


FIGURE 5-3 ADDRESS DETECTION & INHIBIT

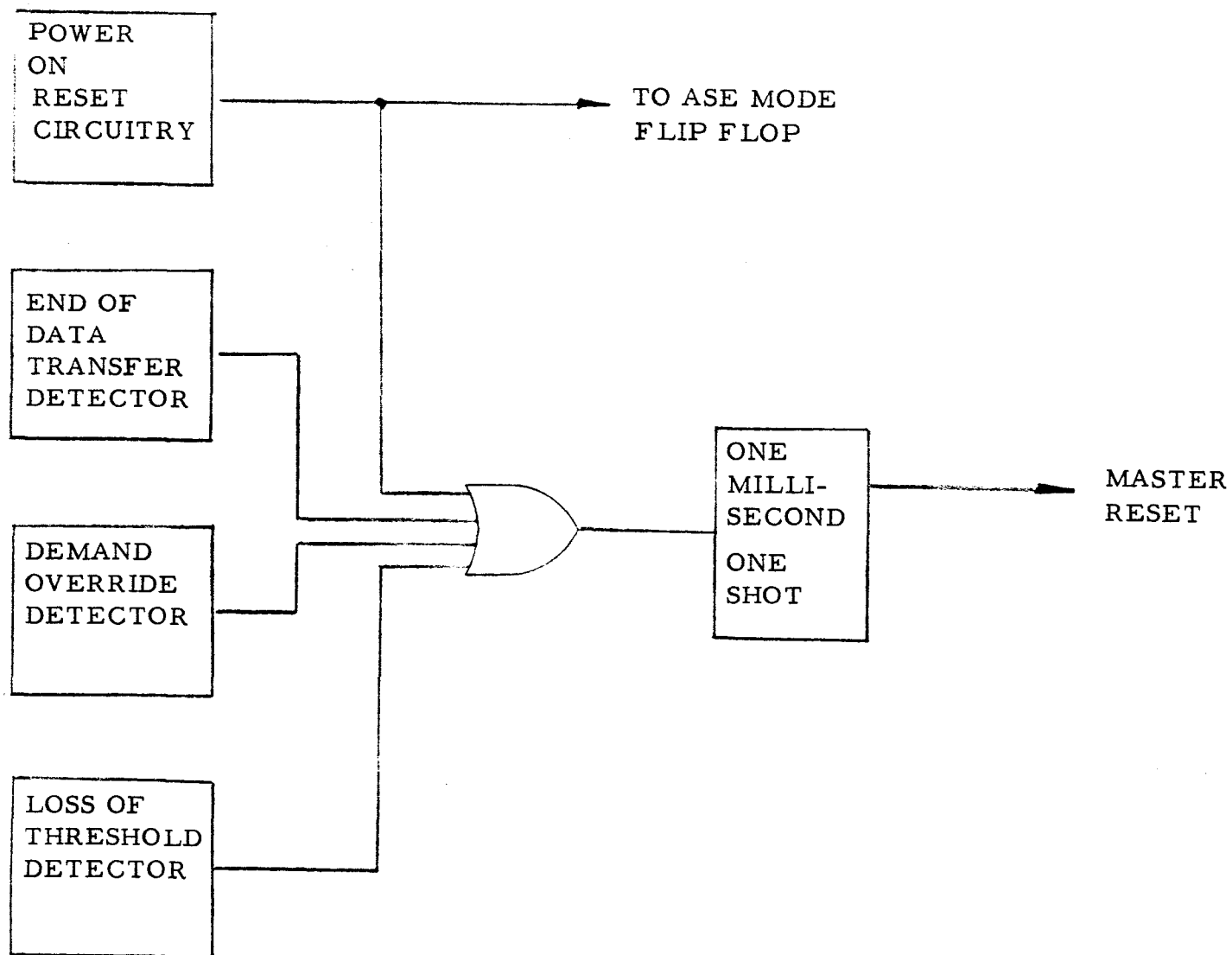


FIGURE 5-4 RESET CIRCUITRY

TABLE 5-3 SINGLE COMMAND DECODER COMPONENT SUMMARY

Function	Quad 2 input gate TI SN 54L005	Hex Inverter gate TI SN 54L04T	Triple 3 input gate TI SN 54L10T	Dual 4 input gate TI SN 54L20T	8 input gate TI SN 54L30T	JK F.F. TI SN 54L72T	Dual JK F.F. TI SN 54L73T	4 bit binary counter TI SN 54L93T	Monostable multivibrator TI SN 54L121T	Triple 3 input gate Fairchild 9047	Misc. Comp.
Shift Register & Parity	4-1/4	1/2					4				
Sub Decoding	1/2			8							
Output Decoding		16								33-1/3	
Timing & Control	4	3	2		3			3			
Delayed Command Sequencer	3	3		7	7			3			
Address Det & Memory	1	1/3			2		1				
End of Mission Counter		1/3	1			1	1				
Reset Circuitry		1/3		1	1				1		2 Res. 2 Cap.
TOTALS	12-3/4	23	3	16	13	1	6	6	1	33-1/3	
Power (mw)	51	138	9	64	13	4	24	96	100	100	N/A



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5.4 Summary:

The use of Texas Instrument 54L T²L low power logic will enable the construction of a completely redundant Command Decoder in the present package size. The output gates will be low power Fairchild 9040 Series DTL. The use of these gates permit the more reliable wire "oring" of the discrete command outputs. A reduction in weight and volume can be achieved along with the increased decoder reliability. The design eliminates a potential single point failure mode in the address inhibit circuit.

6.0 UPLINK SECURITY OPTIONS

The modifications recommended for the Command Decoder are predicated on increased uplink security with a minimum impact to ALSEP and the ground station. Consideration has also been given to the addition of a 4 bit pattern preamble to remove cross strapping between decoders A and B, the use of 5 subbit per bit encoding as used in Apollo, and the adoption of a 70 kHz subcarrier and the Apollo modulation technique. It was not possible during this study to properly evaluate the cost impact to the ground station for implementing the first two options nor has the relative security attained been fully evaluated. However, the present ALSEP command format and encoding technique with the recommended modifications to the command decoder will provide the uplink security required by ALSEP. The adoption of the modulation technique employing a 70 kHz subcarrier is recommended. This approach is already being implemented in the Array D receivers as an option to provide increased address capability and will also provide increased uplink security.

6.1 70 kHz Subcarrier

When two ground stations are transmitting simultaneously, reception of false commands is possible if the two carrier frequencies are offset by approximately 1 or 2 kHz. The phase modulation resulting from the beat between the two signals, is fed through to the command decoder demodulator and can result in the generation of false commands. This possible problem is minimized when the Apollo modulation technique is used because the 1 or 2 kHz signals can be filtered at the input to the subcarrier discriminator and also because a 70 kHz frequency offset between carriers is not possible within the present ground station specifications.



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6.2 Four Bit Pattern Preamble

This option permits the removal of the inhibit between decoders A and B and therefore permits two independent signal paths from the receiver input to the decode gates. Operation is in the following manner. A four bit preamble immediately preceding the decoder address is detected and sets both decoders to search for their address for the next 7 bit period. If the address is not detected during this 7 bit period the decoder is self inhibited for a period sufficient to ensure a command execution by the addressed decoder. Implementation of this option would require minor format modification and the addition of a decoding gate and a flip flop to each decoder. If the subbit encoding and modified Apollo format option is selected for ALSEP the 3 bit (15 subbits) vehicle address can be used to fulfill this function.

6.3 Subbit Encoding

The use of 5 subbit per bit encoding as presently used on Apollo provides a second option for the decoder system.

The use of subbit encoding improves the security of the uplink in the presence of noise or unauthorized signals. This additional security is achieved at the expense of increased command word length and additional part count.

However, the problem remains that there is a possibility that other ALSEP with the same subbit encoding will interpret portions of the address and commands as their valid address. This problem is reduced in the present system by carrying out a parity check on a command complement. The proposed solution for subbit encoding is to preaddress all ALSEP's with a 3 bit code (Vehicle Address in the Apollo format). This will inhibit all ALSEP address searches for a preset period unless a valid address is detected in the 7 bits following vehicle address. (Viz section 6.2) Subbit encoding can be implemented with a modified Apollo format of 22 bit length, this would be broken down as follows:

- | | |
|--------------------|--------|
| a) Vehicle Address | 3 bits |
| b) System Address | 7 bits |
| c) Command | 7 bits |
| d) Timing | 5 bits |

This assumes that a suitable length of preamble is available, compatible with the phase lock loop bandwidth.

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6.3.1 System Address

A system address of 7 bits is retained since it is assumed sufficient to cope with future ALSEP systems.

6.3.2 Command

A command length of 7 bits is assumed to be compatible with future experiment command requirements.

6.3.3 Subbit Decoder Design

In order to accept subbit encoded addresses and commands, additional components (approximately 8 I. C. F. P. 's requiring 64 mw) will be needed at the input to the digital section of the Command Decoder. The existing 8 bit shift register will be modified to a 7 bit storage register, the address circuitry will be modified to a dual address system and there will be some minor modifications to the timing and control sections.

Referring to the block diagram in Figure 6-1, the NRZ data will be inputted to a 5 bit shift register. When the correct pattern for a vehicle address bit appears in this register the Vehicle Address Bit Detector inserts this bit into the 7 Bit Storage Register. This process continues until the Vehicle Address detector recognizes the 3 bit address. The spacing between bits is verified every 5 subbits by the synchronizing circuits which consist of a sync memory and a 5 bit ring counter. A General Reset signal is produced if this spacing is incorrect. When the Vehicle Address is detected the Programmer Counter is enabled, and the bit detection circuits are changed over to inspect for the system address and command bits. The Programmer Counter is clocked on at each bit until a count of seven is reached. If the system address is then detected the decoder is enabled to read in the remaining seven command bits into the storage register. If the system address is not detected, a General Reset signal is produced and the output of the bit detectors is inhibited by the Decoder Inhibit Circuit. The programmer counter continues the inhibit for a few seconds, until the Decoder Inhibit circuit is reset when the Programmer Counter overflows. This delay is necessary to enable the decoder which was addressed to read in and execute the command and read out its command verification word.



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6.3.4 System Trade Offs

The advantages and disadvantages of the subbit encoding over the previous methods described in this document are as follows:

- (a) Security against noise and unauthorized transmissions
- (b) Probability of a false command execute due to noise almost zero (1 in 10^{-23} approximate)
- (c) Command format compatible with NASA systems
- (d) Improved redundancy of address circuits as a result of using vehicle address to remove cross inhibiting of decoders
- (3) Parity check circuits would not be required.
- (f) Threshold detection circuits may not be required.
- (g) Increased part count and power consumption
- (h) Increased message time (4 times)
- (i) Reduced reliability of decoder circuitry.
- (j) Less chance of reading a valid address and command under noisy conditions.
- (k) Unknown cost factors of reprogramming exists MSFN ALSEP software.



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7.0 RELIABILITY CONSIDERATIONS

This section contains a discussion of the reliability analysis performed in the course of selecting the recommended configuration. Reliability predictions were derived for several alternative approaches to determine the degree of improvement achieved as a function of added redundancy. A fully redundant system including dual antennas, and diplexer filters was used as a base line to indicate the maximum practical reliability achievable. Reliability prediction with and without cross strapping were derived to gain an insight into the value of implementing signal switching (cross-strapping) between redundant components. In general, cross-strapping is difficult to implement remotely without the addition of automatic switching since a failure disables the normal command capability. It was also determined that cross-strapping itself is difficult to achieve without the added complexity required to avoid the addition of single point failure mechanisms in the cross-switching circuits themselves. Furthermore, power switching, which is not available with the present uplink components, would be required to achieve the full benefit of cross-strapping. For these reasons, cross-strapping was not seriously considered as a practical means of achieving additional reliability in the uplink electronics.

A minimum improvement configuration was developed to provide a lower bound for the minimum reliability acceptable for two year operation. This system is similar to the present ALSEP electronics with the addition of a fully redundant demodulator. The addition of a redundant demodulator circuit was selected as the minimum acceptable because this circuit contains several possible single point failure mechanisms and is believed to be the most likely location of the EASEP uplink failure. The elevated temperature swing in EASEP, caused by the thermal control degradation during the LM ascent, is believed to have caused a capacitor in the demodulator to fail.

A review of the remaining single point failure mechanisms in the uplink electronics was also performed. Selection of the recommended approach was made by choosing those improvements that could be practically implemented, that provided the most improvement, and that eliminated the most susceptible single point failures.



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7.1 Concept Comparisons

The following paragraphs contain a comparison between three concepts A, B and C in terms of estimated reliability.

Concept A is the fully redundant uplink and Concept C is the minimum redundant uplink. Concept B is the recommended system. Various predictions were calculated to determine the degree of improvement with and without cross-strapping. To achieve greater packaging density, which is required to provide a redundant demodulator without change to the command decoder form factor, a change in the type of logic employed is necessary. The change in logic from the Fairchild DTL 9040 series to TI TTL 54L logic provides an additional reliability bonus because of the net reduction in the parts required.

The present command decoder configuration is shown in Figure 7.0. The improvement achievable with the use of TTL is indicated below:

	<u>DTL</u>	<u>TTL</u>
Decoder Reliability	0.9831	0.9943
Gates and Driver Reliability	0.9728	0.9910
Command Decoder Reliability	0.9607	0.9803

In the subsequent paragraphs, all reliability prediction are based on the use of the TTL 54L series of logic.

Concepts A, B and C are depicted in Figures 7.1, 7.2 and 7.3. Reliability predictions are derived for the full redundant case, Concept A, with and without cross strapping. In all cases employing cross strapping, it is assumed that the redundant component is operated in the off condition. For the cases without cross strapping, the redundant components are all in the powered on condition which means an additional penalty in added power consumption.

An additional calculation is provided for the recommended approach, concept B, shown in Figure 7.2. The reliability prediction with cross strapping at the receiver-demodulator interface was calculated since, the redundant receiver currently under development may incorporate the means to implement cross strapping at this point. Cross strapping is being considered to provide the capability of operation with a single demodulator, i.e. compatibility with the present system.

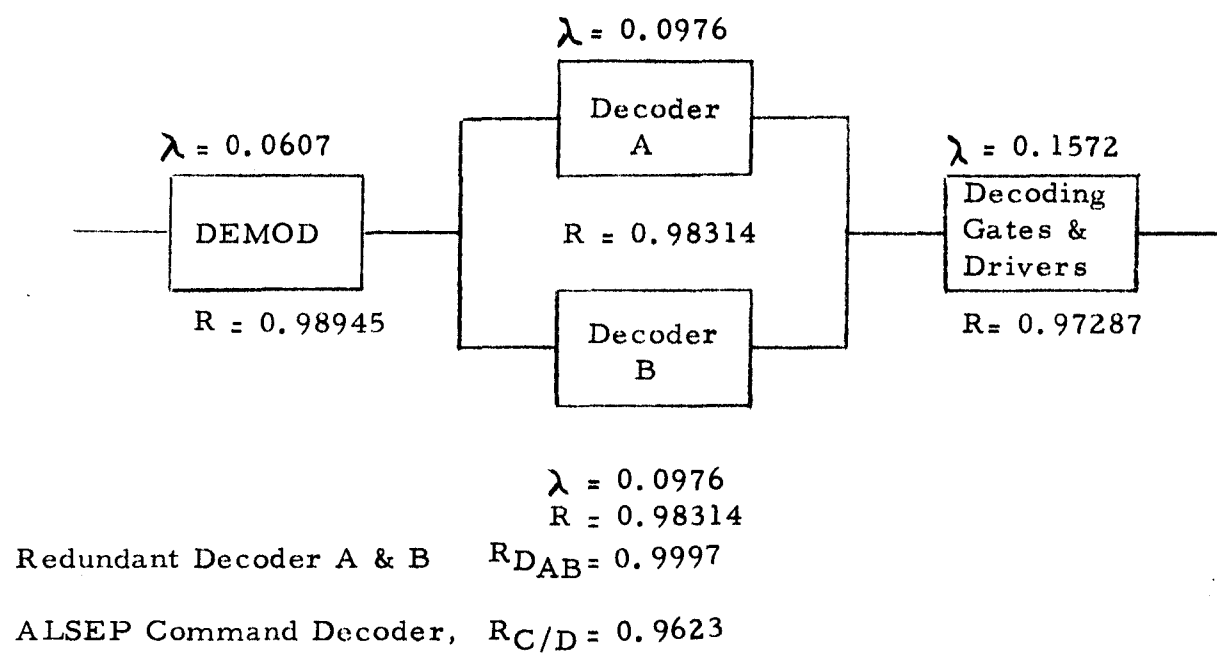
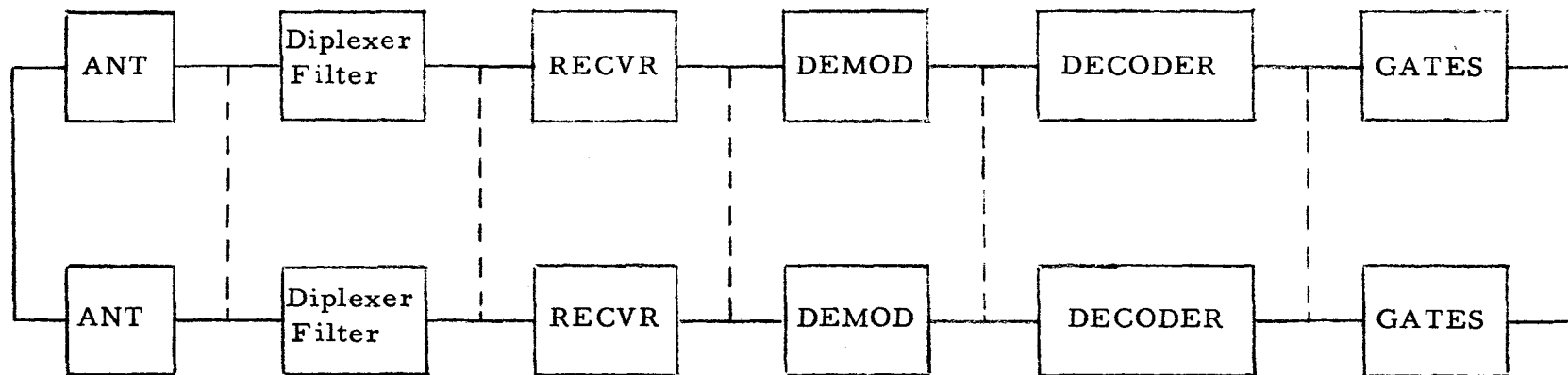


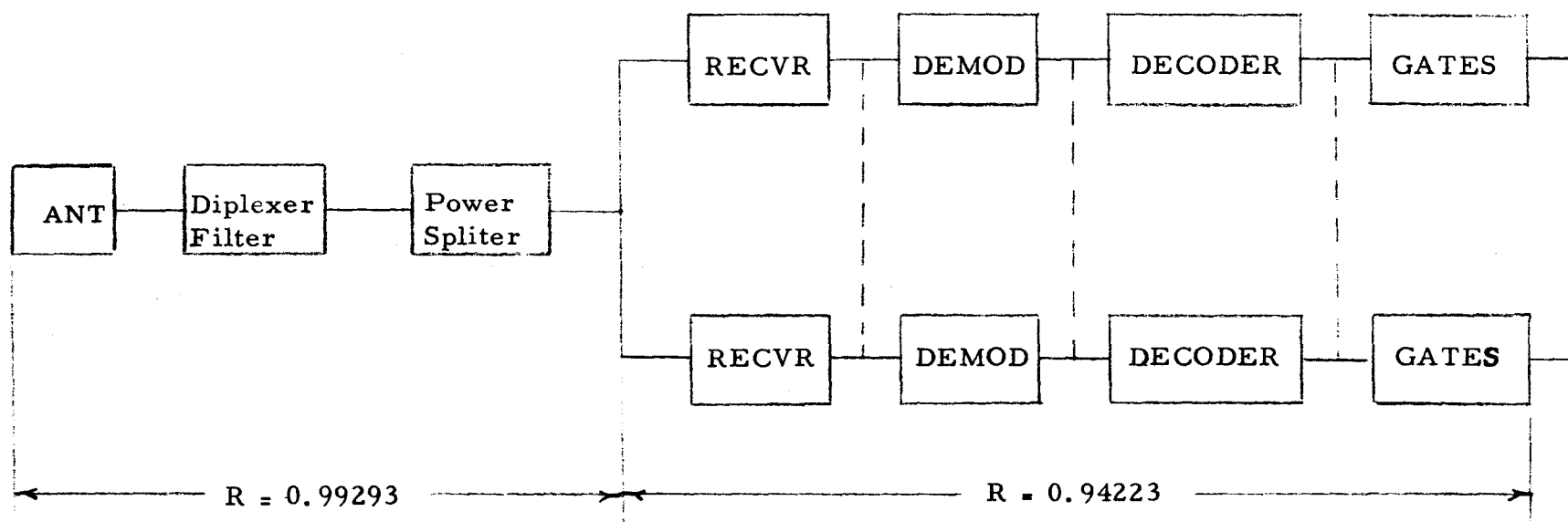
FIGURE 7.0 COMMAND DECODER (DTL LOGIC)



Reliability of Uplink Electronics without Cross Strapping = 0.99588

Reliability of Uplink Electronics with Cross Strapping = 0.99925

FIGURE 7.1 CONCEPT A UPLINK ELECTRONICS

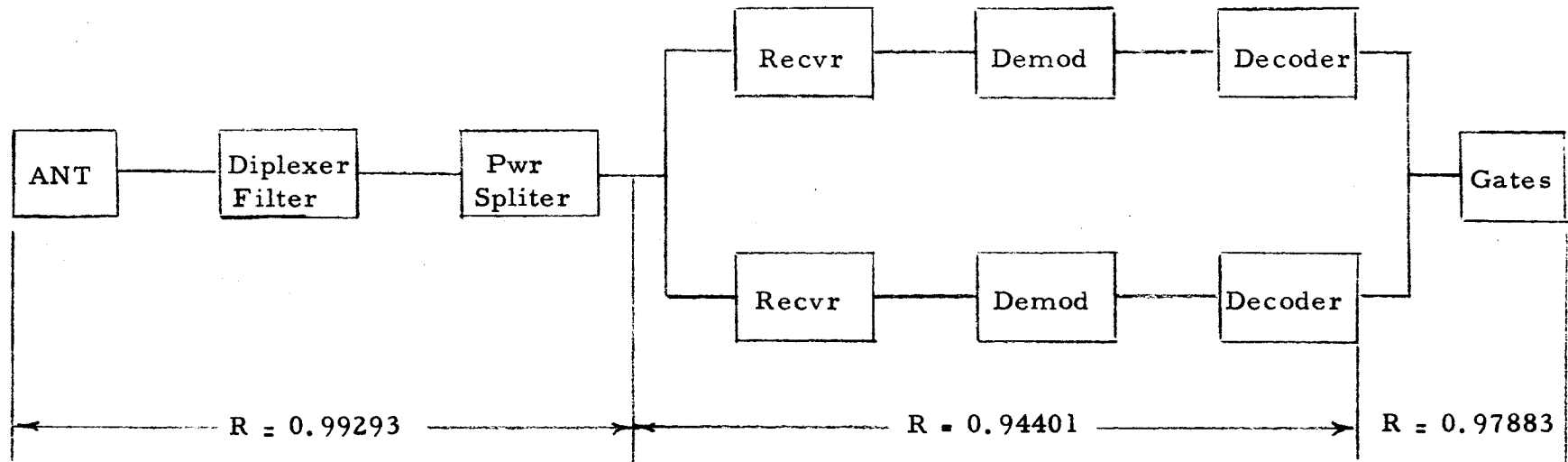


Reliability of Uplink Electronics
without Cross Strapping = 0.9896

Reliability of Uplink Electronics
with Cross Strapping = 0.99081

Reliability of Uplink Electronics
with Cross Strapping at Receiver/Demod
interface = 0.99067

FIGURE 7.2 CONCEPT B UPLINK ELECTRONICS



Reliability of Uplink Electronics with addition
of Redundant Demodulator = 0.96841

FIGURE 7.3 CONCEPT C UPLINK ELECTRONICS

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It should be noted that in each case the devices used to implement cross strapping have been assumed to have a reliability of 1.0, the ideal case. This implies that any practical means to implement such switching will degrade the idealized calculation. It is therefore apparent that cross strapping as the concept B approach does not represent a significant improvement. Concept C in Figure 7.3 provides the minimum reliability approach with the addition of the redundant demodulator only. All active elements are in the powered on mode.

As a comparison the reliability prediction for Array D without the second demodulator, for 2 year operation would be 0.9539.

7.2 Reliability Goals

The success criteria which formed the basis for the reliability goals shown in Figure 7.4 is that the central station shall be capable of accepting and decoding all earth sent commands critical for maintaining the system operation at an acceptable level.

The reliability goal selected for the uplink was derived from the Concept B of Figure 7.2.

7.3 Single Point Failures

Additional sources of single point failure exist in the uplink other than the single demodulator. Included are the antenna, the diplexer filter, the RF power splitter located in the redundant receiver, and the address A or B inhibit circuit currently employed in the decode section of the command decoder.

An additional source of failure which can result in the execution of a command not transmitted when a legitimate command is transmitted exists in the command decoder output gating. The loss of one gate can effect up to 25 commands in this manner.

The recommended approach, concept B, eliminates the address A or B inhibit failure mechanism as discussed elsewhere in this report, and also eliminates the failure of multiple command functions by an addition of redundant output gating. The remaining sources of single point failure are therefore:

- 1) Single antenna
- 2) Diplexer filter
- 3) RF Power splitter

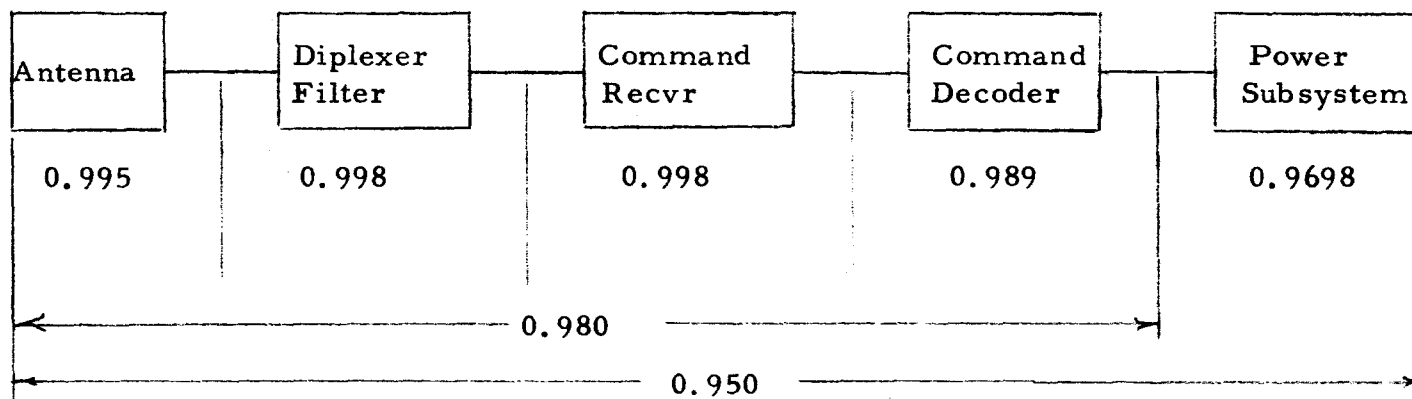


FIGURE 7.4 RELIABILITY GOALS



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Even though reliability would appear to be significantly greater utilizing parallel redundant antennas and diplexer filters, restrictions of weight and space and the fact that both the antenna and diplexer are considered passive elements do not warrant these elements being made redundant.

The power splitter (3 db coupler) which interfaces with the redundant receivers has a λ of 0.00035 or reliability of 0.99994. This coupler is a passive element which could only cause an uplink failure by an open condition. In its present usage and packaging it is highly unlikely that this element (two passive wires) could open to cause a single point failure.

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8.0 TEST PROGRAM

In conjunction with the study to provide a redundant uplink, tests were performed on the ALSEP MSFN model central station. The goal of these tests was to determine the source or sources of anomalous behavior reported for ALSEP 1. Then any needed design change to remove this anomalous behavior could be incorporated with the design changes recommended to achieve redundancy.

8.1 Uplink Anomalies

Anomalous behavior has been reported for ALSEP 1. These include spurious command verification words (CVW) with and without parity with uplink on and off, spurious status changes with uplink off, and no CVW when a command was transmitted and its functional performance verified. The anomalous CVW with uplink on are due to a reset problem in the command decoder. This effect is summarized in ATM-830, June 1969. Spurious CVW without uplink present and command executes without a CVW required further explanation. Thus tests were conducted on the ALSEP MSFN model central station to determine the sources of this anomalous behavior.

8.2 Command Decoder Operation

To transfer a command verification word to the data processor and hence transmit it via the downlink it is necessary only for output of the decoder count 63 flip flop to be low. This flip flop is set low at programmer count 63. Thus, each time the programmer reaches count 63 the data word in the command decoder shift register is transferred to the data processor upon receipt of a data demand from the data processor. Hence, to explain command verification words without uplink present it is necessary to explain how a count 63 can be reached anomalously.

One mechanism for reaching count 63 anomalously has already been explained in ATM-830. One out of eight times a CV word is transferred to the data processor the decoder fails to reset. When this occurs, the count 63 flip flop remains set and upon receipt of the data demand pulse the contents of the shift register are again transferred to the data processor. This source of anomalous CVWs, with uplink off, can only occur if count 63 is reached anomalously. Thus, a mechanism for reaching count 63 is needed to explain the transmission of command verification words without uplink present.

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The operation of the command decoder logic circuitry has been examined carefully in an effort to define a mechanism for reaching count 63 without an uplink signal. No such mechanisms have been found. Therefore, the investigation was directed toward the threshold detector to determine if its operation without uplink signal could be the cause of this anomalous behavior.

In normal operation the threshold detector, detects the presence of the received 1 kHz sync signal following lock on of the demodulator phase lock loop. Its output is applied to the direct clear terminal of the data flip flop and to the decoder reset control. Thus, when the threshold is activated the data flip flop delivers NRZ data to the decoder register and the reset and preset outputs of the reset control are set. When the seven address bits are recognized in the shift register, the address memory is set and the decoder programmer begins to count from count 29. From count 29 to 36 the command complement is read into the register. From count 36 to 43 the command is read into the register and a parity check performed. If parity is achieved the command is executed and the parity bit is placed in SR1. Count 43 to 63 is used for command execute, assuming parity. During this period, count 43 to 63, no data is shifted into the register and the threshold detector is inhibited from resetting the decoder by the parity sample enable flip flop output. When count 63 is reached the threshold detector is inhibited from resetting the decoder by a flip flop set by count 63. No NRZ data is shifted into the register after count 43 is reached until the word in the register is transferred to the data processor. Thus, the decoder is reset by the threshold going low only from counts 29 to 43, a period of 14 msec. However, the state of the threshold detector always effects the NRZ data delivered to the shift register due to the fact that its output is applied to the direct clear terminal of the data flip flop. During periods that the threshold is low only zeros can be delivered to the shift register. When the threshold is high either ones or zeros may be shifted in depending on the noise at the data demodulator input and also on the action of the data demodulator with noise as the input signal. There is a tendency for the data demodulator to be biased toward either a one or a zero with noise in. Thus, for the threshold to be involved in the generation of anomalous CVW it must be activated for a period of 14 msec following address recognition. It has been known for some time that the threshold detector could be activated by receiver noise with no uplink signal present. However, because receiver output noise spectral density was assumed to have only a slight roll off from near DC to 10 kHz and could therefore be considered Gaussian, long periods of threshold activation were not considered possible. Hence, the measurements on the ALSEP MSFN model were directed toward determining whether the threshold detector does remain high for periods exceeding 14 msec and how such operation was possible.



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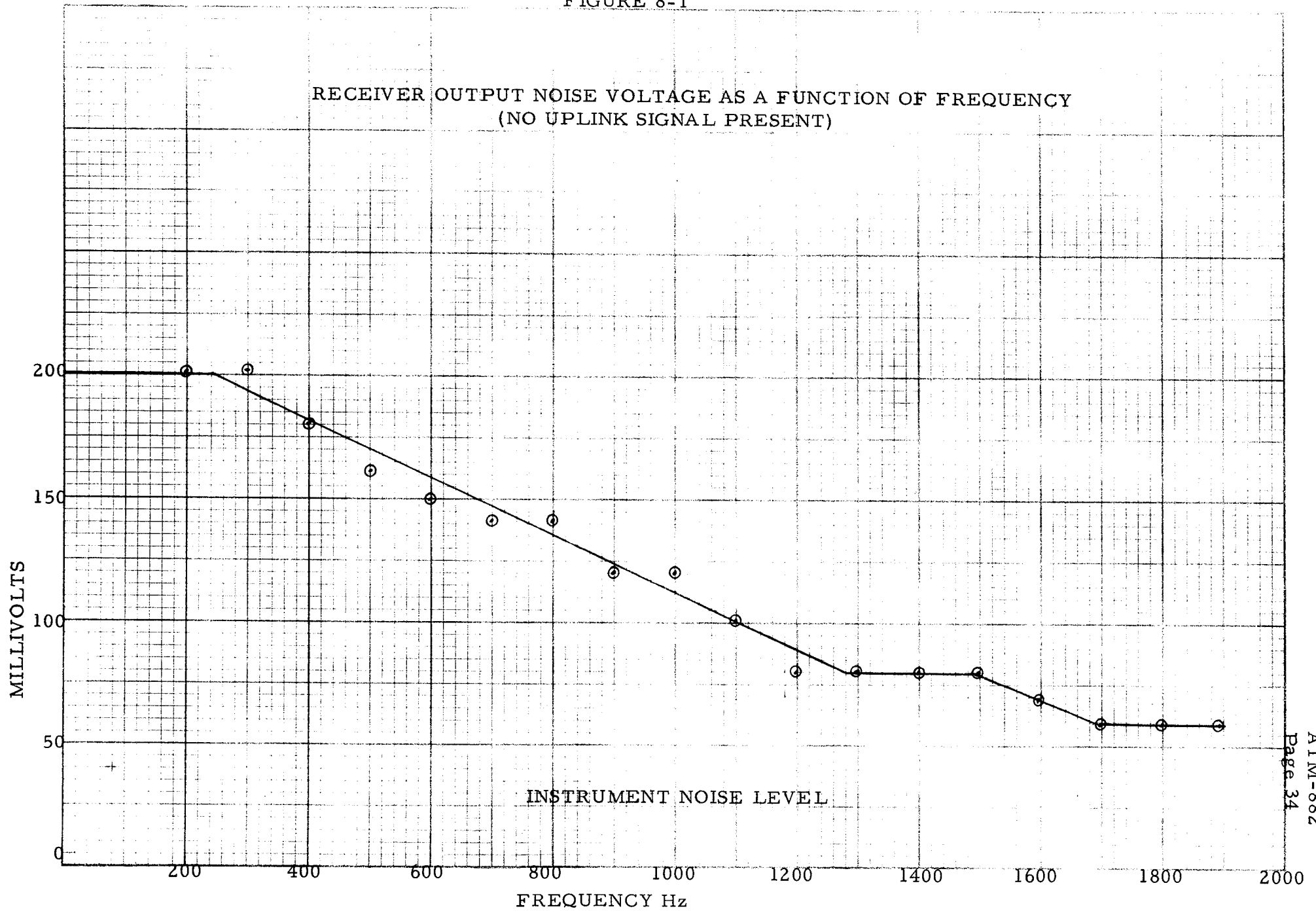
8.3 Preliminary Measurements

These test measurements were performed on the ALSEP MSFN model. Test points were brought out through a test point box (BSX 9745). All measurements were made with the uplink transmitter in standby (except for periodic system test) and the attenuator between the STS and ALSEP placed at maximum to represent a matched termination to the ALSEP receiver.

1. The threshold detector test point was displayed on an oscilloscope. Numerous threshold activations were observed.
2. The NRZ data test point and the threshold detector test point were displayed and photographed on a dual trace scope. NRZ ones and zeros appear when the threshold is high. Only NRZ zeros appear when the threshold is low.
3. The receiver output noise was displayed and photographed. The receiver output noise is clipped at a 16 volt peak to peak voltage.
4. The DC power and the output lines were removed from the receiver. No threshold activations were noted while operating in this mode.
5. The demodulator 1 kHz VCO test point was monitored and the signal frequency measured with a counter. With receiver noise into the demodulator the VCO frequency for the most part varied between 950 and 1000 Hz. With receiver power and output removed the VCO frequency stabilized near 1 kHz. This test was directed toward determining if threshold activation could be due to cross coupling of 1.06 kHz down-link data. The results imply that this is not the case.
6. The receiver output noise signal was measured as a function of frequency with HP 302A wave analyzer. The results are shown in Figure 8-1. Note that the receiver noise output is concentrated at the lower frequencies. These measurements are an average of the meter indications which varied over a range of approximately 4 to 1.

FIGURE 8-1

RECEIVER OUTPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY
(NO UPLINK SIGNAL PRESENT)



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7. The output noise signal from the receiver was used to drive a separate demodulator circuit that had a greater number of test points available. The output voltage of the demodulator input amplifier was displayed and photographed. The noise voltage at this point is further clipped to a peak to peak value of approximately 11 volts. The noise signal and the threshold detector test point were displayed and photographed. During one threshold high period, a period of 10 msec, a 1 kHz component in the noise is easily discernible.
8. The decoder reset test point was used to trigger a counter to determine length of time that the reset line was high. Only periods greater than 2 msec were recorded. Over a 15 minute period, 10 reset periods greater than 2 m seconds were recorded, one with 12 msec duration and one with 16 msec duration. It should be noted that the counter was also triggered by the clock pulse that appears on the reset test point when the threshold detector is low. This had the effect of giving many apparent reset periods equal to the clock period (1 msec). For this reason only periods greater than 2 msec were recorded.
9. The address memory was monitored during a 20 minute period to determine the rate at which false addresses are detected. The address memory was set 26 times during this period. The time period the address memory was set was recorded for the final 20 recognitions. (The address memory is reset if the threshold goes low during the 14 msec following address recognition.)

These time periods were as follows:

1 msec or less	12
2 msec	2
4 msec	3
5 msec	2
10 msec or greater	1

The address monitored for this test was Octal 116.



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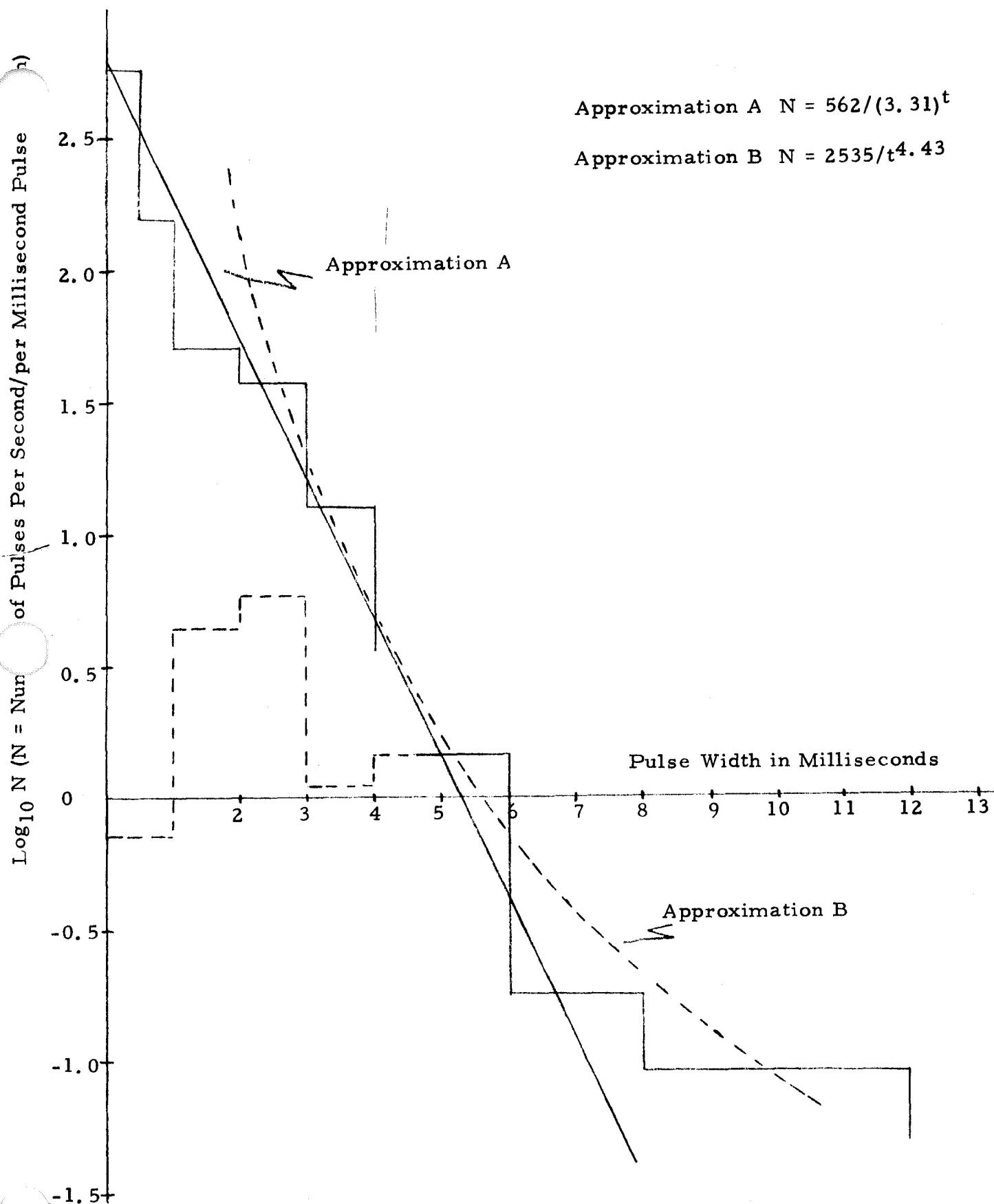
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An analysis was performed on the photographs of the displayed threshold detector test point to determine the frequency of threshold pulses as a function of pulse width. Figure 8-2 is the result. Note that the lower part of the curve is derived from photographs of 20 msec/cm and 50 msec/cm traces (a total of 2800 msec) and the upper curve from photographs of 2 msec/cm traces (a total of 80 msec). The histogram derived from the 20 msec/cm and 50 msec/cm traces is unreliable for short pulse lengths because of resolution limitations. Extrapolating the empirically fitted curve suggests that pulse widths greater than 14 msec should occur about once per 11 seconds and pulse widths greater than 21 msec about once per 47 seconds. These are rough estimates which are valid only for order-of-magnitude calculations. Although it is possible for a CVW to be generated due to a 14 msec pulse length if it immediately follows an address recognition due to the random bit stream, the most likely mechanism for spurious CVW generation requires a pulse length greater than 18 msec. Using the rate of occurrence of such pulse lengths from figure 8-2 and the observed mark-space space ratio the predicted rate of spurious CVW is one per 2000 seconds. The long term tests discussed in paragraph 8.5 show spurious CVW occurring at a rate of approximately one per 1600 seconds. The predicted and measured rates are in surprisingly good agreement considering the gross estimates used in deriving them.

The above discussion refers only to the random generation of CVW. Random command executions resulting in a status change will be much less frequent.

FIGURE 8-2. FREQUENCY OF THRESHOLD PULSES
AS A FUNCTION OF PULSE WIDTH



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8.4 Discussion

These tests show strong evidence that the threshold detector, activated by receiver noise, is involved in the anomalous reception of status changes and the transmission of anomalous command verification words. Past considerations that were based on an essentially random noise input to the demodulator do not adequately define the actual operation of the threshold detector with no uplink signal present. First, the receiver noise output is not broad band but concentrated at the low frequencies. Second, the large loop bandwidth of the demodulator phase lock loop permits rapid tracking of the input noise signal and therefore enhances threshold activation by the noise signal. The large 1 kHz component of the noise that appears periodically makes it doubtful that improvements to the present threshold detector scheme, such as filtering or reducing loop bandwidth, will result in elimination of the present problems, although the reduction of the loop bandwidth would no doubt provide improvement. There is reason to believe that a threshold detector activated by the 2 kHz subcarrier signal can result in a further improvement. First, because the phase of the 2 kHz noise component is not coherent with the 1 kHz component, the action of the phase lock loop does not enhance threshold activation and second the measured 2 kHz component of the noise is considerably less than the 1 kHz component although it is possible that this second point may prove invalid for the redundant receiver in development.

8.5 Long Term Tests

The second group of tests included operation of the MSFN model central station with no uplink signal - receiver operating, no uplink signal-receiver not operating, and uplink carrier only-receiver operating. These tests were designed (1) to provide a statistical model of the anomalous behavior for the ALSEP MSFN model central station that could be compared with ALSEP 1 and (2) to determine if any mechanisms other than those already defined could be contributing to the anomalous behavior.

The MSFN model central station was operated with no uplink signal for a total of 91 hours. During this period a total of 207 CVW's were recorded. Four of these CVW's showed parity.

The MSFN model central station was operated with power removed from the receiver and the receiver disconnected from the command decoder demodulator for a total of 21 hours. No CVW's were recorded during this period.

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The MSFN model central station was operated with the uplink carrier on (no modulation) for a total of 28 hours. With the uplink carrier on the receiver output noise is reduced by approximately 20 db. No CVW's were recorded during this period.

Thus CVW's were recorded at a rate slightly greater than two per hour when high receiver noise was delivered to the command decoder demodulator. No CVW's were recorded when this noise signal was removed. These results support the argument that noise acting on the demodulator is the principal cause of anomalous CVW's.

Statistical analysis was applied to the test results with no uplink present and receiver operating to determine if the results were essentially random or if they were systematic and to provide a model for comparison of the results from ALSEP 1. The 207 CVW's recorded showed a ratio of "ones" to zeros of approximately 4/3. Although it might be expected that ones and zeros should have equal probability, past measurements on the data demodulator show that it is often biased toward a one or zero when there is no 2 kHz signal present. Knowledge of the one/zero ratio allows the prediction of the number of CVW's containing a specific number of ones and zeros. Table 1 is a comparison of the values predicted on the basis of a 4/3 ratio and the measured values.

No. of 1's in command Word	Predicted occurrence	Measured occurrence
0	0.5	1
1	5.2	6
2	21.2	21
3	46.4	54
4	60.4	50
5	47.4	48
6	20.8	21
7	3.9	5

Note that the predicted rate of occurrence and the measured rate of occurrence correlate reasonably well. This implies that the anomalous CVW's can be explained by the noise activating the threshold detector and are not due to a systematic anomalous behavior.



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It is also possible to predict the rate of occurrence of possible status changes due to noise operating the threshold detector. A possible status change is defined as occurring when the 14 bits following address detection consist of two 7 bit words that are complementary. The predicted number of occurrences may be expressed as $P(1)^7 \cdot P(0)^7 \cdot 2^7 N$

where $P(1)$ = probability of a one occurring when the threshold is high = $1/(r+1)$

$P(0)$ = probability of a zero occurring when the threshold is high = $r/(r+1)$

N = number of CVW

r = ratio of zeros to ones in bit stream when threshold is high.

Figure 8-3 is a graph of $P(1)^7 \cdot P(0)^7$ as a function of r .

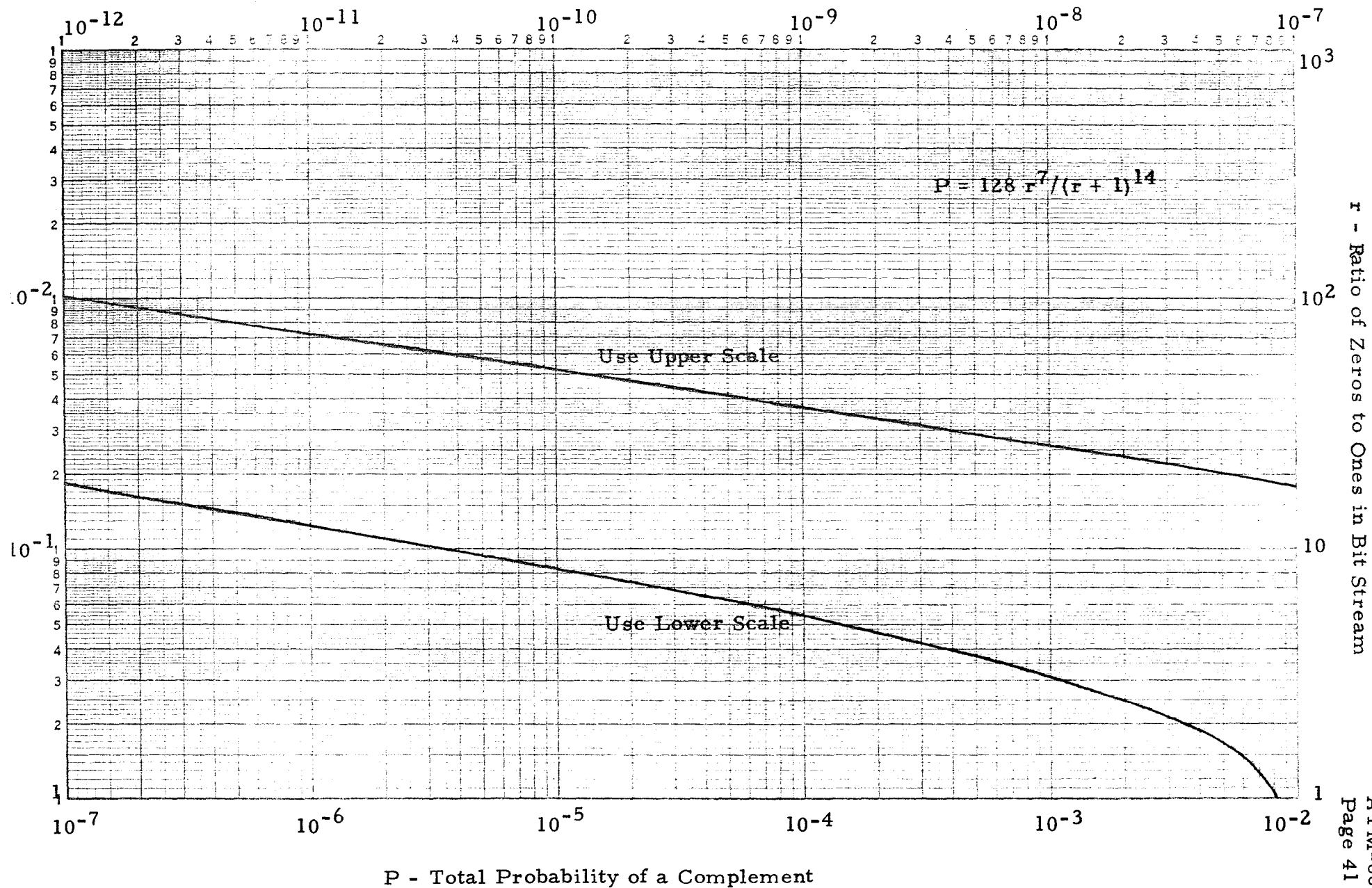
The predicted result for $N = 207$ is 1.4. Actually four CVW with parity were recorded. However, there exists a second mechanism for generating CVW's with parity.

The CVW transmitted when the decoder reset fails is simply the contents of decoder shift register, read in when the prior CVW is read out. Thus, if the parity position of the register contains a logical 1 when the second CVW is readout, the result is a CVW with parity. Examination of the data show that two CVW with parity appeared in the data frame immediately following reception of a CVW without parity. Hence, the likelihood is that these two are due to reset failure and do not represent a possible status change. This leaves two possible status changes due to noise only, which approaches the predicted value.

The number of CVW due to the decoder reset failure is also of interest. Each time the decoder fails to reset a second CVW should be transmitted. Only four such events were recorded during the 91 hour test. Reset failure should occur approximately one time in seven that a CVW is transmitted.

Thus, the expectation is that approximately 30 of the recorded CVW will be due to this cause. That this is not the case must be due to the fact that only logical 0's are read into the shift register during the 7 msec CVW readout period. When only 0's are contained in the shift register, a CVW containing only 0's is transmitted. However, such words are not recognized as CVW.

FIGURE 8-3 PROBABILITY OF A COMPLEMENT OCCURRING



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8.6 Comparison of Measured Data With ALSEP 1 Data

Analysis similar to that applied to the MSFN model CVW activity was also applied to the reported CVW activity for ALSEP 1 for the period from the beginning of day 14 to the end of day 127. This particular period was chosen because the available data is the most complete. During this period, a total of 2210 CVW were reported. (See the Appendix for the complete list.) The total number of hours for which data exist is 2,460. Thus, CVW were recorded at a rate of approximately one per hour or one-half the rate for the MSFN model.

The ratio of zeros to ones in the CVW without parity was 1:1,073. A comparison of the expected and actual number of CVW with given number of 1's is as follows:

<u>Number of 1's in Command Word</u>	<u>Predicted Occurrence</u>	<u>Measured Occurrence</u>
0	14	Not known
1	102	105
2	324	317
3	591	601
4	632	598
5	406	418
6	145	157
7	22	14

The correlation between predicted and measured rates of occurrence is fairly good, suggesting that a simple statistical response to a random bit stream is the dominant mechanism producing CVW without parity.

On the assumption that the ALSEP 1 noise spectrum is similar to that of the MSFN model an attempt was made to estimate the ALSEP spurious CVW rate. Again the estimate is based only on the longer threshold pulses. However, because the ALSEP 1 decoder address word has a logical one appearing earlier than does the MSFN decoder address word, somewhat longer pulses are generally required for generation of a spurious CVW. This estimate for ALSEP 1 is one spurious CVW per 3000 seconds. The reported rate is approximately one per 4000 seconds. Again, the predicted and reported rates are in surprisingly close agreement considering the gross estimates used.



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Based on the 0/1 ratio, the predicted number of CVW with parity for the entire period (not counting those due to reset failure) is 17. Some Command Words with genuine parity will not execute because they are not valid ALSEP 1 commands, others will be blocked by incorrect sequencing or by being existing status. A study of ALSEP 1 command list suggests that a genuinely complemented random Command Word has a 1-in-3 chance of producing an observable execution. On this basis there should have been 5.7 observed executions in the period of interest; in fact there were four. This is certainly not excellent agreement, but four could occur by chance 15% of the time when the expectation is 5.7. The CVW with parity reported for this period is 130. (See the Appendix for the complete list.) It is apparent, from examination of the station reports, that many of these reported CVW with parity are not due to anomalous behaviour of ALSEP 1. Many are related to real time support and the octal 177's due to reset failure during periods of real time support (a maximum of 88). Others occurred during periods of large signal fluctuation or when decommutator dropouts were reported. In seven cases CVW with parity were reported by one station and not by another although both were receiving at the time. Thus, comparison of the predicted rate of occurrence of CVW with parity with the measured value is not possible.

The ALSEP 1 data was also analyzed to determine the rate of occurrence of CVW due to the reset failure with no uplink present. Approximately 500 of the reported CVW have their time of occurrence listed to sufficient accuracy for analysis. Analysis of these yielded only two CVW that could have been due to the reset failure. Thus, for both the MSFN model and ALSEP 1, CVW due to reset failure with no uplink is a rare occurrence.

8.7 No CVW When a Command Is Transmitted and its Functional
Performance Verified

For the first 1,753 commands transmitted to ALSEP 1 and executed by ALSEP 1, there were 27 occurrences where no CVW was received by the ground station. Therefore, tests were conducted on the MSFN model to determine whether this model exhibited the same anomalous behavior. Five hundred commands were transmitted to the MSFN model and a CVW was received every time.

If this behavior occurred at the same rate for the MSFN model as exhibited by ALSEP 1, the failure to receive a CVW should have occurred approximately seven times in 500 trials. Therefore, the MSFN model when operated with a test set does not show the same anomalous behavior reported for ALSEP 1.

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8.8 Conclusion

The tests on the MSFN model of the ALSEP central station show that anomalous CVW activity, and in some cases the reception of falsely generated commands, is due to the activation of the demodulator threshold detector by the receiver output noise with no uplink present and by the decoder reset failure. No other causes of anomalous behavior were uncovered.

Although it is not possible to provide a correlation between the anomalous CVW activity of ALSEP 1 and that of the MSFN model, no evidence has been uncovered that is contrary to the conclusion that this anomalous behavior is due only to the command decoder reset failure and the operation of the demodulator with a large noise input.

The apparent discrepancies in the behavior of ALSEP 1 when compared with the MSFN ALSEP and with simple statistical theory will probably never be conclusively explained. However, after considerable examination of all available data and the consideration of possible mechanisms within ALSEP it is difficult to avoid the opinion that the remaining, relatively minor anomalies must arise within the ground reporting system and/or procedures. To assume otherwise requires the postulation of highly contrived, intermittent faults within ALSEP 1 to explain less than 1% of the reported events.



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9741-373	Spurious CVW and Commands Due to Simultaneous Operation of Two Uplink Carriers
9741-377	Discussion on Subbit Encoding
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971-34	A Simple Statistical Study of ALSEP Command Anomalies



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CVW WITHOUT PARITY REPORTED FOR ALSEP 1
(Day 14 to Day 127)

<u>Octal</u>	<u>Number Reported</u>	<u>Octal</u>	<u>Number Reported</u>	<u>Octal</u>	<u>Number Reported</u>	<u>Octal</u>	<u>Number Reported</u>
000		040	9	100	17	140	15
001	12	041	7	101	16	141	16
002	13	042	9	102	11	142	18
003	14	043	15	103	13	143	15
004	14	044	14	104	16	144	19
005	17	045	18	105	18	145	14
006	11	046	18	106	23	146	17
007	22	047	16	107	19	147	17
010	21	050	20	110	20	150	15
011	12	051	21	111	20	151	18
012	11	052	22	112	20	152	18
013	16	053	21	113	21	153	22
014	18	054	22	114	19	154	17
015	13	055	18	115	15	155	13
016	13	056	20	116	7	156	23
017	21	057	23	117	22	157	17
020	19	060	15	120	23	160	11
021	17	061	14	121	16	161	11
022	18	062	15	122	22	162	22
023	16	063	24	123	11	163	17
024	20	064	17	124	17	164	15
025	18	065	24	125	35	165	22
026	20	066	10	126	24	166	21
027	24	067	16	127	19	167	22
030	13	070	10	130	8	170	13
031	20	071	16	131	13	171	24
032	16	072	8	132	17	172	24
033	15	073	18	133	18	173	26
034	20	074	19	134	9	174	25
035	13	075	15	135	19	175	25
036	18	076	17	136	28	176	28
037	16	077	20	137	19	177	14



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CVW WITH PARITY REPORTED FOR ALSEP 1
(Day 14 to Day 127)

<u>Octal</u>	<u>Number Reported</u>	<u>Comment</u>
000	5	Four reported by one station during a 4 hour period. One occurred during period of 10 db signal fluctuations.
003	1	
004	1	May have been due to reset failure.
006	2	
013	1	
015	1	
017	1	
032	2	One occurred during period of real time support (RTS).
044	1	
052	2	One occurred during period of RTS
053	3	Three due to RTS
054	3	Three due to RTS
055	3	Three probably due to RTS
057	1	
066	9	Minimum of eight due to RTS
070	13	Minimum of twelve due to RTS
071	10	Minimum of eight due to RTS
072	6	Minimum of six due to RTS
077	2	
103	9	Minimum of nine due to RTS
112	1	
114	1	
117	1	
123	1	
124	1	
127	1	
130	1	
131	7	Minimum of six due to RTS
137	1	
140	1	
142	1	
144	1	
154	1	
160	1	
161	1	
164	1	
165	1	
172	1	
177	30	Minimum of sixteen occurred during period of RTS