Bendix

Aerospace Systems Division

NO.	REV. NO.
ATM-971	
PAGE ____ OF ____	
DATE 4/7/71	

ALSEP ARRAY E

CROSSTALK AND GROUND DIFFERENTIALS

IN THE CENTRAL STATION

Prepared by: R. A. Ziesmer
R. A. Ziesmer

Approved by: D. J. Dautlat

1.0 SUMMARY

The length of signal paths have been minimized to reduce crosstalk to acceptable levels. This study identifies residual problems and suggests solutions.

Interwire interference between digital signals produced by 54L logic elements is caused mainly by capacitive coupling. Due to the nature of the crosstalk mechanism and the output impedance of the logic elements, crosstalk to a logic zero level will not pose a problem in the Central Station wire harness. Crosstalk to unprotected logic one levels may cause signal interference in worst case conditions.

The design of the Central Station is such that most of the synchronous signals in the wire harness are at a logic one only when no other synchronous signal is switching. Therefore most of the synchronous signals will be logic zero levels at critical times and will be mutually compatible. The asynchronous signals will be shielded to eliminate crosstalk to the synchronous signals. This will also prevent mutual asychronous signal interference. With the exception of three synchronous signals between the Command Decoder and the Data Processor which will be shielded, this is the only crosstalk control required.

Calculations are presented which indicate that transient ground differentials will be well within worst case design margins.

2.0 BACKGROUND:

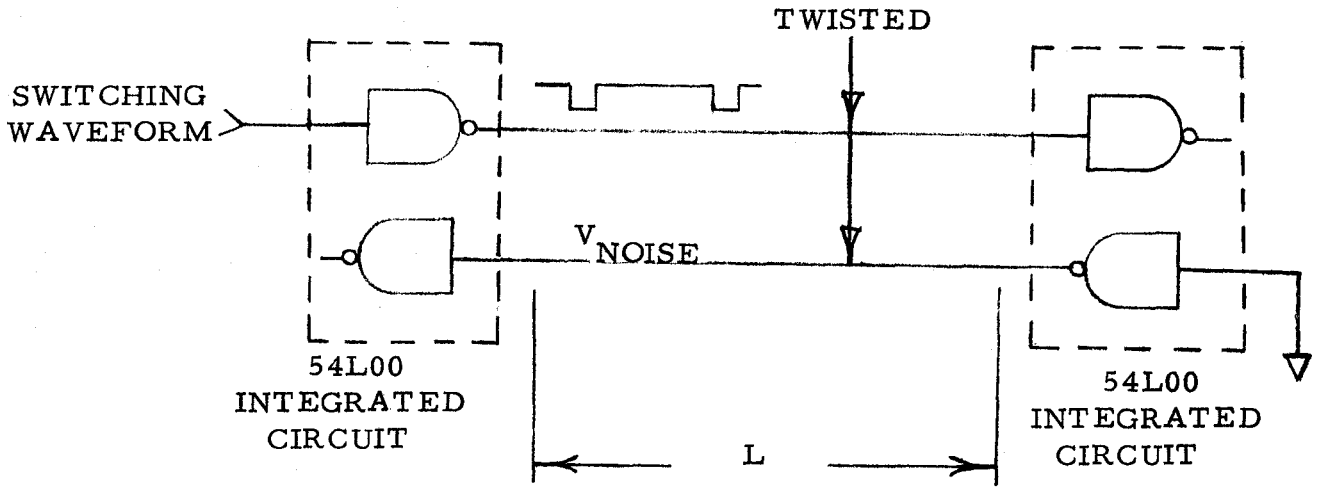
2.1 INTERWIRE INTERFERENCE

Within the Central Station, 54L series logic elements will be used to interface with the internal wire harness. The crosstalk which appears on any of the signal lines due to switching of another signal in the harness must be limited to less than the noise margin of the receiving circuit. To determine the techniques necessary to limit the crosstalk to less than the noise margin, the following study was undertaken. First the amount of crosstalk that will appear in an unprotected wire harness was determined.

The coupling between signal lines in the harness was determined to be due mainly to interwire capacitance and not due to magnetic effects. This may be expected due to the small $\frac{dI}{dt}$ compared to the $\frac{dv}{dt}$ on the signal lines. The amplitude of current change to voltage change is approximately $\frac{100 \text{ microamperes}}{4 \text{ volts}} = 2.5 \times 10^{-5}$. Therefore $\frac{dI}{dt} << \frac{dv}{dt}$.

An analytical study of the crosstalk will be presented assuming capacitive coupling. The results of the analysis will then be compared with empirical data to confirm the validity of the model. The model is presented as an aid to an intiutive understanding of the crosstalk mechanism.

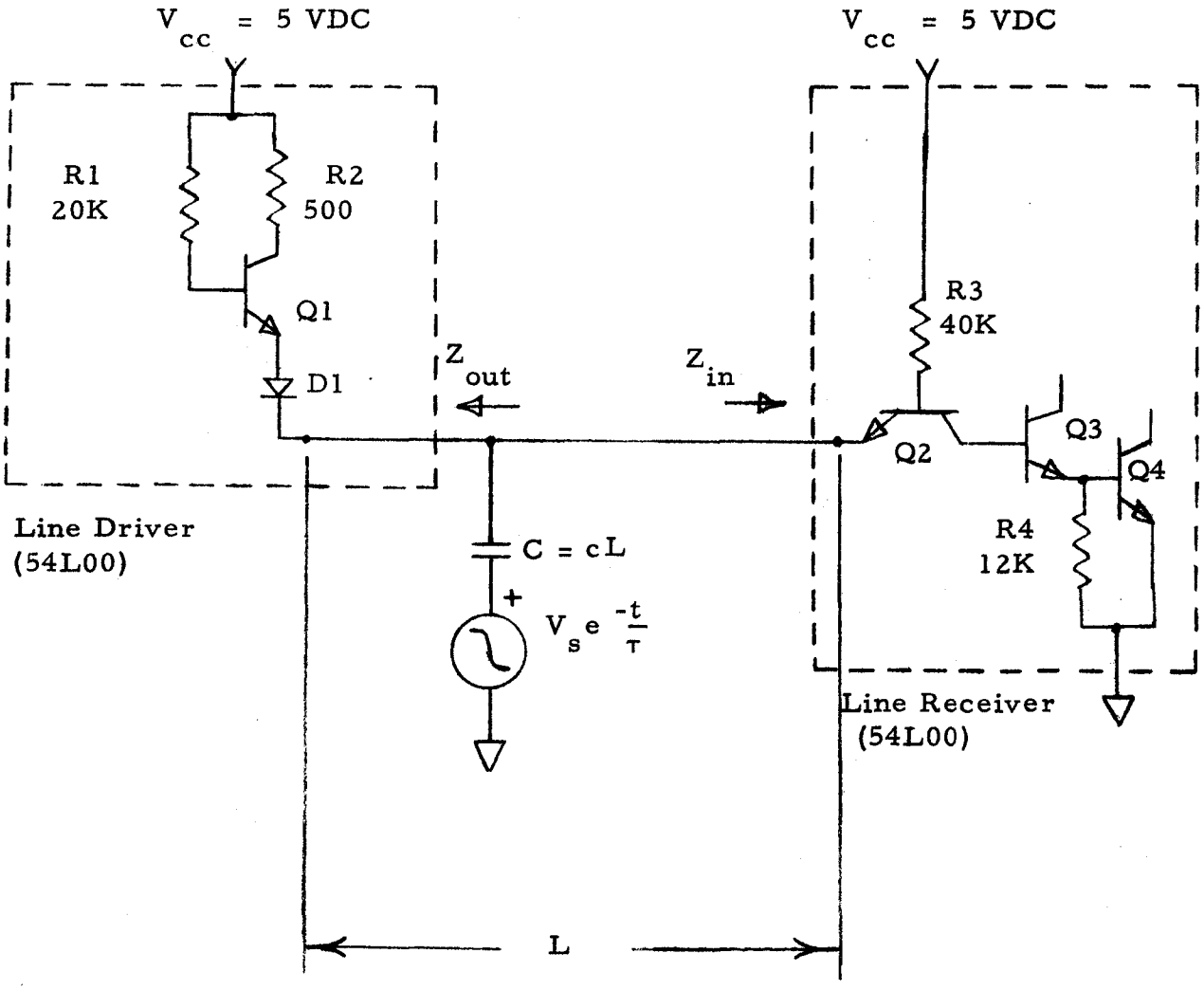
The circuit of Figure 1 is the configuration to be modeled. The line which is talked to, the V_{noise} line, is continually driven with a logic one level. The parallel line has a pulse train with period and pulse width sufficiently long that the crosstalk produced by each edge is independent. The wire used for the cable in this study is the same wire that will be used in the Central Station wire harness. It is AWG 24 gauge, stranded, teflon insulated wire.



NOTE: Wire, #24, stranded, teflon insulated

Crosstalk Circuit
Figure 1

Figure 2 presents the model that will be used to describe the performance of the interface circuits of Figure 1. A mathematical expression for the amount of crosstalk, V_{noise}, superimposed on the logic one level due to a falling edge on the adjacent conductor will be developed from this model.



Crosstalk Model
Figure 2

In the model, L is the length of adjacent conductors, c is the inter-wire capacitance per foot, and $V_s e^{\frac{-t}{\tau}}$ is the model for the falling edge of the switching waveform, The fall time of the switching waveform equals 2.2τ and the amplitude of the falling waveform is V_s.

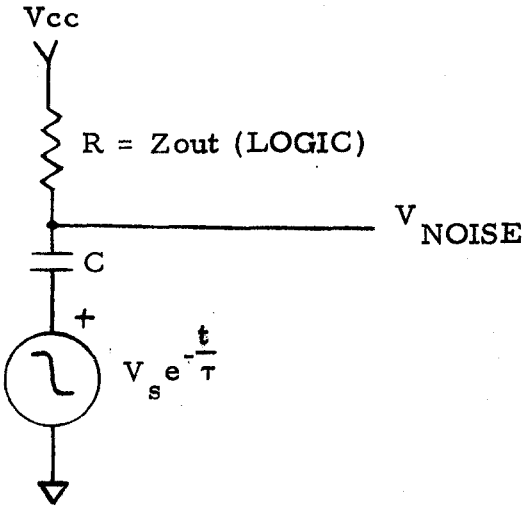
The transistor circuits in Figure 2, labeled line driver and line receiver, are the output and input circuits respectively of the 54L00 logic elements interfacing with the harness.

The output impedance of the line driver is given by equation 1.

Equation 1: $$R_{out} \cong \frac{R_1}{h_{fe1}}$$

where h_{fe1} is the gain of transistor Q1 and R1 is its base resistor.

Equation 1 is derived in the appendix, section 3.1, and is supported by empirical data. The impedance as described by equation 1 is purely resistive with a value of approximately 10^3 ohms, since R_1 = 20K ohms and $h_{fe} \cong 20$.



Simplified Crosstalk Model

Figure 3

The base to emitter junction of the line receiver's input transistor, Q2, is reverse biased when driven by a logic one. Consequently the input impedance of the line receiver is high compared to the output impedance of the line driver.

Because Z_{in} and Z_{out} are parallel, and $Z_{in} > Z_{out}$, the impedance from the V_{noise} conductor to ground is approximately equal to Z_{out}.

Therefore, the model for crosstalk can be simplified and redrawn as in Figure 3, where the line driver and line receiver for the V_{noise} conductor are replaced with one resistor of value equal to Z_{out}.

Equation 2 describes the transient voltage waveform at V_{noise} for the simplified model.

Equation 2: $$V_{noise} = \frac{RCV_S}{RC-\tau}\left[e^{\frac{t}{-\tau}} - e^{\frac{t}{-RC}} \right]$$

for $\tau \neq RC$

By differentiating the equation for V_{noise} with respect to time and setting it equal to zero, the time at which V_{noise} has its maximum amplitude can be determined. The expression for the time of maximum crosstalk is presented as Equation 3. Equations 2 and 3 are derived in detail in the appendix in Sections 3.2 and 3.3 respectively.

Equation 3: $$t \text{ (for } V_{noise} \text{ MAXIMUM)} = \frac{(\tau RC)\, \ell n \left(\frac{RC}{\tau}\right)}{RC-\tau}$$

The maximum amplitude of the crosstalk can be determined by first evaluating equation 3 for the time when maximum voltage occurs. Using this time in the V_{noise} expression, equation 2, and using the values of V_s, τ, R, L and c, the maximum crosstalk amplitude can be calculated.

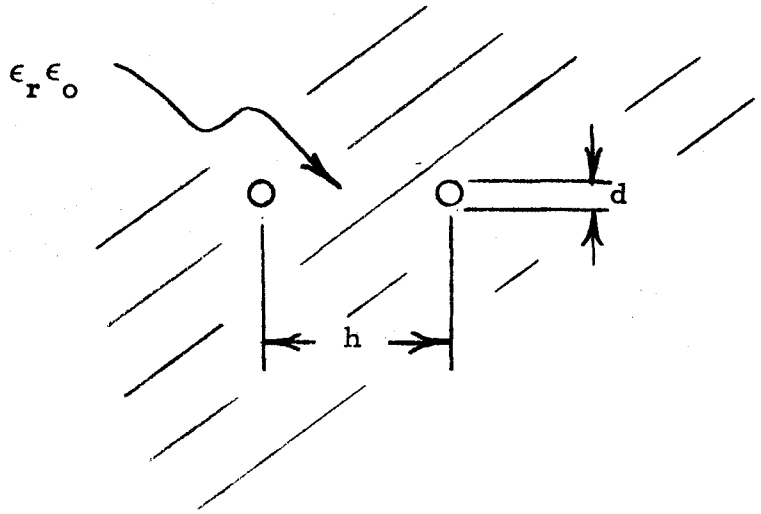
The solutions for equations 2 and 3 will be presented for the case L = 2 feet. These solutions will be compared to pictorial data for the same case.

The values of V_s and τ have been measured for the case under study. Their values are V_s = 4 volts, and τ = 30 nanoseconds; supporting data is given in the empirical section of this report. The value of R has been presented as 10^3 ohms.

The value of interwire capacitance per unit length, c, can be calculated using equation 4 when the geometry of the parallel conductors and the dielectric constant of the insulation are known.

$$c \simeq \frac{\pi \epsilon_r \epsilon_o}{\ln\left(\frac{2h}{d}\right)} \qquad \frac{\text{FARADS}}{\text{METER}}^{1}$$

Where $\epsilon_r \epsilon_o$ is the dielectric constant of the material surrounding the conductors and the dimensions, h and d, are defined in Figure 4.



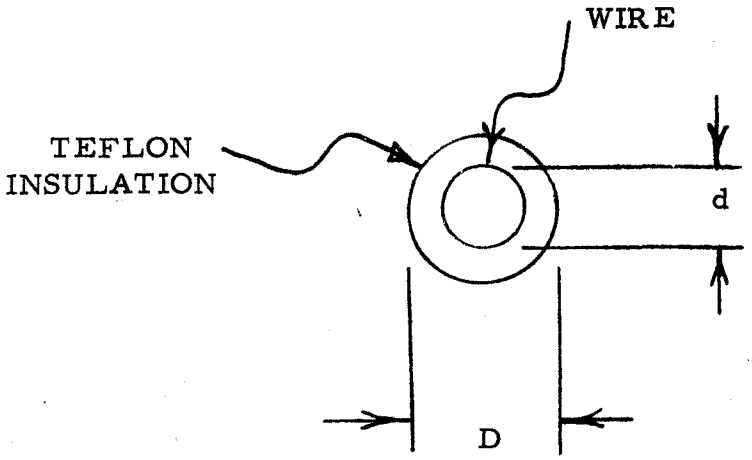
Capacitance Between Two Parallel Wires

Figure 4

Equation 4 applies for two parallel wires immersed in a uniform dielectric. For the case under study, the dielectric constant will not be uniform over space nor will the conductors have uniform spacing over the length of the cable. The maximum interwire capacitance will be calculated, however, assuming the wires are as close together as the insulation will allow and that the dielectric constant is uniformly that of teflon.

[1] Pulse, Digital, and Switching Waveforms, by Millman and Taub, Page 85.

The dimensions of the wire used in this study were determined by measurement with a micrometer. The wire dimensions are presented in Figure 5.



$d = 0.023$ inches

$D = 0.035$ inches

ϵ_r = (Teflon) = 2.1

Dimensions of Wire Used in Study

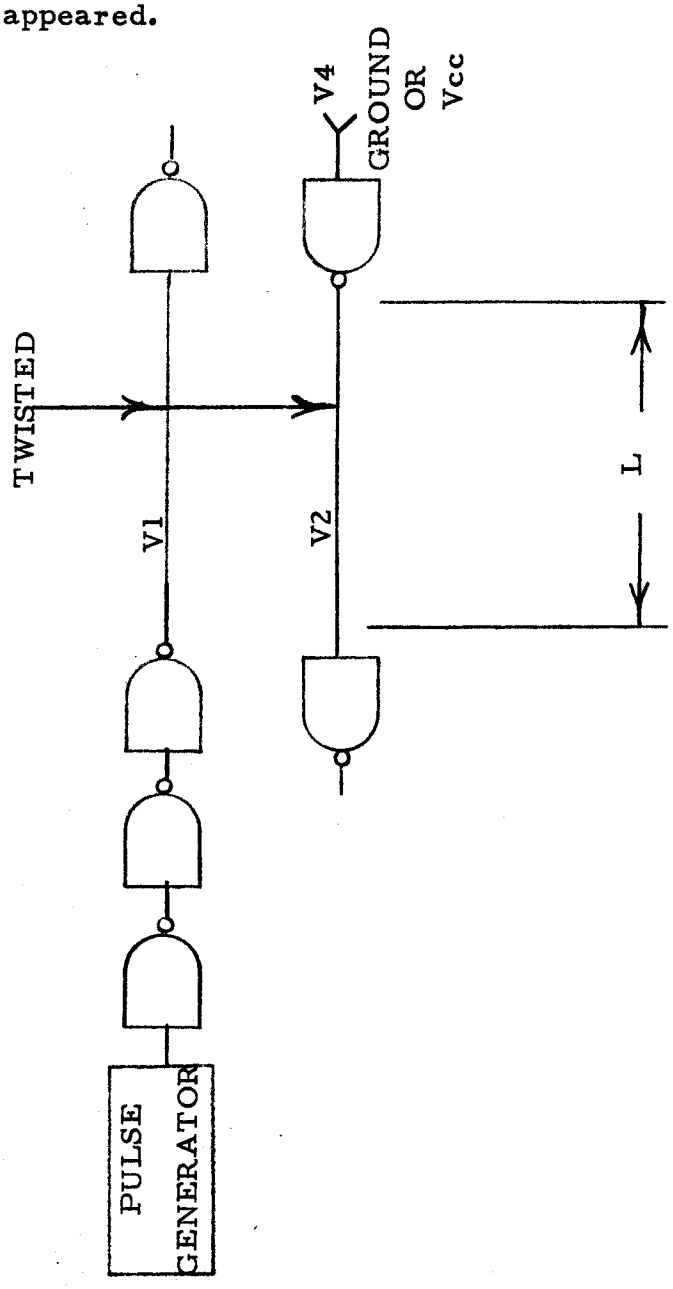
Figure 5

Using equation 4 with d = 0.023 inches and h = (0.035) inches, the calculated value of c is 16.0 pf/ft.

Because the distance between the conductors on the average must be greater than the thickness of the insulation and the average dielectric constant will be less than that of teflon, the calculated value of capacitance is greater than the capacitance experienced within the wire harness. Past experience shows that the actual value of interwire capacitance is approximately one half of this calculated value. Therefore, the value of capacitance to be used in the model is 8 picofarads/foot.

Using the before mentioned parametric values and equation 3, the maximum crosstalk amplitude is calculated to occur 15 nanoseconds after the switching waveform on the adjacent conductor begins to fall. Using equation 2, the crosstalk amplitude is calculated to be 1.5 volts negative from the logic one level.

A picture of the crosstalk waveform for line length of two feet is presented on page 11. It shows a negative going spike of 1.4 volts from the logic one level which occurred 28 nanoseconds after the crosstalk first appeared.



Test Circuit

Figure 6

The good correspondence between the empirical data and the model response is presented as an indication that the mechanism which produces the crosstalk is capacitive coupling. The model as presented is intended for use as an aid for intuitive understanding of the crosstalk and not necessarily as a precision analytical tool. To this end, the correspondence of empirical data to model response appears more than adequate.

The circuit of Figure 6 was used to collect the empirical crosstalk data. The cable consisted of two AWG 24 gauge, teflon insulated, stranded wires which were tightly twisted to simulate worst case coupling conditions. Data was taken for crosstalk to both logic one and logic zero levels, where the steady state logic level was controlled by the input voltage, V4. For both cases, the switching voltage waveform, V1, was a logic zero pulse of 100 microseconds duration with a 7.5 millisecond period. The waveforms presented on pages 10 through 13 were observed with L = 2.0 feet.

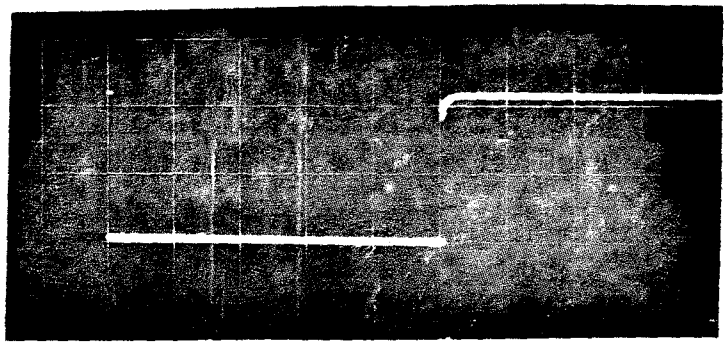
The amplitude of the most negative going crosstalk spike, from a logic one level, was recorded at V2 for various lengths of cable. The amplitude of the most positive going crosstalk from a logic zero level was recorded at V2 using the same cables. The results are presented graphically in Figures 7 and 8.

Figure 8 indicates that crosstalk to a logic zero level will be less than 0.4 volts between two parallel conductors with common routing of less than 30 inches. In comparison, Figure 7 indicates that crosstalk to a logic one level of 0.4 volts will occur with common routing of approximately 4 inches.

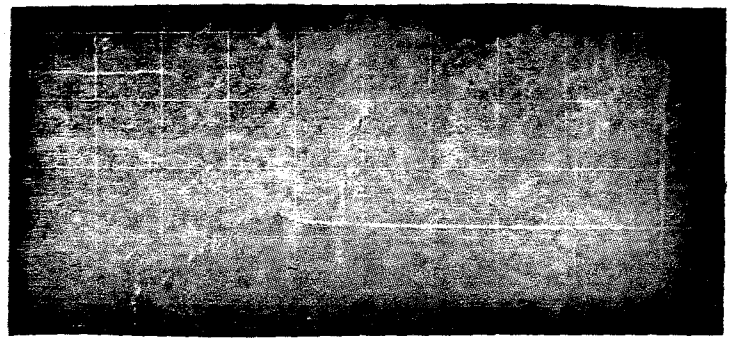
This data indicates that crosstalk to a logic one level is by far a more serious problem than crosstalk to a logic zero level.

The reason for the large difference in the amount of crosstalk for the two cases can be explained with the crosstalk model. The impedance to ground from the signal line which experiences the crosstalk, the V_{noise} line, is the impedance of a saturated transistor for the logic zero case.

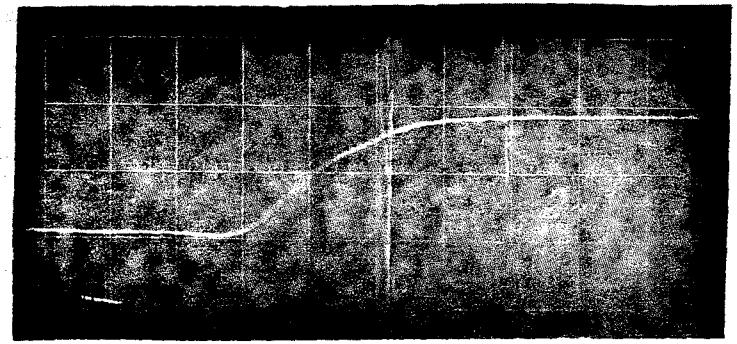
Switching Waveform, V1, With L = 2 Feet



V1: 20 Microseconds/Centimeter
2 Volts/Centimeter

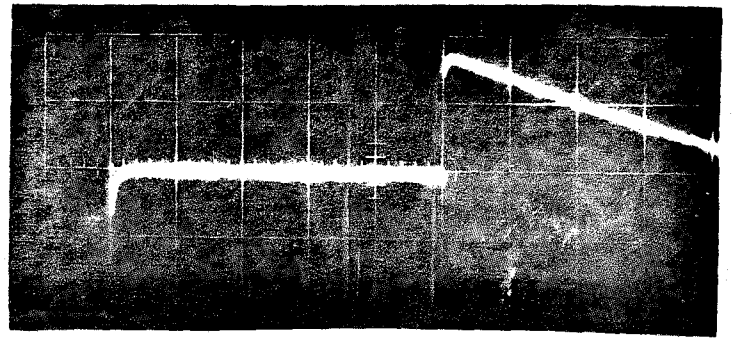


V1 Fall: 20 Nanoseconds/Centimeter
2 Volts/Centimeter



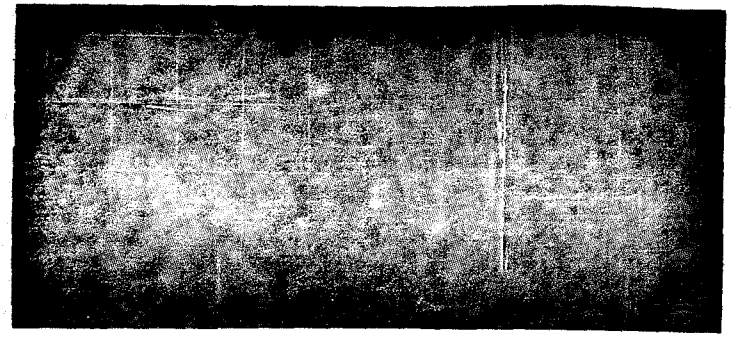
V1 Rise: 20 Nanoseconds/Centimeter
2 Volts/Centimeter

Crosstalk Waveform, V2, On Logic One With L = 2 Feet



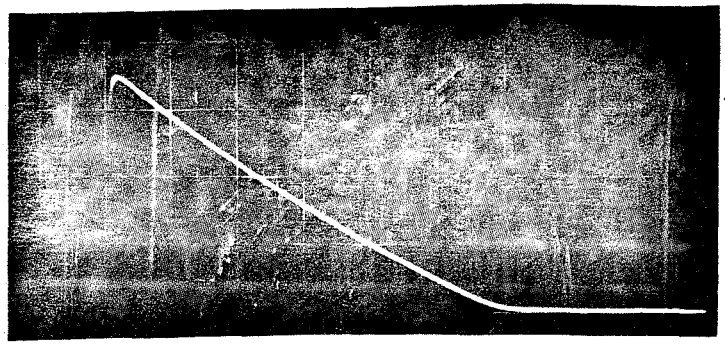
V2: 20 Microseconds/Centimeter
1 Volt/Centimeter

V2 Fall: 500 Nanoseconds/Centimeter
0.5 Volts/Centimeter

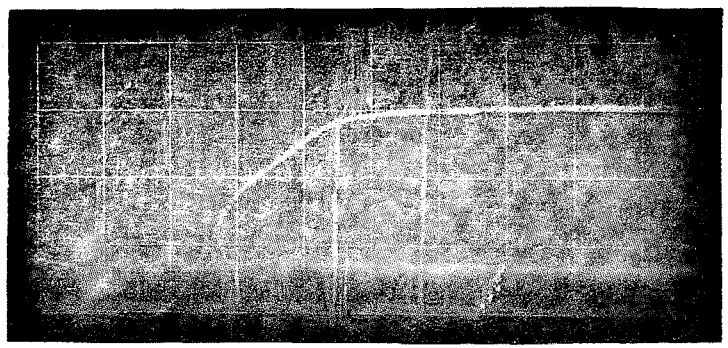


V2 Fall: 20 Nanoseconds/Centimeter
0.5 Volts/Centimeter

Crosstalk Waveform, V2, On Logic One With L = 2 Feet

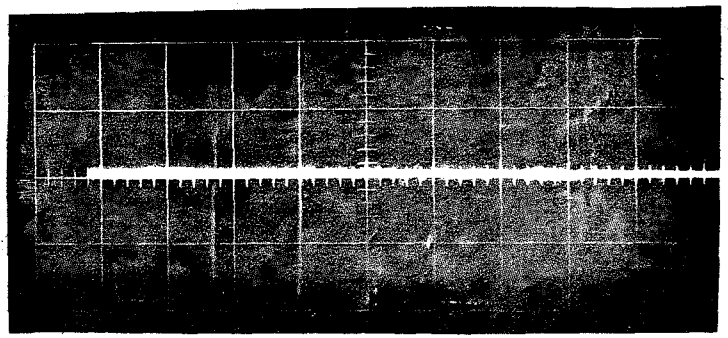


V2 Rise: 20 Microseconds/Centimeter
0.5 Volts/Centimeter

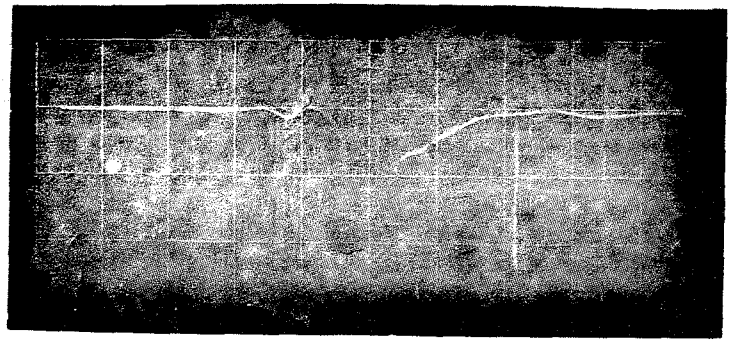


V2 Rise: 20 Nanoseconds/Centimeter
0.5 Volts/Centimeter

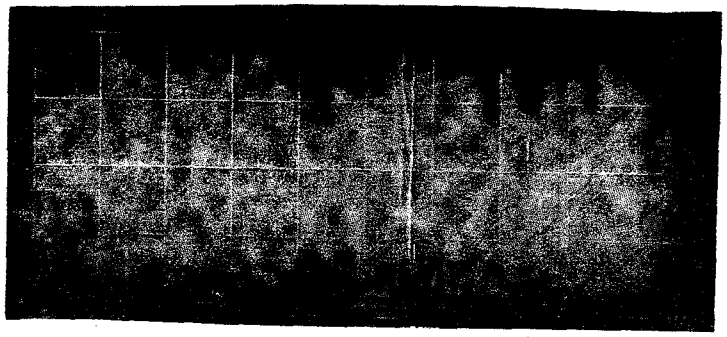
Crosstalk Waveform, V2, On Logic Zero With L = 2 Feet



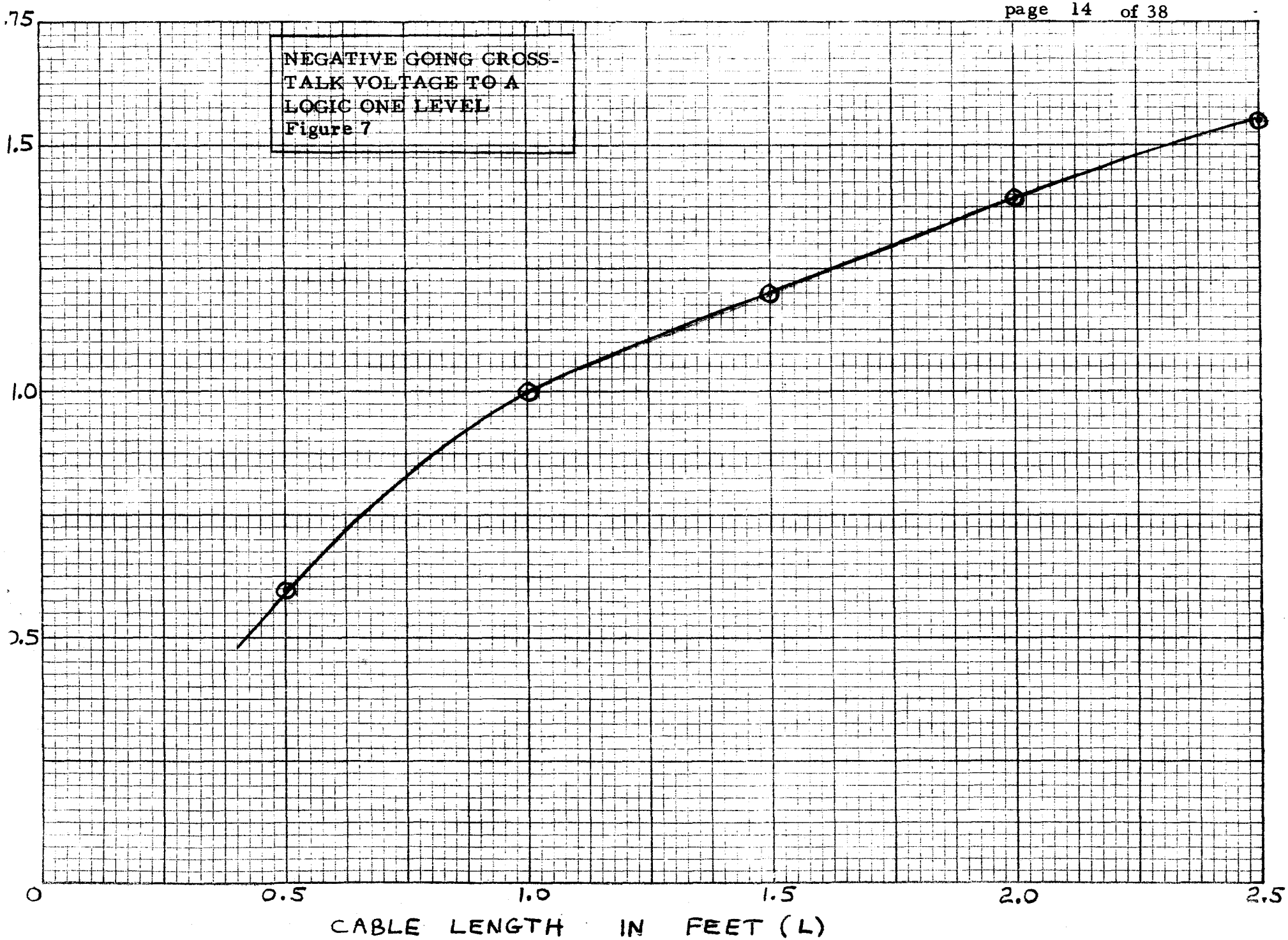
V2: 20 Microseconds/Centimeter
0.5 Volts/Centimeter

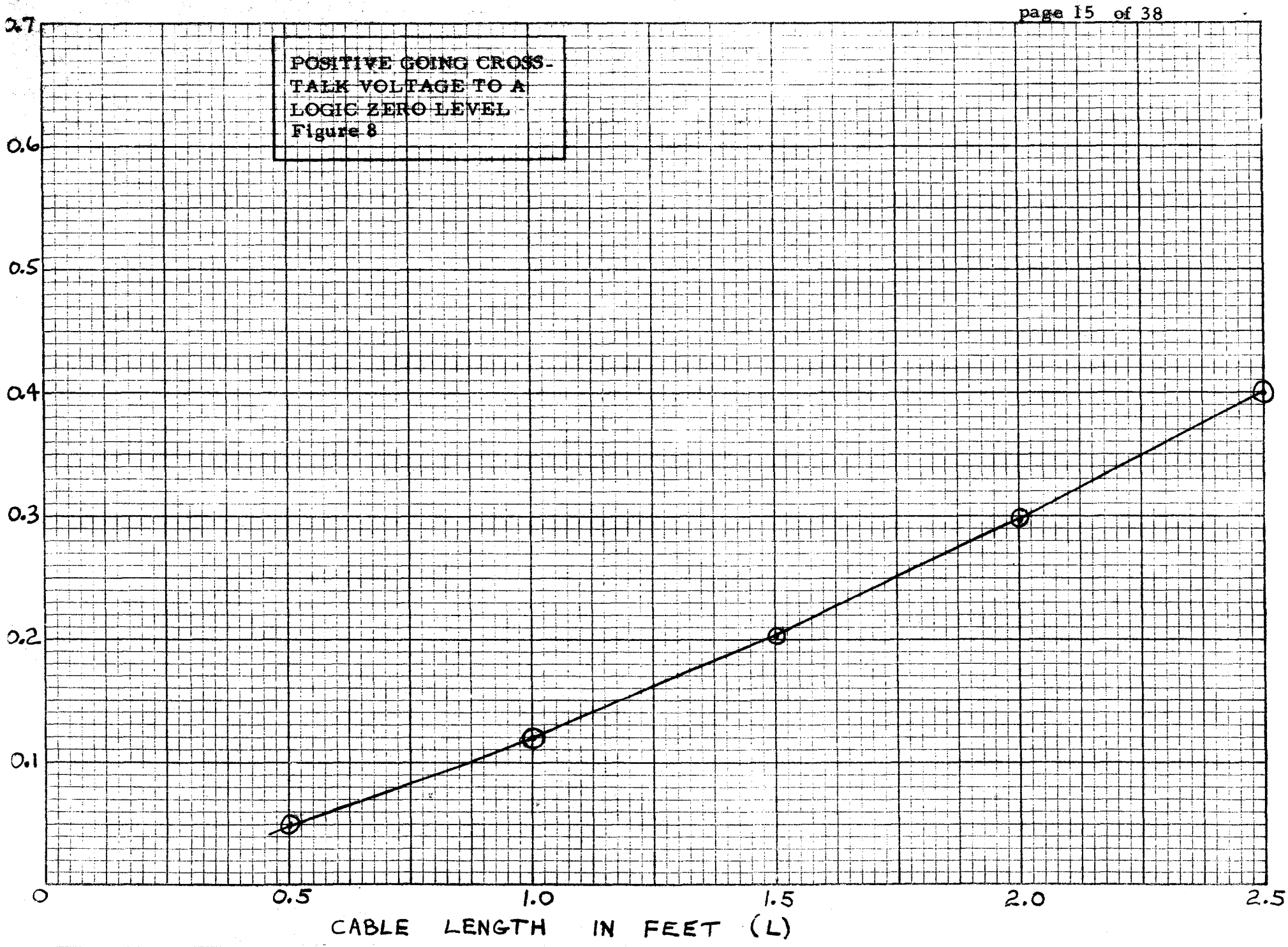


V2 Fall: 40 Nanoseconds/Centimeter
0.5 Volts/Centimeter



V2 Rise: 20 Nanoseconds/Centimeter
0.5 Volts/Centimeter





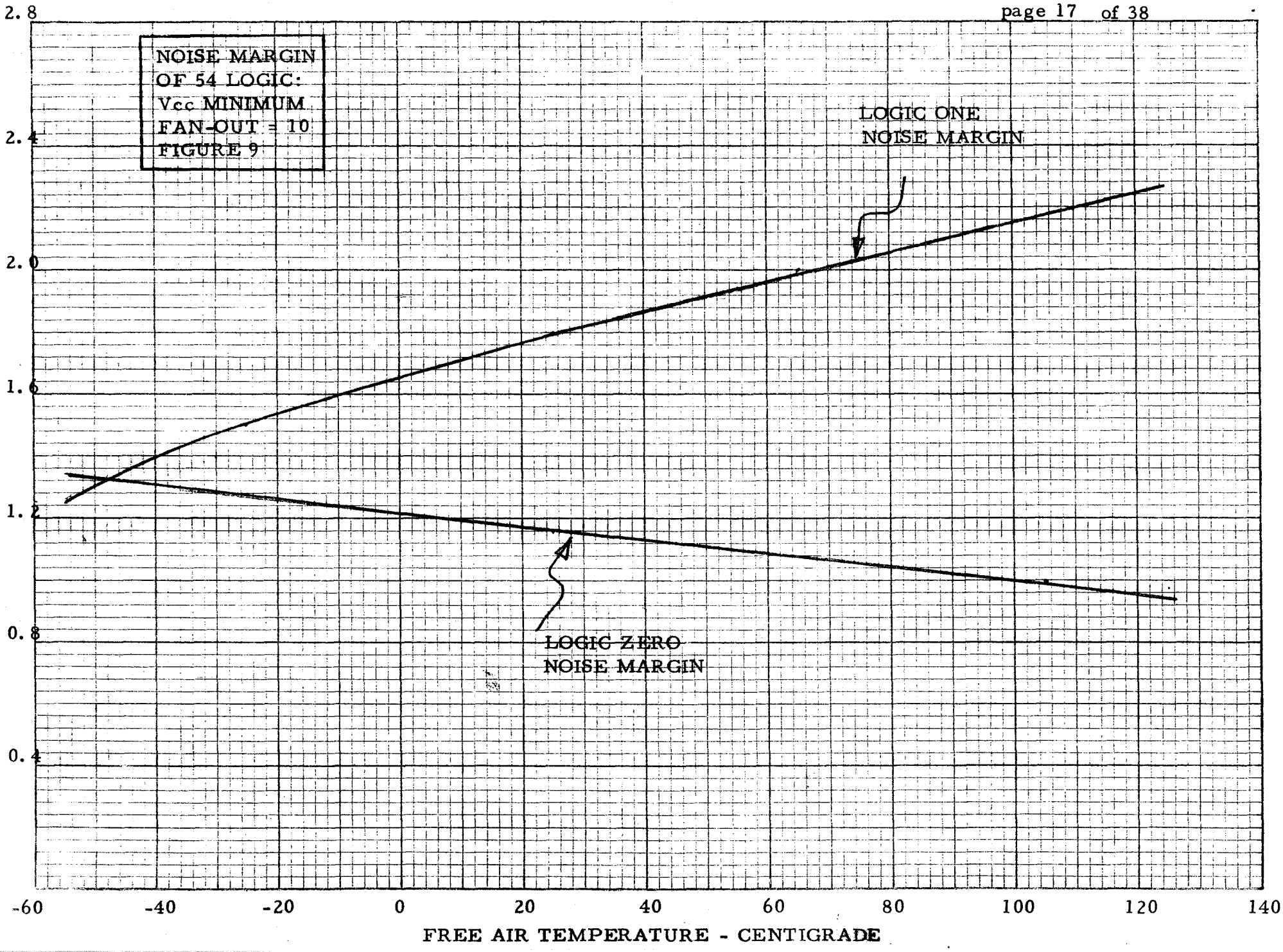
Due to the low impedance of the saturated transistor, large transient currents need to be impressed upon the V_{noise} line to generate substantial crosstalk voltage. Since large currents cannot be supplied by the noise source due to its internal impedance, crosstalk is effectively shorted to ground. The magnitude of the impedance to ground for the logic zero case is at least two orders of magnitude less than for the logic one case.

Examination of the equation for crosstalk amplitude, equation 2, indicates that the entire expression for crosstalk is multiplied by the value of the line resistance to ground, R. As the value of the resistance approaches zero, the amplitude of crosstalk approaches zero. Consequently, a large reduction in crosstalk is expected with a two order of magnitude reduction in resistance.

The noise immunity of the 54L logic elements will be determined and used in conjunction with the crosstalk data to develop design requirements which will eliminate all potential crosstalk problems. The logic manufacturers guaranty the noise immunity of the 54L logic series to be at least 400 millivolts over fan out conditions of one to ten, with power supply variation from 4.5 to 5.5 volts d.c., and over the temperature range of -55° to +125° centigrade. The logic in the Central Station will be used under less severe conditions, indicating that the noise immunity of the logic will be greater than 400 millivolts for this application.

The fan out of logic elements driving the wire harness will be limited to one, the power supply will be held between 4.6 to 5.4 volts, d. c., and the ambient temperature range will be -30° to +70° centigrade.

The noise immunity of the 54L logic when used in the Central Station will be developed by derating typical noise margin data supplied by Texas Instruments. The typical data will be derated the standard 50% to obtain a noise margin design limit. The graph of Figure 9 is a redrawing of Texas Instruments data for SN54 series logic elements under the worst case conditions of minimum supply voltage of 4.5 volt d.c. with ten loads on the gate. This data is presented on page XI of Texas Instruments Catalog CC201.



The typical noise margin for the logic zero level is minimum at high temperature. From the graph, the typical noise margin at 70°C is approximately 1.1 volts. Derating 50%, the noise margin design parameter is 0.55 volts. Comparing the 0.55 volt noise margin to the logic zero crosstalk data of Figure 8, it can be seen that the logic elements can drive a logic zero level well over 30 inches with no crosstalk degradation.

The noise margin data of Figure 9 indicates that the minimum logic one noise margin occurs at low temperature. At -30°C the typical noise margin is 1.4 volts. Derating 50% gives a design parameter of 0.7 volts for the logic one level. Comparing this with the crosstalk data of Figure 7, it can be seen that the 54L logic can drive a logic one level for slightly more than seven inches with no crosstalk interference.

The following wire harness design criteria were developed considering that a logic zero level can drive over thirty inches of cable and the logic one level can drive seven inches of cable with no crosstalk interference.

(1) A digital signal can be transmitted on AWG 24, unshielded wire for up to thirty inches if it is a logic one only when no other signals in the wire harness has a falling edge which could cause false triggering.

(2) Those signals which remain at a logic one when another signal in the wire harness switches to a logic zero are susceptible to crosstalk. The offending signal should be shielded if it is over 7 inches.

Since shielding in general reduces crosstalk by at least an order of magnitude, shielding of the wire harness allows effectively seven inches of unshielded wiring internal to the units driving and receiving the digital signal.

The interpath capacitance of parallel conductors on Central Station printed circuit boards is approximately 2 picofarads per foot. This is one-fourth of the coupling between number twenty-four harness wires. Consequently a logic one level should be capable of driving twenty-eight inches of printed circuit board wiring without crosstalk interference.

(3) Unshielded signal lines which are at a logic zero must be reduced in length by a factor equal to the number of signals with coincident rising edges in the vicinity of the signal line, if these edges occur at a time critical to the logic zero signal.

(4) Unshielded signal lines which are at a logic one must be reduced in length by a factor equal to the number of signals with coincident falling edges in the vicinity of the signal line, if these edges occur at a time critical to the logic one signal.

(5) Signals with coincident edges do not have to be shielded unless they also conform to one of the above categories.

These criteria were used to develop the table of Figure 10, which defines the wires requiring shields. Signals with rise and fall time control are not included in this table. These signals have crosstalk suppression which has been treated in other reports. The rise time controlled signals will be routed separately from non-controlled signals. It can be seen that the bulk of the signals in the wire harness are immune to crosstalk, the major crosstalk offenders being the commands.

Commands are asynchronous with the other signals in the wire harness. Consequently, the falling edge of a command may occur when any other signal is at a logic one. Therefore, the command signals over 7 inches will be shielded. The timing signals Data Gate, CWE, and Shift Clock may cause interference on signals between the Command Decoder and Data Processor; these three signals will be shielded. This shielding and the rise time control of signals interfacing with the experiments is the only crosstalk control required.

The following five techniques were considered as solutions to potential crosstalk problems.

1. Thick insulation, low capacitance wire.
2. Line filters.
3. Reduced logic one source impedance.
4. Reduced logic speed.
5. Shielding.

INTERFERRING SIGNAL	SIGNAL INTERFERRED WITH								
	Ninetieth Frame Mark	Even Frame	Frame	Commands	Demand	Data (NRZ)	Data Gate	CWE	Shift Clock
Ninetieth Frame Mark	X	X	X	S	X	X	X	O	O
Even Frame	O	X	X	S	X	X	X	O	O
Frame	O	O	X	S	X	X	X	O	O
Commands	S	S	S	S	S	S	S	S	S
Demand	O	O	O	S	X	O	X	O	O
Data (NRZ)	X	X	X	S	X	X	O	O	X
Data Gate	X	X	X	S	S*	X	X	O	O
CWE	O	O	O	S	S*	S*	O	O	S*
Shift Clock	O	O	O	S	S*	X	O	O	X

O - signal interferred with is a logic zero at critical times

S - problem - signal interferred with is at a logic one

X - coincident edges

* - shield signal conductor between Command Decoder and Data Processor only

Wire Harness Shielding

Figure 10

1 LOW CAPACITANCE WIRE

Crosstalk can be reduced by decreasing the interwire capacitance, as can be shown with the equation for V_{noise}, equation 2. The expression for interwire capacitance, equation 4, indicates that the capacitance can be reduced by either decreasing the dielectric constant, ϵ_r, decreasing the wire diameter, d, or by increasing the distance between wires, h.

The wire diameter is fixed due to mechanical strength considerations. The selection of dielectric material is constrained by physical properties such as thermal characteristics. The only parameter of equation 4 which is easily variable in this application is the interwire spacing h.

For the case under study, the interwire capacitance was calculated to be 16.0 picofarads/foot using equation 4, where d = 0.023 inches, ϵ_r = 2.1, and h = 0.035 inches.

If the interwire spacing is increased by a factor of 10, the interwire capacitance given by equation 4 decreases to 5.2 picorarads/foot. Note that increasing the interwire spacing by a factor of 10, to almost four tenths of an inch, reduces interwire capacitance by less than 70%. It can be concluded that increasing the interwire spacing to a reasonable distance, but much less than four tenths of an inch, will only slightly increase the allowable length of parallel wires in the wire harness.

2 LINE FILTERS

The use of line filters is effective in reducing crosstalk as has been shown in studies of the passive filters used in the Central Station/Experiments interfaces.

Line filters have the disadvantage of decreasing reliability, increasing weight, and increasing power dissipation.

3 REDUCED SOURCE IMPEDANCE

Reducing the impedance of a digital signal to ground is an effective method of reducing crosstalk as was found for the logic zero. The logic one level impedance to ground could be reduced with decoupling capacitors.

These capacitors would reduce voltage transients by coupling them to ground. A pull up resistor could be used instead of a capacitor if the driving gate were capable of sinking the extra logic zero current. These techniques are similar to line filtering and have the same disadvantages.

The use of lower output impedance logic elements, such as the medium power, 54 series logic, can increase logic one crosstalk immunity. These logic elements dissipate ten times as much power, however.

4 REDUCED LOGIC SPEED

Because the signal lines are capacitively coupled, the coupling impedance can be increased by eliminating the high frequency components of the signals. The highest frequencies generated by digital signals are produced by the sharp rising and falling edges of the pulses. The roll off frequency of these signals can be reduced by increasing the rise and fall times of the signals. This can be implemented by using slower logic. The difficulty with this approach lies with the fact that the only alternate logic types are less reliable, require more weight and volume, or have only one source. In particular, Diode Transistor Logic have slower rise times but the fall times are simular to the 54L series.

5 SHIELDING

Shielding of the signal lines is in general an effective technique of crosstalk suppression. A reduction in crosstalk of better than a factor of 10 can be expected when shields are used. Observations of the effects of shielding on this problem have verified this statement.

The use of shields increases weight and necessitates the added manufacturing process of grounding each of the shields. Adding shields only slightly reduces circuit reliability, if any, since the shields are not a functional component of the circuits.

Of the five suggested solutions, only shielding has a major effect on crosstalk with minimal effects on reliability and power dissipation. It is for this reason shielding has been recommended as the primary solution to possible wire harness crosstalk problems in the Central Station.

2.2 CENTRAL STATION GROUNDING

Another mechanism which can cause a logic element to misinterpret a logic level is transient voltages on the ground or supply lines. Transient currents can cause a voltage differential between the grounds or power sources of the logic driver and logic receiver at an interface. The base of the input transistor of a 54L logic element is the reference level for the logic element. This reference is coupled to ground through three forward biased PN junctions when the logic element is driven with a logic one. The low transient impedance of these foward biased junctions directly couples ground voltage transients to this reference voltage. An increase in the ground voltage increases the reference voltage. This is interpreted by the logic element as a corresponding decrease in the logic one level at its input.

The grounding technique that will be used in the Central Station-Array E will provide a low impedance path between the various units. Consequently only small ground voltage transients will be experienced. Low impedance between the grounds is achieved by using planer surfaces as current returns. This reduces the inductance of the returns and the impedance between ground points.

The following calculations are presented to give an indication of the magnitudes of the ground transients that will be experienced. First, calculations will be presented for a single, AWG gauge 18 wire ground return. These calculations will be used to compare with the grounding technique for Array E.

For these calculations, the impedance of the ground return will be assumed purely inductive. Since the mechanism to be studied is a current induced phenomenon, this model should be adequate. The magnitude of the impedance between two ground points separated by an inductance is given in Equation 5.

Equation 5: $$X_L = 2\pi fL$$

Where f is the frequency of ground current and L is the total inductance between the ground points under study.

The maximum frequency observed on the ground lines is determined by the rise and fall times of the logic elements; a major component of transient current will occur at these maximum frequencies. A fall time of thirty-five nanoseconds corresponds to approximately a ten megahertz roll off frequency. Higher frequencies may be observed on the ground lines due to the advertized faster switching times of the 54L logic elements produced by some suppliers. The grounding techniques will be compared at ten megahertz, however, due to the availability of inductance data at this frequency.

Using a precision bridge, the inductance of an AWG gauge 18, stranded wire was determined to be 180 nanohenrys per foot at ten megahertz. For these calculations, the distance between ground points will be chosen as two feet. The total inductance between grounds is therefore 360 nanohenrys.

The magnitude of the impedance between these points is 23 ohms as indicated below.

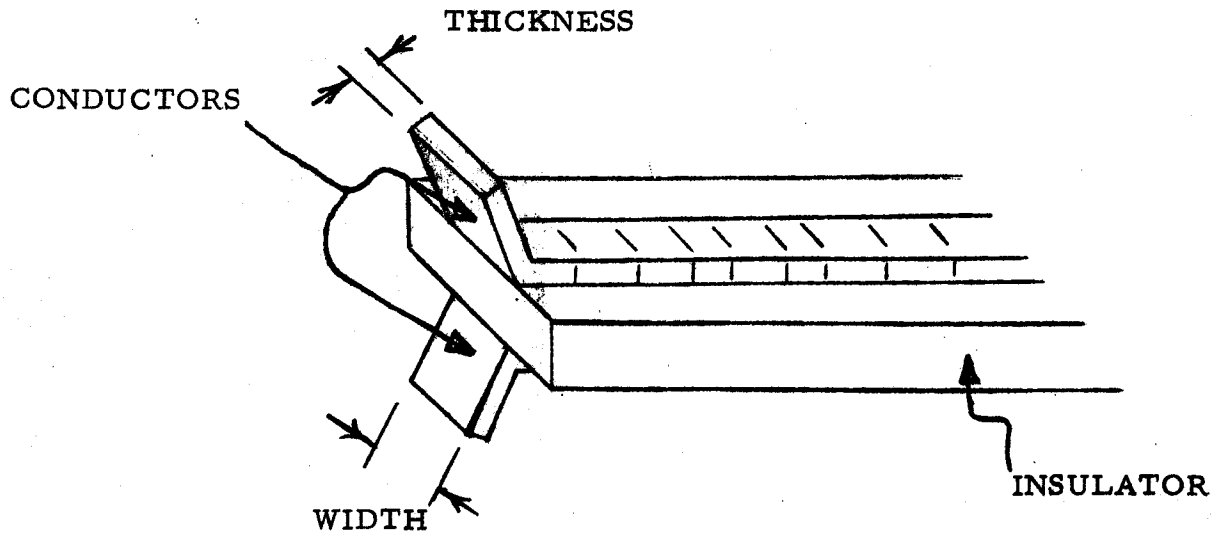
$$X_L = 2\pi fL = (6.28)(10^7)(3.6 \times 10^{-7}) = 23 \text{ OHMS},$$

for 18 gauge wire.

The grounding technique used in the Central Station - Array E will incorporate the thermal plate as a system ground plane. Each logic element in the Central Station will be grounded to a printed circuit board path with approximately one quarter of an inch width. This ground path is connected to the thermal plate by way of a clamp which fastens the card to the end of the unit. The end of the unit is electrically and thermally grounded to the Central Station thermal plate through the unit base plate.

With this grounding technique, the maximum inductance between the ground of any logic element in the Central Station and the thermal plate is the sum of the inductance of the printed wiring path and the inductance of the unit end and baseplate. The maximum inductance between the grounds of any two logic elements in the Central Station is twice this inductance, where the inductance of the system thermal plate is negligible. The inductance of the thermal plate is negligible compared to the rest of the ground path due to the large dimensions of this plane.

The inductance of the conductors shown in figure 11 were measured at ten megahertz using a Siemens-Halske precision bridge. The measured inductance of the 1.5 inch wide conductor is 4 nanohenrys per foot. The inductance of the 0.125 inch conductor is 20 nanohenrys per foot. These will be used as worst case parameters for the ground paths at the end of the unit and printed wiring paths respectively. The actual path widths will be approximately twice as wide, so the inductance used for these calculations is worst case (maximum).



NOTE: Measurements were made on two sets of conductors having the following dimensions.

Conductor Width-Inches	Conductor Thickness-Inches	Insulation Thickness-Inches
1.5	0.010	0.006
0.125	0.006	0.006

Path Inductance

Figure 11

The maximum printed path length between a circuit ground point and the edge of the printed wiring board is 0.25 feet. Using the empirical inductance data, this gives a path inductance of 5 nanohenrys. The maximum distance the ground current must flow through the end of the unit is 0.17 feet; this gives a path inductance of 0.7 nanohenrys.

The maximum inductance between the ground of a logic element and the thermal plate is therefore 5.7 nanohenrys, and the maximum inductance between the grounds of any two logic elements in the Central Station is 11.4 nanohenrys. Using equation 5, the maximum impedance between these ground points is 0.7 ohms.

$$X_L = 2\pi fL = (6.28)(10^7)(1.14 \times 10^{-8}) = 0.7 \text{ ohms}$$

This impedance compares most favorably to the 23 ohms of an 18 gauge wire.

The voltage drop across the 0.7 ohm ground connection will be calculated assuming a net of twenty-five worst case logic gates simultaneously switching from a logic one to a logic zero. For this condition, each logic gate input switches 190 microamperes, which gives a total switched current of 4.75 milliamperes for the twenty-five gates. Assuming all this current was at ten megahertz, the maximum voltage drop across distance grounds carrying this current in the Central Station would be as follows:

$$V = IX_L = (4.75 \times 10^{-3})(0.7) = 3.3 \times 10^{-3} \text{ volts}$$

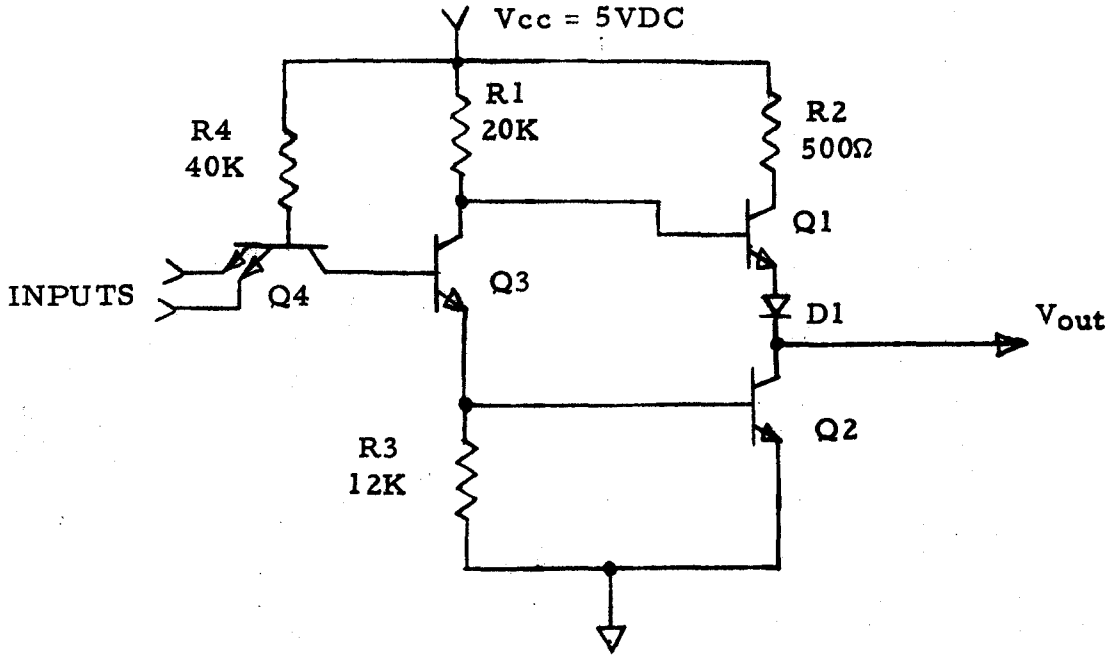
This three millivolt drop across the grounds will not affect the logic elements since they have a logic one noise margin of 700 millivolts.

Transients on the power supply lines can reduce the effective noise margin of the logic in a manner similar to ground noise. To keep the reactance of these lines small, the connectors in the Central Station have been arranged so that the cable lengths of the supply lines are maintained at a minimum. The power supply and ground paths on the printed wiring boards will have the maximum surface area possible to reduce the impedance to the power source. Decoupling capacitors are also employed at the loads to reduce voltage transients.

3.0 APPENDIX

3.1 OUTPUT IMPEDANCE OF 54L00 TTL LOGIC GATE (EQUATION 1)

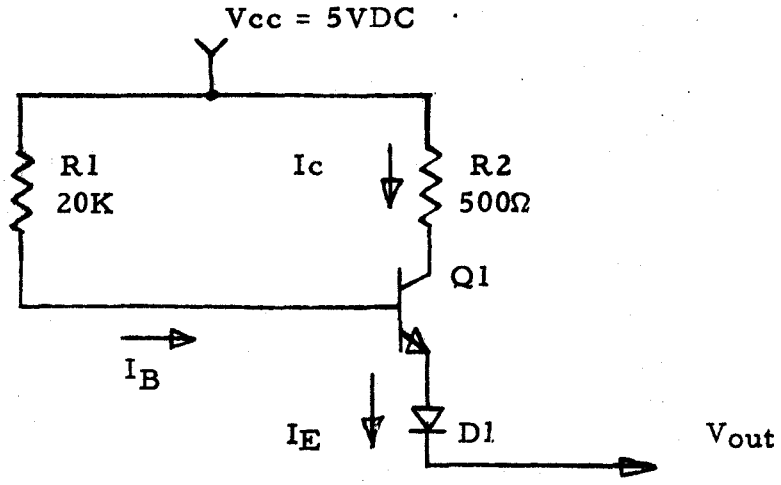
The following schematic represents one gate of an SN54L00 logic element as presented on page 4-4 of Texas Instrument's Catalog CC201.



54L00 Schematic

Figure 1A

With a logic one on the output, transistors Q2 and Q3 are turned off. Therefore, the equivalent output circuit driving a logic one has the form shown in Figure 2A.



54L00 Equivalent Output Circuit

Figure 2A

For Q1 to saturate,

$$H_{FE}\, I_B \geq I_{C\,(max)}$$

$$H_{FE} > \frac{I_{C\,(max)}}{I_B} \quad \text{for Q1 to saturate}$$

$$I_B = \frac{V_{CC} - V_{BE} - V_{Diode} - V_{out}}{R_1}$$

$$I_B \cong \frac{V_{CC} - 2\,V_{Diode} - V_{out}}{R_1}$$

$$I_{C\,(max)} = \frac{V_{CC} - V_{CE\,(sat)} - V_{Diode} - V_{out}}{R_2}$$

$$I_{C\,(max)} \cong \frac{V_{CC} - 2V_{Diode} - V_{out}}{R_2}$$

$$H_{FE} \geq \frac{\frac{V_{CC} - V_{out} - 2V_D}{R_2}}{\frac{V_{CC} - V_{out} - 2V_D}{R_1}}$$

$$H_{FE} \geq \frac{R_1}{R_2} \text{ for Q1 to saturate}$$

Therefore:

$$H_{FE} \geq \frac{2 \times 10^4}{5 \times 10^2} = 40 \text{ for Q1 to saturate}$$

Since H_{FE} is typically 20, Q1 is within its active region. Ignoring the A. C. impedance of diode D1 and the base to emitter junction of Q1, the output impedance of the driving logic element will be calculated. Note that all of the voltages and currents in the following equations represent transient conditions. The D. C. output impedance is of no concern since crosstalk is transientory.

Assuming Q1 is active:

$$I_B \cong \frac{V_{cc} - V_{out}}{R_1}$$

and

$$I_E = (h_{FE} + 1)\, I_B$$

$$Z_{out} = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{\Delta V_{out}}{\Delta I_E}$$

$$Z_{out} = \frac{\Delta V_{out}}{(h_{FE} + 1)\,\Delta I_B}$$

$$Z_{out} = \frac{\Delta V_{out}}{\frac{(h_{FE} + 1)\,(\Delta(V_{cc} - V_{out}))}{R_1}}$$

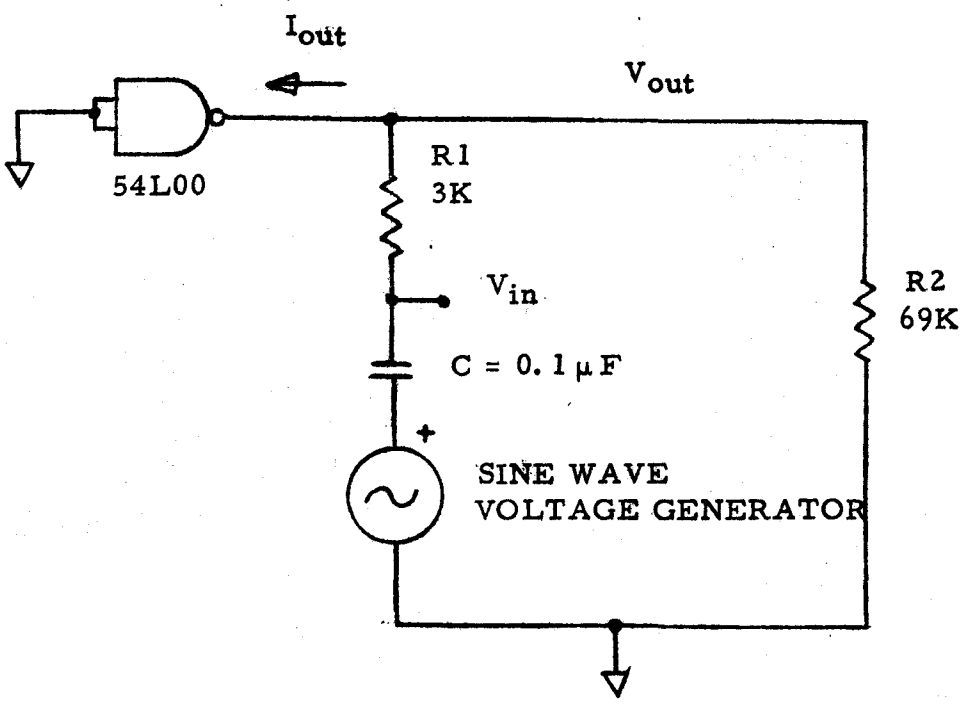
$$Z_{out} = \frac{R_1\,(\Delta V_{out})}{(h_{FE} + 1)\,(\Delta V_{out})}$$

$$Z_{out} = \frac{R_1}{(h_{FE} + 1)} \simeq \frac{R_1}{h_{FE}}$$

Note that the preceding equation for Z_{out} gives an output impedance which is purely resistive. For the typical values of $h_{fe} = 20$ and $R_1 = 20\ K\Omega$, the output impedance of the logic gate can be calculated as follows:

$$R_{out} = \frac{R_1}{H_{FE}} = \frac{20K}{20} = 1K\Omega$$

Two gates of one sample of an SN54L00N logic element were tested to verify the above results. The test circuit of figure 3A was used.



Output Impedance Test Circuit

Figure 3A

Resistor R2 was incorporated to bias the logic to an output current of approximately 50 microamperes. The sine wave signal generator was used to excite the logic element with a current waveform of less than 50 microamperes peak. The A. C. voltage at V_{in} and V_{out} were then measured. Knowing these voltages and the values of R_1 and R_2, the amplitude of the current waveform into the logic element can be calculated. By using the equation

$$Z_{out} = \frac{V_{out}}{I_{out}},$$

the amplitude of the output impedance of the logic element can be calculated.

With an excitation frequency of 10^6 Hertz, the A.C. current into the logic element was 4.1×10^{-5} amperes peak, while V_{out} was 5.0×10^{-2} volts.

$$Z_{out} = \frac{5.0 \times 10^{-2}}{4.1 \times 10^{-5}} = 1200\ \Omega \text{ at } 10^6 \text{ Hertz}$$

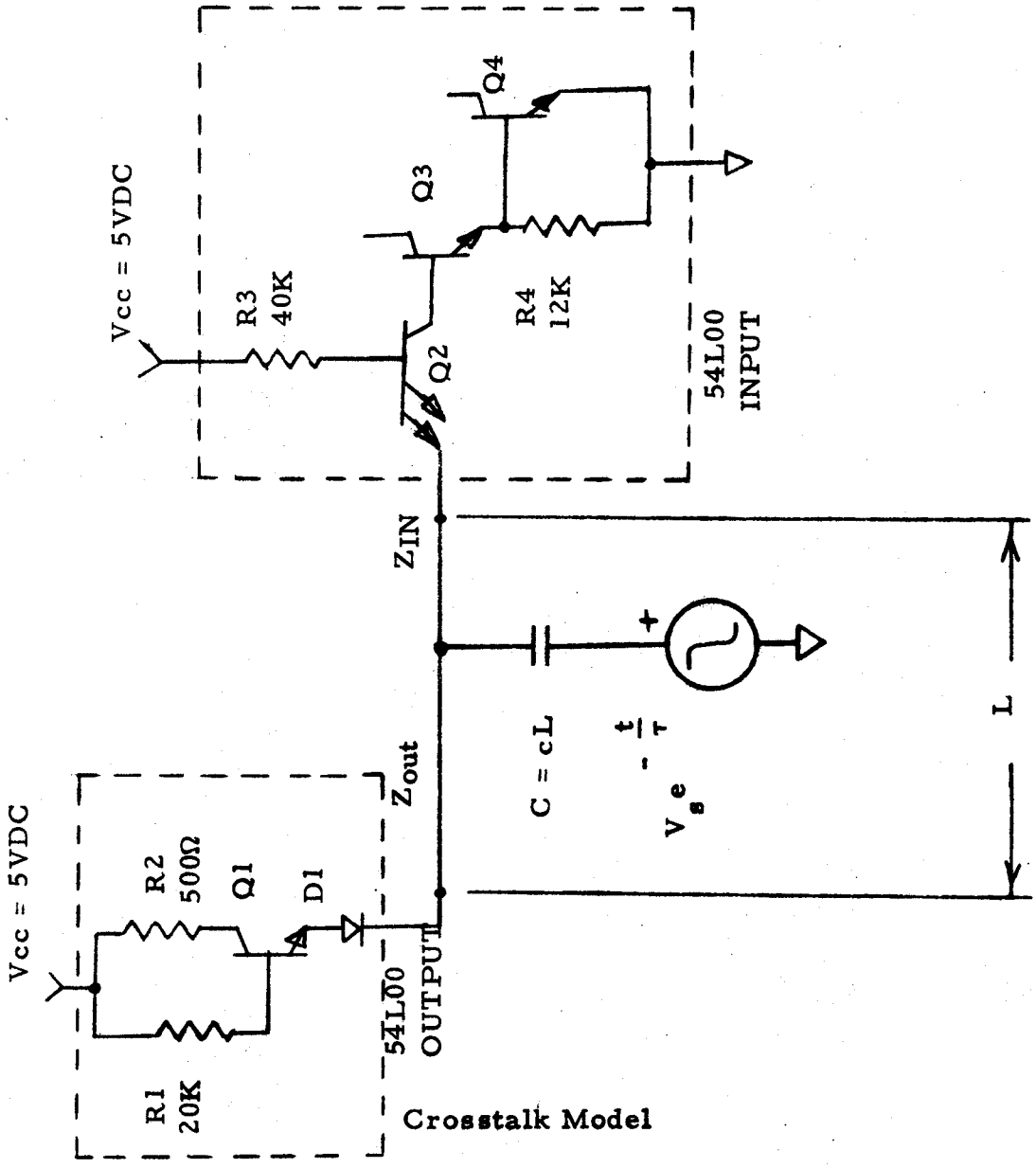
The same result was obtained with both gates tested.

3.2 CAPACITIVE CROSSTALK: V_{NOISE} (EQUATION 2)

Using the model of Figure 4A, the equation for V_{noise} will be developed, where L is the length of the adjacent conductors in feet, Z_{in} is the input impedance of the line receiver, and Z_{out} is the output impedance of the line driver. The model applies for crosstalk to a signal which is at a logic one from a digital signal which is falling from a logic one to a logic zero.

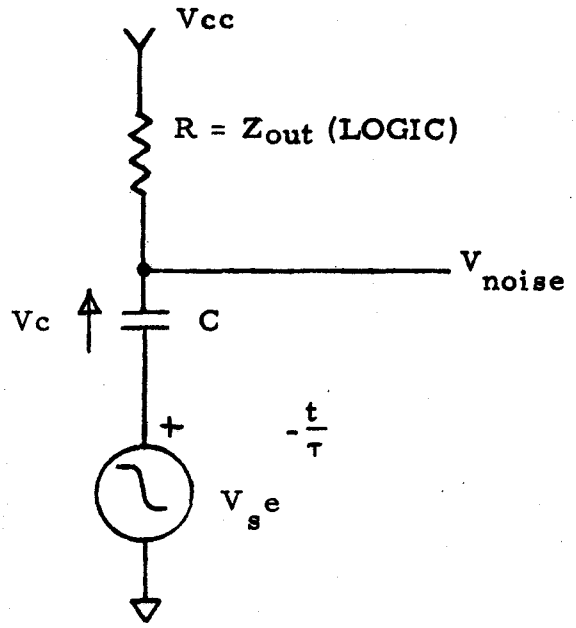
The signal generator, $V_s e^{-\frac{t}{\tau}}$, represents the switching waveform, C is the amount of capacitance coupling from the switching line to the V_{noise} line, and V_{noise} is the crosstalk superimposed on the logic one. The transistor circuits are the equivalent circuits for 54L00 logic elements driving and receiving logic one levels.

With a logic one level at the input of the line receiver, the base emitter junctions of transistor Q2 are reverse biased. Consequently, Z_{in} is large compared to Z_{out}. Because Z_{in} and Z_{out} are in parallel, the impedance from the V_{noise} conductor to ground is approximately equal to Z_{out}. As shown in Section 3.1, Z_{out} is resistive and equal to approximately 10^3 ohms. The circuitry on the V_{noise} line will be modeled with a resistor equal to Z_{out}, as shown in the simplified block diagram, Figure 5A.



Crosstalk Model

Figure 4A



Simplified Crosstalk Model

Figure 5A

The solution for V_{noise} will have the following form since the response is comprised of the forced and natural frequencies.

$$V_{noise} = V_1 e^{-\frac{t}{RC}} + V_2 e^{-\frac{t}{\tau}} + V_3$$

The solution for $\tau \neq RC$ follows:

at $t = 0$, $V_{noise} = 0$

at $t = \infty$, $V_{noise} = 0$

$$V_{noise}(\infty) = V_1 e^{-\infty} + V_2 e^{-\infty} + V_3$$

$$V_{noise}(\infty) = V_1 \cdot o + V_2 \cdot o + V_3 = 0$$

Therefore

$$V_3 = 0$$

$$V_{noise}(0) = V_1 e^{0} + V_2 e^{0} = 0$$

$$V_1 + V_2 = 0$$

$$V_2 = -V_1$$

Let

$$V = V_2$$

Then

$$V_{noise} = -Ve^{-\frac{t}{RC}} + Ve^{-\frac{t}{\tau}}$$

$$V_{noise} = V\left[e^{-\frac{t}{\tau}} - e^{-\frac{t}{RC}}\right]$$

Because the voltage across C cannot change instantaneously,

$$\frac{dV_c}{dt} = 0; \text{ at } t = 0$$

and

$$\frac{d\left[V_s e^{-\frac{t}{\tau}}\right]}{dt} = \frac{d\,V_{noise}}{dt}\ ;\ \text{at } t = 0$$

$$\frac{d\left[V_s e^{-\frac{t}{\tau}}\right]}{dt} = -\frac{V_s}{\tau} e^{-\frac{t}{\tau}}$$

$$\frac{d\left[V_s e^{-\frac{t}{\tau}}\right]}{dt} = -\frac{V_s}{\tau}\ ;\ \text{at } t = 0$$

$$\frac{d\left[V_{noise}\right]}{dt} = \frac{d\left[V\left(e^{-\frac{t}{\tau}} - e^{-\frac{t}{RC}}\right)\right]}{dt}$$

$$\frac{d\left[V_{noise}\right]}{dt} = -\frac{V}{\tau} e^{-\frac{t}{\tau}} + \frac{V}{RC} e^{-\frac{t}{RC}}$$

$$\text{at } t = 0,\ \frac{d\left[V_{noise}\right]}{dt} = -\frac{V}{\tau} + \frac{V}{RC}$$

Since

$$\frac{d\left[V_{noise}\right]}{dt} = \frac{d\left[V_s e^{-\frac{t}{\tau}}\right]}{dt};\ \text{at } t = 0$$

$$-\frac{V}{\tau} + \frac{V}{RC} = -\frac{V_s}{\tau}$$

$$V = \frac{RC\,V_s}{RC - \tau}$$

Therefore

$$V_{noise} = \frac{RC\,V_s}{RC - \tau}\left[e^{-\frac{t}{\tau}} - e^{-\frac{t}{RC}}\right]$$

For

$$\tau \neq RC$$

3.3 TIME WHEN MAXIMUM CROSSTALK OCCURS (EQUATION 3)

The maximum of the V_{noise} equation will be determined by differentiating it with respect to time and setting it equal to zero. The differentiated equation will then be solved for time.

$$\frac{d\left[V_{noise}\right]}{dt} = \left[\frac{RC\,V_s}{RC - \tau}\right]\left[-\frac{1}{\tau}e^{-\frac{t}{\tau}} + \frac{1}{RC}e^{-\frac{t}{RC}}\right] = 0$$

Since

$$\frac{RC\,V_s}{RC - \tau} \neq 0$$

$$-\frac{1}{\tau}e^{-\frac{t}{\tau}} + \frac{1}{RC}e^{-\frac{t}{RC}} = 0$$

$$-RC\,e^{-\frac{t}{\tau}} + \tau e^{-\frac{t}{RC}} = 0$$

$$\tau e^{-\frac{t}{RC}} = RC\,e^{-\frac{t}{\tau}}$$

$$\ln(\tau) - \frac{t}{RC} = \ln(RC) - \frac{t}{\tau}$$

$$t\left(\frac{1}{\tau} - \frac{1}{RC}\right) = \ln(RC) - \ln(\tau)$$

$$t = \frac{\ln(RC) - \ln(\tau)}{\frac{1}{\tau} - \frac{1}{RC}}$$

$$t = \frac{\tau\, RC \ln\left[\frac{RC}{\tau}\right]}{RC - \tau}\ ;\ \text{for maximum } V_{noise}$$