This ATM documents the Failure Modes, Effects and Criticality Analysis on the Digital Data Processor. The analysis reflects analysis on those parts which are presently planned to be used in final flight configuration.

This document is prepared in accordance with the requirements of Section 5.2 of the Reliability Program Plan for Array E, ALSEP-RA-08, Bendix document number BSR 3024 dated 11-30-70.

From the results of these analyses, it has been concluded that the reliability and design objectives have been fully satisfied.

Prepared by John G. Smith
John G. Smith
ALSEP Reliability Dept.

Prepared by S. J. Ellison
S. J. Ellison
ALSEP Reliability Manager

1.0 INTRODUCTION

The results of the Reliability Prediction and the Failure Mode, Effects and Criticality Analysis for ALSEP E. Digital Data Processor is documented in this report.

2.0 CIRCUIT DESCRIPTION

Figure 1 presents a Functional Block Diagram of the Digital Data Processor. The redundant circuits are in power standby.

2.1 TIMING AND CONTROL WORD GENERATOR

The timing pulses for the Data Processor are generated in this module. The three control words are also generated in this module.

2.2 DEMAND MATRIX

The Demand Matrix generates the commands for each experiment and collects the data from each experiment and sends that data to the modulator.

2.3 INTERFACE BOARD

The Interface Board takes the Demand Matrix Commands and buffers the Data Demand Lines to the experiments.

3.0 RELIABILITY PREDICTION

The reliability goal for the Digital Data Processor in standby redundant configuration is .996. The reliability prediction for the Digital Data Processor with standby redundancy is .99828 for processing all experiment data. The reliability prediction for the processing all experiment data except for one experiment is .99953. This reliability is based on a time span covering launch, deployment and two years of lunar operation.

3.0 Figure 2 defines the Digital Data Reliability Block Diagram. Two identical channels are represented by "X" in operation and "Y" in standby redundancy. The non-redundant blocks to each of the experiments consist of filter resistors and capacitors on data demand lines and filter capacitors on data lines from each experiment.

The probability of failure for each block identified in figure 2 is tabulated in Table I. The probability of failure shown represents the composite totals derived from the parts application stress ratios of each electronic piece part modified by the failure mode apportionment.

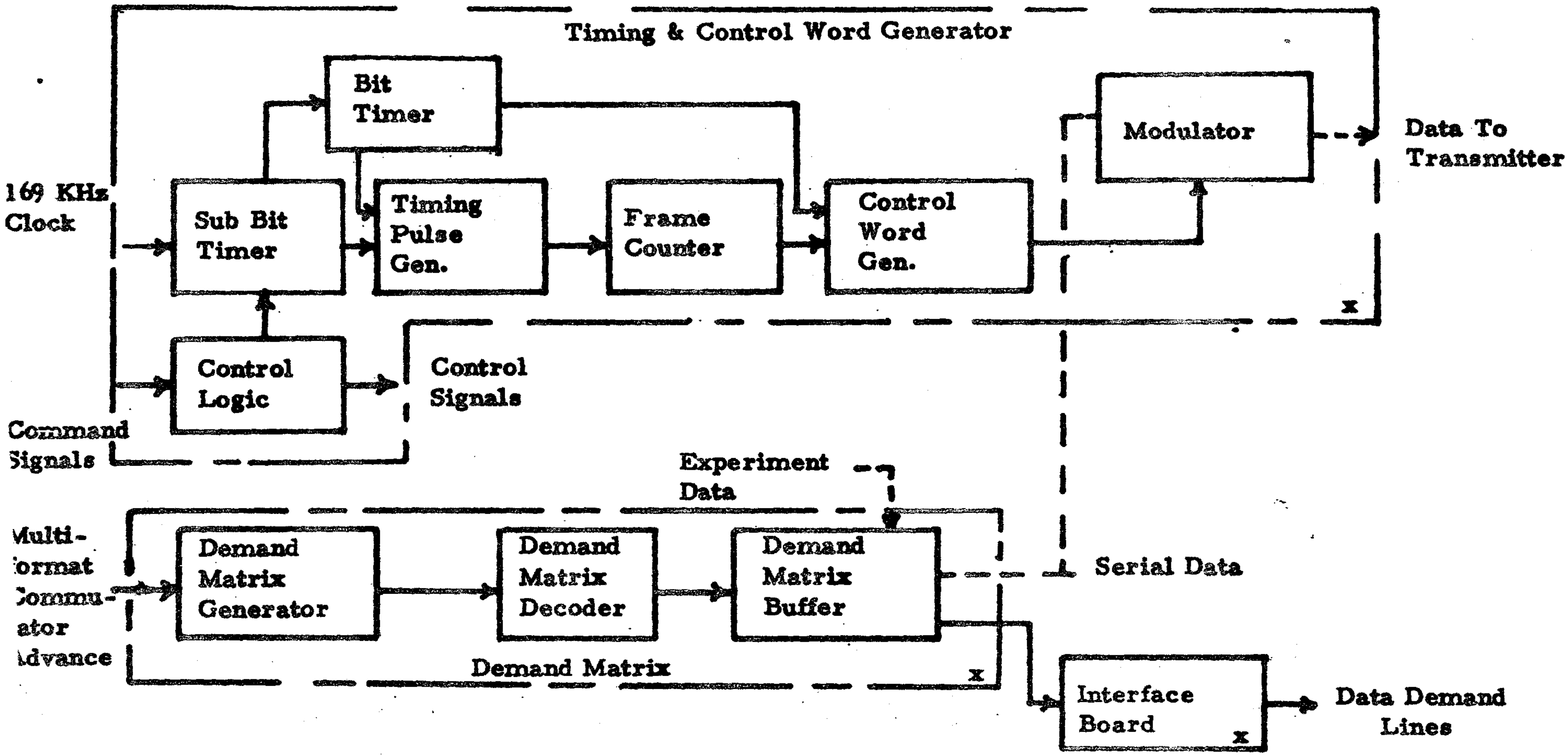

Figure 1 Digital Data Processor Functional Block Diagram

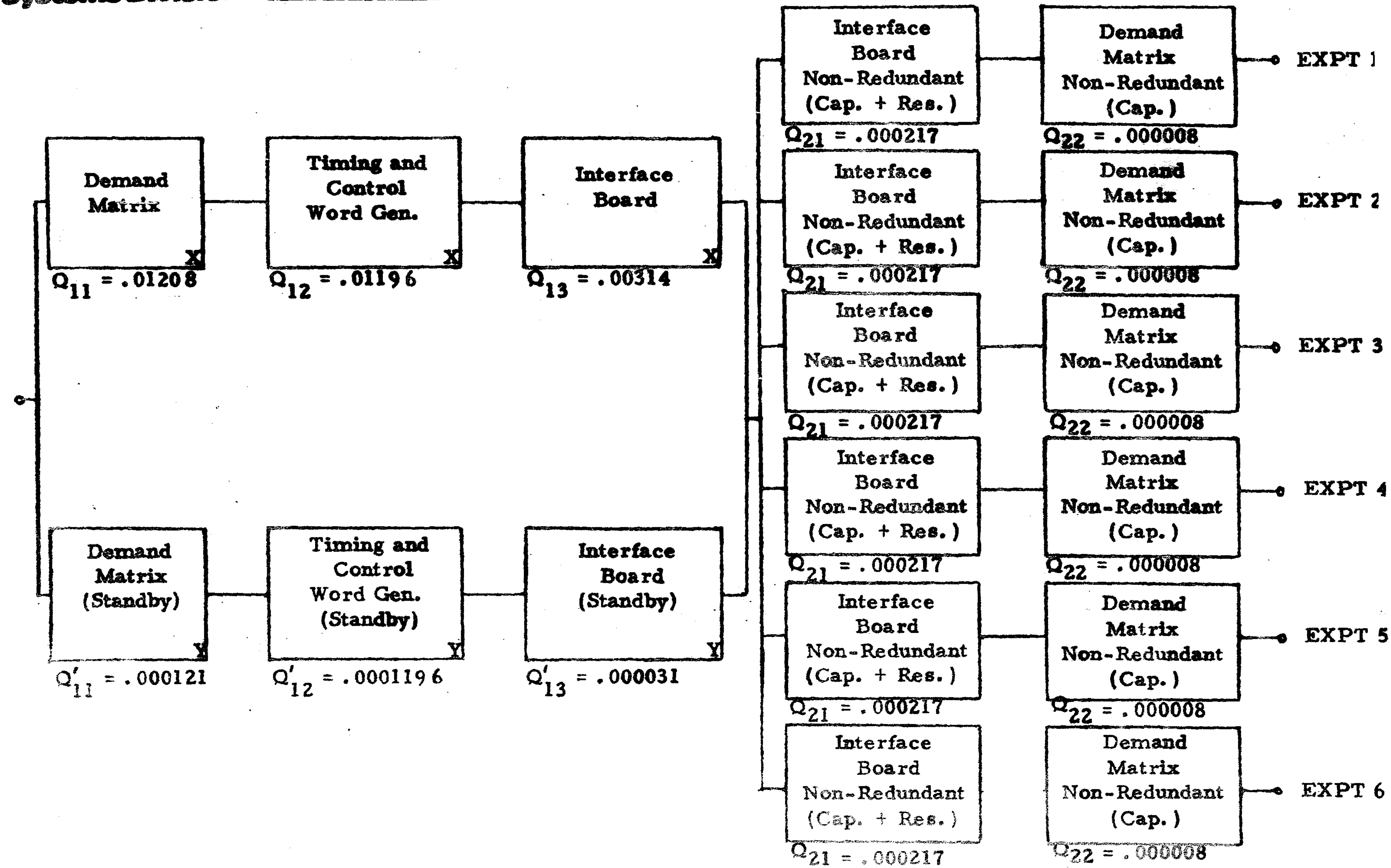

Figure 2 Digital Data Processor Reliability Block Diagram

TABLE I

PROBABILITY OF FAILURE SUMMARY

ASSEMBLY	Q OPERATING	Q^1 STANDBY
X - Demand Matrix	.01208	.000121
X - Timing & Control Word Generator	.01196	.000120
X - Interface Board	.00314	.000031
Interface Board Non-Redundant	.000217	———
Demand Matrix Non-Redundant	.000008	———

* Y-functions have same Q as X-functions

3.1 RELIABILITY CALCULATIONS

3.1.1 Q_T = probability of failure of processing all experimental data

$Q_1 = Q_{11} + Q_{12} + Q_{13}$ $\qquad$ $Q_2 = Q_{21} + Q_{22}$

$Q_1^1 = Q_{11}^1 + Q_{12}^1 + Q_{13}^1$

$$Q_T = \frac{Q_1 Q_1'}{2} + \frac{Q_1 Q_1}{2} + 6\, Q_2$$

$$Q_T = \frac{1.01\, Q_1^2}{2} + 6Q_2$$

$R_T = 1 - Q_T =$ reliability of processing all experimental data

3.1.2 Q_s = probability of failure of processing all experimental data except for one experiment.

$Q_2 = Q_{21} + Q_{22}$ $\qquad$ $R_2 = 1 - Q_2$

$$Q_s = \frac{Q_1\, Q_1^1}{2} + \frac{Q_1\, Q_1}{2} + \left[1 - R_2^6 + 6\, R_2^5\, Q_2\right]$$

$$Q_s = \frac{1.01\, Q_1^2}{2} + \left[1 - R_2^6 + 6\, R_2^5\, Q\right]$$

$R_s = 1 - Q_s$ = reliability of success of processing all experimental data except for one experiment.

3.1.3 $Q_1 = Q_{11} + Q_{12} + Q_{13} = .01210 + .01182 + .00314$

$Q_1 = .02706$

$Q_2 = Q_{21} + Q_{22} = .000217 + .000008$

$Q_2 = .000225$

$$Q_T = \frac{1.01 Q_1^2}{2} + 6Q_2$$

$$Q_T = 0.5\ (.0271\ 8)^2 + 6\ (.000225)$$

$$Q_T = .000369\ 0\ 0 + .001350$$

$$Q_T = .001719$$

$$R_T = 1 - Q_T = 1 - .001719$$

$R_T = .998284$ reliability of processing all experiment data

3.1.4 $$Q_S = \frac{1.01 Q_1^2}{2} + [\ 1 - R_2^6 + 6 R_2^5\ Q_2]$$

$$Q_S = 0.5\ (.0271\ 8)^2 + [\ 1 - (.999775)^6 + 6\ (.999775)^5\ (.000225)]$$

$$Q_S = .000369 + [\ 1 - .998551 + 6\ (.998775)(.000225)]$$

$$Q_S = .000369 + [\ 1 - .998551 + .0013497]$$

$$Q_S = .000369\ [\ 1 - .999901]$$

$$Q_S = .000369 + .000099$$

$$Q_S = .000468$$

$$R_S = 1 - Q_S = 1 - .000468$$

$R_S = .999532$ reliability of processing all experiment data except for one experiment.

4.0 FAILURE MODES, EFFECTS & CRITICALITY ANALYSIS

The failure mode and effects analysis for the Digital Data Processor is documented in Table II. Table II delineates the failure modes at the piece part level.

The failure probabilities reflect the identified line item. The format of Table II is designed to provide the reader with a narrative description of the varying types of failure that could occur, combined with the resultant performance characteristics. This information is useful to system support in performing fault isolation should any anomaly occur. There are no ALSEP E single point failures with the Digital Data Processor, but each experiment has a critical failure mode in the filter capacitor on each data line and the filter capacitor and resistor on each data demand line. This means that we can lose the ability to process data from an experiment and still process data on the other experiments.

The failure probability figures were derived using the data obtained in Table II. ATM 605A was used to derive the component α's (open, short, drift, etc. apportionment). Some failure modes, such as drift of a resistor in a digital circuit, do not affect the operation. The failure modes which do not affect the operation are not included in the FMECA. For this reason, the sume of α's for some circuit/function items do not equal one.

Not all failure modes are serious. When the effect of failure on the system is termed "output slightly erroneous ', the digital value received on the ground can be adjusted to the correct value. This can be done by observing how the failure or drift has affected the calibration signals.

The Digital Data Processor circuits are ranked according to criticality ranking which rates the effect on mission success. The higher the criticality ranking number the lesser the effect on mission success.

Criticality Ranking

I Loss of system

II Loss of system control

III Loss of one experiment

Criticality Ranking (Cont.)

IV Loss of housekeeping channel

V Loss of redundant element

VI Degradation of a redundant element

5.0 RELIABILITY ASSESSMENT

The purpose of performing a reliability prediction and failure mode analysis is to identify inherent design weaknesses. From the results of these analyses, it has been concluded the reliability and design objectives have been fully satisfied.

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS (TTL)

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
1.0 Demand Matrix 1.1 C1 - C8 C17 - C21	1.1 A) C1-C8, C16-C21 Fail Short B) C1-C8, C16-C21 Fail Drift	1.1 A) Increase 5V supply capacitance B) Increase or decrease in 5V capacitance	1.1 A) Increases 5V supply filtering which helps system limit noise B) Not much effect on system	11.4	VI
1.2 Command Advance Register U1	1.2 A) FF U1A Fails — $Q\ \bar{Q}$: 0 1; 0 0 B) FF U1A Fails — $Q\ \bar{Q}$: 1 1; 1 0 C) FF U1B Fails — $Q\ \bar{Q}$: 0 1; 0 0; 1 0; 1 1	1.2 A) Command advance register's bits A, B, C, D, E, F stop changing B) Command advance register's bits B, C, D, E, F continues to count C) Command advance register's bits B, C, D, E, F stop changing	1.2 A) Data demand line command stay at the same word B) Data demand line command, commands wrong word and causes 32 words to repeat C) Data demand line command alternates between two words	29.8	VI
1.3 U2	1.3 A) U2A Fails — $Q\ \bar{Q}$: 1 0; 1 1 B) U2A Fails — $Q\ \bar{Q}$: 0 1; 0 0 C) U2B Fails — $Q\ \bar{Q}$: 1 0; 1 1; 0 0; 0 1	1.3 A) Command advance register's bits A, B, D, E, F continue to count B) Command advance register's bits C, D, E, F stop changing C) Command advance register's bits D, E, F stop changing	1.3 A) Data demand line command commands wrong word and causes a different set of 32 words to repeat B) Data demand line commands causes 4 words to repeat in serial fashion C) Data demand line command causes 8 words to repeat in serial fashion	29.8	VI

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS (TTL)

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁵	CRITICALITY
1.4 Command Advance Register U3	1.4 A) U3A Fails Q Q̄: 1 0; 1 1 B) U3A Fails Q Q̄: 0 1; 0 0 C) U3B Fails Q Q̄: 1 0; 0 1; 1 1; 0 0	1.4 A) Command advance register's bits A, B, C, D, F continue to count B) Command advance register's bit E, F stop changing C) Bit F stops changing	1.4 A) Data demand line command commands wrong word and causes a different set of 32 words to repeat B) Data demand line command causes 16 words to repeat in serial fashion C) Data demand line command causes 32 words to repeat in serial fashion	29.8	VI
1.5 U4 U5 U6 U7 U39 U8 U9 U10 U11	1.5 A) U4A Fails High U7A Fails Low B) U4A Fails Low U7A Fails High NOTE: 1.5 is repeated 15 times for other 15 coded outputs from command generator	1.5 A) Demand matrix decoder will not decode 8 of 64 words B) Demand matrix decoder will cause 2 words to be commanded on at the same time and this will happen 8 times out of 64 words	1.5 A) Data demand line commands will be missing 8 words per frame B) Data demand line commands will cause 2 words to be commanded on at the same time and this will happen 8 times out of 64 words	A) 228.9 B)	VI
1.6 R1	1.6 A) R1 Fails Open B) R1 Fails Drift	1.6 A) Command advance register's A, B, C, D stop counting E, F B) Command advance register's might count erratically	1.6 A) Data demand line command stay at same word B) Data demand line command might command wrong word	6.0	VI
1.7 R18	1.7 A) R18 Fails Open	1.7 A) Command advance register's E, F stop counting	1.7 A) Data demand line command will cause 16 words to repeat in serial fashion	6.0	VI

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q × 10⁵	CRITICALITY
2. Demand Matrix Decoder				28	VI
2.1 U20	2.1 A) U20A Fails High	2.1 A) Decoder nand pin 3 stay in 1-state	2.1 A) First word command stays at one state or first word off position for all commands		
	B) U20A Fails Low	B) Decoder nand pin 3 stay in 0-state	B) First word command stays at zero state or first word on position for all commands		
	C) U20B Fails High	C) Decoder nand pin 14 stay in 1-state	C) Second word command stays in second word off position for all commands		
	D) U20B Fails Low	D) Decoder nand pin 14 stay in 0-state	D) Second word command stays in second word on position		
	E) U20C Fails High	E) Decoder nand pin 8 stay in 1-state	E) Third word command stays in third word off state for all commands		
	F) U20C Fails Low	F) Decoder nand pin 8 stay in 0-state	F) Third word command stays in third word on state for all commands		
	G) U20D Fails High	G) Decoder nand pin 5 stay in 1-state	G) N/C		
	H) U20D Fails Low	H) Decoder nand pin 5 stay in 0-state	H) N/C		
2.2 U12	2.2 A) U12A Fails High	2.2 A) Decoder wired or pin 8 stays in 1-state	2.2 A) 57 word stays in off condition	28	VI
	B) U12A Fails Low	B) Decoder wired or pin 8 stays in 0-state	B) 57 word stays in on condition		
	C) U12B Fails High	C) Decoder wired or pin 3 stays in 1-state	C) 58 word stays in off condition		
	D) U12B Fails Low	D) Decoder wired or pin 3 stays in 0-state	D) 58 word stays in on condition		

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^5$	CRITICALITY
2.2 U12	2.2 E) U12C Fails High	2.2 E) Decoder wired or pin 5 stays in 1-state	2.2 E) 60 word command stays in off condition for all commands		
	F) U12C Fails Low	F) Decoder wired or pin 5 stays in 0-state	F) 60 word command stays in on condition for all commands		
	G) U12D Fails High	G) Decoder wired or pin 14 stays in 1-state	G) 61 word command stays in off condition for all commands		
	H) U12D Fails Low	H) Decoder wired or pin 14 stays in 0-state	H) 61 word command stays in on condition for all commands		
2.3 U13 U24 U23 U14 U21 U15 U25 U16 U22 U17 U26 U18 U27 U19 U28	2.3 U13-U19 Same condition as U12 U21-U28 Same condition as U12	2.3 Same condition as U12 except different word	2.3 Words 4-56, 59, 62-64 are effected same as word 57	392.4	VI
2.4 U8C	2.4 A) U8C Fails High	2.4 A) Nand gate pins fails in high condition	2.4 A) 64 word cannot be commanded on	6.8	VI
	B) U8C Fails Low	B) Nand gate pin 5 fails in low condition	B) 64 word command stay on all time		
3. Demand Buffer					
3.1 U30	3.1 A) U30A Fail Q Q̄ = 0 1	3.1 A) U30A experiment I is commanded on	3.1 A) (DDIZP) Data demand line commanded on and data flows out (SIDYN)	29.8	VI
	B) U30A Fail Q Q̄ = 1 0	B) U30A experiment I is commanded off	B) (DDIZP) Data demand line commanded off and data stops flowing out (SIDYN)		
	C) U30A Fail Q Q̄ = 1 1	C) Experiment I turns I-data demand line off and I data line on	C) (DDIZP) Data demand line commanded off, but I data line is turned on to SIDYN		

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

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PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q × 10⁵	CRITICALITY
3.1 U30	3.1 D) U30A Fail $\frac{Q\ \bar{Q}}{0\ 0}$ E) U30B E) through H) fails same as 3.1 A) through D) F) G) H)	3.1 D) Experiment I turns I data demand line on and I data line off	3.1 D) (DDIZP) data demand line commanded on, but I data line is turned off to (SIDYN) E) (DDBYN) fails same as 3.1 A) through D) F) G) H)		
3.2 U33	3.2 A) U33A A) through D) fails same as 3.1 A) through D) B) C) D) E) U33B E) through H) fails same as 3.1 A) through D) F) G) H)	3.2	3.2 A) (DDHYN) fails same as 3.1 A) through D) B) C) D) E) (DDEYN) fails same as 3.1 A) through D) F) G) H)	29.8	VI

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE		FAILURE PROBABILITY Q x 10⁵	CRITICALITY
		ASSEMBLY	END ITEM		
3.3 U34	3.3 A) U34A A) through D) fails same as 3.1 A) through D) B) C) D) E) U34 E) through G) fails same as 3.1 A) through D) F) G) H)	3.3 A)	3.3 A) (DDGYN) fails same as 3.1 A) through D) B) C) D) E) (DDAYP) fails same as 3.1 A) through D) F) G) H)	29.8	VI
3.4 U35	3.4 A) U35A A) through D) fails same as 3.1 A) through D) B) C) D) E) U35B E) through D) fails same as 3.1 A) through D) G) H)	3.4 A)	3.4 A) (DDFYN) fails same as 3.1 A) through D) B) C) D) E) (DDDYN) fails same as 3.1 A) through D) G) H)	29.8	VI
3.5 U36 U37 U38	3.5 A) U36A Fails High Low B) U37A Fails High Low C) U36B Fails High Low	3.5 A) U36A Block I expt. data B) U37A Block H expt. data C) U36B block G expt. data	3.5 A) Command decoder data fails B) H expt. data fails C) G expt. data fails	68.9	VI

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PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^5$	CRITICALITY
	D) U37B Fails High Low	D) U37B block F expt. data	D) F expt. data fails		
	E) U37C Fails High Low	E) U37C block A expt. data	E) Housekeeping data fails		
	F) U36C Fails High Low	F) U36C block E expt. data	F) E expt data fails		
	G) U37D Fails High Low	G) U37D block D expt. data	G) D expt data fails		
	H) U36D Fails High Low	H) U36D block B expt. data	H) B expt data fails		
	I) U38 Fails High Low U7F Fails High Low	I) Block all data	I) (SIDTN) data is completely lost		
3.6 U29 U31D	3.6 A) U29 Fails High U31D Fails Low	3.6 A) FF U30B expt. B is commanded on	3.6 A) (DDBYN) data demand line is on and data flows out of (SIDYN) no matter what data demand line is on	35	VI
	B) U29 Fails Low U31D Fails High	B) FF U30B expt. B is commanded off	B) (DDBYN) data demand line is off and no data flows from expt. B		
3.7 R10 R11 R12 R13 R14 R15	3.7 A) R10 Fails Open-Drift	3.7 A) FF U30B expt. B is commanded on	3.7 A) (DDBYN) data demand line is on and data demand line cannot be turned off	35.7	VI
	B) R11 Fails Open-Drift	B) FF U30B expt. B is commanded on	↓		
	C) R12 Fails Open-Drift	C) FF U30B expt. B is commanded on	↓		
	D) R13 Fails Open-Drift	D) FF U30B expt. B is commanded on	↓		
	E) R14 Fails Open-Drift	E) FF U30B expt. B is commanded on	↓		
	F) R15 Fails Open-Drift	F) FF U30B expt B is commanded on	F)		

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PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{5}	CRITICALITY
3.8 R2 R5 R8 R3 R6 R16 R4 R7 R17	3.8 Same as 3.7	3.8 Same as 3.7	3.8 Same as 3.7	53.6	VI
3.9 R9	3.9 R9 Fails Open, Drift	3.9 Demand register might turn on all data demand lines at once	3.9 Noise might turn on all demand data lines causing mixing of data	6.0	VI
3.10 U40	3.10 A) U40A Fails High U40C Fails Low B) U40A Fails Low U40C Fails High C) U40B Fails High U40D Fails Low D) U40B Fails Low U40D Fails High	3.10 A) FF U33A expt. H is commanded on B) FF U33A expt H is commanded off C) FF U35A expt. F is commanded on D) FF U35A expt F is commanded off	3.10 A) (DDHYN) data demand line is on and data flows out (SIDYN) B) (DDHYN) data demand line is off and no data flows out (SIDYN) C) (DDFYN) data demand line is on and data flows out (SIDYN) D) (DDFYN) data demand line is off and no data flows out (SIDYN)	28.0	VI
3.11 U32A U32B U32C	3.11 A) U32A U32B Fail High U32C B) U32A U32B Fail Low U32C	3.11 A) Demand buffer register U30, U33, U34, U35 cannot be preset B) Demand buffer register stays in preset condition disabling demand buffer	3.11 A) Demand register cannot be preset when (ASEYP) command is given B) Demand Register is disabled and no data demand signals can pass	14.0	VI
3.12 U31B U32E U32F	3.12 A) U31B U32E Fail Low or High U32F	3.12 Demand buffer loses its clock and is disabled	3.12 Demand buffer is disabled and last data demand line on after the failure stays on till a preset pulse comes along and turns data demand line off	14.0	VI

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PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{5}$	CRITICALITY
3.13 U32D U31C	3.13 A) U32D Fails High U31C Fails Low B) U32D Fails Low U31C Fails High	3.13 A) FF U30A is commanded on B) FF U30A is commanded off	3.13 A) Command decoder data demand line is on and data flow out (SIDYN) B) Command decoder data demand line is off and no data flows out (SIDYN)	11.5	VI
3.14 U31A	3.14 A) U31A Fails High B) U31A Fails Low	3.14 A) DDIZP is commanded on B) DDIZP is commanded off	3.14 A) DDIZP is commanded on and cannot be turned off B) DDIZP is commanded off	5.3	VI
3.15 C9 C10 C11 C13 C14 C15	3.15 A) C9 Fails Short B) C10 Fails Short C) C11 Fails Short D) C13 Fails Short E) C14 Fails Short F) C15 Fails Short	3.15 A) Lose EDFZD data B) Lose EDGZP data C) Lose EDHZP data D) Lose EDEZP data E) Lose EDDZP data F) Lose EDBZP data	3.15 A) (EDFZP) data fails B) (EDGZP) data fails C) (EDHZP) data fails D) (EDEZP) data fails E) (EDDZP) data fails F) (EDBZP) data fails	3.3	VI

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^5$	CRITICALITY
1. Subbit Timer U68 U69 U70 U71 U67	54L04 1.1 Inverter A1-1 Fails low or high U68A Fails Q $\bar{Q}$ 1 0 54L73 0 1 1 1 0 0	.047	1.1 Subbit Timer stop all timing pulses	1.1.1 Loss Timing pulses to timing pulse generator 1.1.2 Loss start and data transfer signals for A/D converter (TT3YN) 1.1.3 Loss pulses to bit timer 1.1.4 Loss of subbit timing pulses (SB1YE)	14.66	VI
	54L04 1.2 Inverter A1-2 Fails low or high U69A fails Q $\bar{Q}$ U69B fails Q $\bar{Q}$ 0 1 0 1 54L78 0 0 54L78 1 0 0 0 1 1	.071	1.2 Subbit timer stop timing pulses for ace 10.6 KHz and LSPE 3.5 KHz	1.2 Loss timing pulse generator signals ACJZN; and DSHYP signal, HSLZN and modulator bit rate; for LSPE and ace experiments.	22.14	VI
	1.3 U69A fails Q $\bar{Q}$ 1 0 54L78 1 1	.024	1.3 Subbit timer divider E_2, E_3 divides by 2 instead of by 3	1.3 Timing pulse generator signals, for LSPE experiment are increased by 1.5	7.48	VI
	54L00 1.4 2 Input cats U70A fails high	.012	1.4 Subbit timer steps timing pulses for LSPE experiments	1.4 Loss timing pulse generator signals, for LSPE experiment	3.74	VI
	54L00 1.5 2 input gate U70A fails low U70B fails low U70C fails low or high	.046	1.5 Subbit timer stops timing pulses for ace and LSPE experiments	1.5 Loss timing pulse generator signals, for LSPE and ace experiments	14.35	VI
	54L00 1.6 2 input gate U70B fails high	.012	1.6 Subbit timer stops timing pulses for ace experiments	1.6 Loss timing pulse generator signals, for ace experiments	3.74	VI
	1.7 Counter 54L93 U71B (÷8) BCD fails high or low	.071	1.7 Subbit timer stops timing pulses for ace and LSPE experiments	1.7 Loss timing pulse generator signals, for LSPE and ace experiments	22.14	VI

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PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^5	CRITICALITY
1. Subbit Timer (Cont.)	54L04 .017 1.8 Inverter U67C fails high or low	1.8 Subbit timer stops timing pulses for ACJZN	1.8 Loss timing pulse generator signals, for ACJZN	5.30	VI
	54L04 .008 1.9 Inverter U67D fails high	1.9 A) Subbit timer would supply data shift pulses at 3.52 KHz or 10.6 KHz with control signal B at high. B) At (3.52 KHz or 10.6 KHz) and (540 Hz or 1.5 HKz) with control signal B at low.	1.9 A) Timing pulse generator signals ok B) Timing pulse generator signals DSHYP, HSLZN data shift signals at wrong pulse rates.	2.49	VI
	54L04 .008 1.10 Inverter U67D fails low	1.10 Subbit timer stops timing pulses for data shift and modulator for ACE and LSPE experiments.	1.10 Loss Timing pulse generator signals for data shift and modulator for ACE and LSPE experiments.	2.49	VI
U72	54L00 .011 1.11 2-Input gate U72A fails high	1.11 Subbit timer stops timing pulses for data shift lines and modulator for ACE and LSPE experiments	1.11 Loss timing pulse generator signals for data shift and modulator for ACE and LSPE experiments.	3.43	VI
	54L00 .022 1.12 2-Input gate U72A fails low U72B fails low	1.12 Subbit timer stops timing pulses for data shift lines and modulator for all experiments	1.12 Loss timing pulse generator signals for data shift and modulator for all experiments.	6.86	VI
	54L00 .011 1.13 2-Input Gate U72B fails high	1.13 Subbit timer stops timing pulses for data shift lines and modulator which need 540 Hz or 1.06 KHz.	1.13 Loss timing pulse generator signals for data shift and modulator which need 540 Hz or 1.06 KHz.	3.43	VI

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PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^5$	CRITICALITY
1. Subbit Timer (Cont)	54L00 1.14 2-Input Gate U72C fails high and low " " U55C " " "	.022	1.14 Subbit Timer stops timing pulses for data shift lines and modulator for all experiments	1.14 Loss timing pulse generator signals for data shift and modulator for all experiments	6.86	VI
	54L04 1.15 Inverter U67E fails low 54L04 1.15 Inverter U67E fails high	.017	1.15 Subbit timer stops timing pulses for data shift lines and modulator which need 540 Hz and TT3YN, TT2YP which need 8.44 KHz 1.15A) Subbit timer supplies timing pulses correctly if slow mode command is given B) If normal mode command is given the subbit timer supplies timing pulses at 540 Hz with 75% duty cycle and TT3YN pulses at 4.28 KHz with 75% duty cycle	1.15 Loss timing pulse generator signals for data shift lines and modulator which need 540 Hz and TT3YN, TT2YP which need 8.44 KHz for transfer signals for A/D conv. 1.15A) Timing pulse generator signals are correct if slow mode command is given B) If normal mode command is given the subbit timer supplies timing pulses at 540 Hz with 75% duty and TT3YN pulses at 4.28 KHz with 75% duty cycle	5.30	VI
U73 U74 U75	54L00 1.16 2 Input gate U73C fails high	.0[illegible]	1.16 Subbit timer stops timing pulses for data shift, modulator, TT3YN, and bit timer when slow mode command is given	1.16 No pulses for subbit timer data shift, modulator TT3YN, and bit timer when slow mode command is given	3.43	VI
	54L00 1.17 2 Input gate U73C fails low 2 Input gate U73A fails low	.022	1.17 Subbit timer stops timing pulses for data shift, modulator, TT3YN, and bit timer when slow or normal mode commands are given	1.17 No pulses for subbit timer data shift, modulator, TT3YN, and bit timer when slow or normal mode commands are given	6.86	VI
	54L00 1.18 2 Input gate U73A fails high	.031	1.18 Subbit timer stops timing pulses for data shift, modulator, TT3YN, and bit timer when normal mode command is given	1.18 No pulses for subbit timer data shift, modulator TT3YN, and bit timer when normal mode command is given	3.43	VI
	54L00 1.19 2 input gate U73B fails high or low U73D fails high or low	.045	1.19 Subbit timer stops timing pulses for data shift, modulator TT3YN, and bit timer when normal or slow mode commands are given	1.19 No pulses for subbit timer data shift, modulator TT3YN, and bit timer when normal mode or slow mode commands are given	14.03	VI

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PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁵	CRITICALITY
1. Subbit Timer (Cont)	54L73 Q $\bar{Q}$ 1.20 FF-U68B fails 0 0; 0 1; 1 0; 1 1 FF-U74A fails (Q $\bar{Q}$) 1 0; 0 0 FF-U74B fails (Q $\bar{Q}$) 1 0; 0 1; 0 0 FF-U75A fails (Q $\bar{Q}$) 1 0; 0 1; 0 0 FF-U75B fails (Q $\bar{Q}$) 1 0; 0 1; 1 1	.198	1.20 Divide by ten counter stops and subbit timer stops timing pulses	1.20 No pulses for subbit timer data shift, modulator TT3YN, and bit timer when normal or slow mode commands are given	61.75	VI
	54L73 Q $\bar{Q}$ 1.21 FF-U74A fails 0 1; 1 1 FF-U74B fails (Q $\bar{Q}$) 1 1 FF-U75A fails (Q $\bar{Q}$) 1 1 FF-U75B fails (Q $\bar{Q}$) 1 1	.038	1.21 Divide by ten counter. Divide by two instead of by ten	1.21 Pulse rate for subbit timer data shift, modulator and bit timer are increased by factor of 5 for normal or slow mode commands	11.85	VI

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{-3}$	CRITICALITY
1. Subbit Timer (Cont) U76 U77	54L00 1.22 2-Input gate U70D fails-low	.012	1.22 Divide by ten counter (E5-E9) stops dividing by 10	1.22 No pulses for subbit timer, data shift, modulator, and bit timer	3.74	VI
	54L00 1.23 2-Input gate U70D fails-high	.012	1.23 Divide by ten counter (E5-E9) Operates manually except E6, E7 and E8 might not be reset properly and cause an error in pulse rate	1.23 Might have error in pulses for subbit timer, data shift, modulator, and bit timer	3.74	VI
	54L04 1.24 Inverter U67F fails-high or low	.117	1.24 Counter E10-E13 stops dividing by eight	1.24 No pulses for subbit timer, data shift, modulator and bit timer	5.30	VI
	54L73 1.25 FF-U76A fails: Q Q̄ = 1 0; 0 1; 0 0 FF-U76B fails: Q Q̄ = 1 0; 0 0 FF-U77A fails: Q Q̄ = 1 0; 0 1; 0 0 FF-U77B fails: Q Q̄ = 1 0; 0 1; 0 0	.457	1.25 Counter E10-E13 stops dividing by eight	1.25 No pulses for subbit timer, data shift, modulator and bit timer	47.09	VI

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PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE — ASSEMBLY	EFFECT OF FAILURE — END ITEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
1. Subbit Timer (Cont)	54L73 1.26 FF-U76A fails Q 1, $\bar{Q}$ 1 FF-U76B fails Q 0, $\bar{Q}$ 1; Q 1, $\bar{Q}$ 1 FF-U77A fails Q 1, $\bar{Q}$ 1 FF-U77B fails Q 1, $\bar{Q}$ 1	.038	1.26 Counter E10-E13 divides by 2 instead of by eight	1.26 Pulse rate for subbit timer, data shift, modulator and bit timer will increase	11.85	VI
	54L20 1.27 2 input gate U72D fails low	.011	1.27 Counter E10-E13 stops divide by eight	1.27 No pulses for sub-bit timer, data shift, modulator and bit timer	3.43	VI
	54L20 1.28 2 input gate U27D fails high	.011	1.28 Counter E10-E13 divides by ten but a miss count might cause error	1.28 might have error in pulses for sub-bit	3.43	VI
	1.29 Counter 54L93 U71A fails low or high	.024	1.29 Counter E14 stops dividing by 2 and slow mode loses its timing pulses	1.29 No pulses for sub-bit timer, data shift, modulator and bit timer in slow mode command	7.48	VI

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PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE — ASSEMBLY	EFFECT OF FAILURE — END ITEM	FAILURE PROBABILITY Q x 10⁻⁵	CRITICALITY
2. Timing Pulse Generator U78 U79 U80 U81	54L10 .085 2.1 3-input gate U78A fails-low, high	2.1 Timing pulse generator poses DGYN, DGTYP, FMN, FMLZN, and NFYN, AALZP, ACLZP	2.1 A) Data gate output DGYN, DGTYP fail B) Fram marker outputs, FMN, FMLZN, NFIZN and NFYN fail C) Analog multiplex AALZA and active seimic closk ALSEP outputs fail	9.65	VI
	54L04 .043 2.2 Inverter U79A fails-low high	2.2 Timing pulse generator loses DGTYP, FMN, FMLZN, NFIZN NFYN, AALZP, ACLZP	2.2 Timing pulse generator out-put DGTYP, FMN, FMLZN, NFIZN NFYN, AALZP, ACLZP fail	4.88	VI
	54L04 .030 2.3 Inverter U81B fails low	2.3 Timing pulse generator loses FMN, FMLZN	2.3 Timing pulse generator output FMN, FMLZN fail	3.41	VI
	54L04 .013 2.4 Inverter U81B fails high	2.4 Timing pulse generator outputs FMN, FMLZN, ARS on for all 90 words in a frame instead of for 1 word in each frame	2.4 Fram marker outputs FMN and FMLZN are on for all 90 words in a frame instead of for 1 word in each frame.	1.48	VI
	54L00 .044 2.5 2 input gate U80A fails low	2.5 Timing pulse generator outputs FMN and FMLZN	2.5 Fram marker outputs FMN, FMLZN fail	5.00	VI
	54L00 .019 2.6 2 input gate U80A fails high	2.6 Timing pulse generator outputs FMN, FMLZN, NFIZN and NFYN fail	2.6 A) fram marker outputs FMN, FMLZN fail B) 90 fram marker outputs NFYN and NFYN fail	2.16	VI
Timing Pulse Generator U50 U82 U59	54L04 .030 2.7 Inverter U81A fails low	2.7 Timing pulse generator loses FMLZN, NFIZN and NFYN	2.7 A) fram marker for multiplexer outputs FMLZN fails B) 90 fram marker NFIZN and NFYN fail	3.41	VI
	54L04 .013 2.8 Inverter U81A fails high	2.8 timing pulse generator loses FMLZN	2.8 fram marker for multiplexer output FMLZN fail	1.48	VI

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PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^5$	CRITICALITY
2 Timing Pulse Generator	2.9 54L04 Inverter V81C Fails low or high	.043	2.9 Timing pulse generator loses FMLZN	2.9 Frame marker for multiplexer output FMLZN fails	4.88	VI
	2.10 54L00 2-Input gate U80D fails low or high	.063	2.10 Timing pulse generator loses NFIZN and NFYN	2.10 90 Frame marker outputs NFIZN and NFYN fail	7.15	VI
	2.11 54L04 Inverter U50E fail low or high	.046	2.11 Timing pulse generator loses NFIZN	2.11 90 Frame marker output NFIZN fails	5.22	VI
	2.12 54L10 3-Input gate U78B fail low or high	.083	2.12 Timing pulse generator loses PCLYN signal	2.12 Multiformat command advance PCLYN fails	9.42	VI
	2.13 54L04 Inverter U79B fail low or high	.043	2.13 Timing pulse generator loses SIFYP and AALZP signals	2.13 a) 64 word interval output SIFYP fails b) Analog multiplex advance gives false information or fails AALZP	4.88	VI
	2.14 54L00 2-Input gate U80B fail low or high 54L04 Inverter U81D fail low or high	.106	2.14 Timing pulse generator loses AALZP signal	2.14 Analog multiplex advance output AALZP fails	12.03	VI
	2.15 54L00 2-Input gate U82A fail low or high	.063	2.15 Timing pulse generator loses HSLZH signal	2.15 Housekeeping shift to D/A converter output HSLZN fails	7.15	VI
	2.16 54L20 4-Input gate U59B fail low or high 54L04 Inverter U81E fail low or high	.167	2.16 Timing pulse generator loses ACLZP signal	2.16 Active seismic clock output ACLZP fails	18.96	VI
	2.17 54L00 a) 2-Input gate U80E fails low or high b) Inverter U81F fails low or high	.106	2.17 Timing pulse generator loses CWEZP	2.17 Active Seismic clock output CWEZP fails	12.03	VI
3 Control Logic U83 U84	3.1 54L00 2-Input gate U83A fails high 54L20 4-Input gate U84A fails low	.129	3.1 Timing Pulse generator ACJZN stays at 3.52 kHz	3.1 Active seismic clock output stays at 3.52 kHz	11.96	VI
U85	3.2 54L00 2-input gate U83A fails low 54L20 4-Input gate U84A fails high	.098	3.2 Timing pulse generator ACJZN stays at 10 kHz, SBJYN stays 28.17 kHz	3.2 Active seismic clock output stays at 10 kHz	9.08	VI

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PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10[-6]	CRITICALITY
3 Control Logic	3.3 54L20 4-Input gate U84B fails low 54L00 2-Input gate U83D fails high	.129	3.3 Subbit timer stays in slow mode all time	3.3 Timing pulse generator outputs data shift (DSHYP), HSLZN housekeeping shift and bit rats to modulator stay in slow mode	11.96	VI
	3.4 54L20 4-Input gate U84B fails high 54L00 2-Input gate U83D fails low	.098	3.4 Subbit timer stays in normal mode and the time	3.4 Timing pulse generator outputs data shift (DSHYP), (HSLZN) housekeeping shift and bit rat8 to modulator stay in normal mode	9.08	VI
	3.5 54L74 a) F.F. U85A fails Q 1, $\overline{Q}$ 0 b) fails Q 0, $\overline{Q}$ 1 c) fails Q 1, $\overline{Q}$ 1 d) fails Q 0, $\overline{Q}$ 0	.159	3.5 a) Subbit timer stays in normal mode all the time b) Subbit timer stays in slow mode all the time c) Subbit timer stays in slow mode d) Subbit timer stays in normal mode	3.5 a) Timing pulse generator outputs stay in normal mode b) Timing pulse generator output stay in slow mode c) Timing pulse generator output stay in slow mode but control word gen. will say data processor is in normal and slow mode d) Timing pulse generator output stay in normal mode but control word generator will say data processor is not in mormal mode or slow mode	14.74	VI
	3.6 54L00 a) 2-input gate U82B fails high b) 2-Input gate U82B fails low	.078	3.6 a) Subbit timer for LSPE experiment will not go from normal mode to slow mode b) Subbit timer has output of 1 kHz or 540 kHz for data shift for all operating modes	3.6 a) Timing pulse generator output in LSPE experiment (ACJYN) will not go from normal mode to slow mode b) Timing pulse generator's data shift pulses are in error for LSPE and active seismic experiments	7.23	VI
	3.7 54L74 a) F.F. U85B fails Q 0, $\overline{Q}$ 1	.159	3.7 a) Subbit timer will stay in normal mode when you command slow mode for normal mode and slow mode get wrong data shift signals	3.7 a) Timing pulse generator's output DSHYP, HSLZN modulator clock will be at wrong rate in normal and slow modes.	14.73	VI

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁵	CRITICALITY
	3.7 b) 54L74 F.F. U85B fails Q/Q̄ 1/0	3.7 b) Subbit timer LSP will not shift to slow mode and LSP and active seismic experiments will have wrong data shift pulses, and modulator clock frequency	3.7 b) Timing pulse generators output DSAYP, HSLZN, modula[illegible] clock will be at wrong rate [illegible] and active seismic exper[illegible] command		
	c) fails Q/Q̄ 1/1	c) Subbit timer LSP experiment command will not go into its slow mode and normal and slow modes will have wrong pulse rate for data shift pulses, and modulator clock frequency	c) Timing pulse generators output DSHYP, HSLZN, modulator clock will be at wrong rate for normal and slow mo[illegible]		
	d) fails Q/Q̄ 0/0	d) Subbit timer will not shift from normal to slow mode rate	d) Timing pulse generator output DSHYP, HSLZN, modulator clock will be at wrong rate for LSP and active seismic experiment commands.		
	54L00 .076 3.8 a) 2-Input gate U83B fails high	3.8 a) Subbit timer will not shift from normal mode to slow mode	3.8 a) Timing pulse generator output DSHYP, HSLZN, modulator clock will be at wrong rate for slow mode command	7.04	VI
	b) fails low	b) Subbit timer will not shift from slow mode to normal mode	b) Timing pulse benerator outputs DSH[illegible], HSLZN, modulator clock will be at wrong rate for normal mode command		
	54L00 .076 3.9 a) 2-Input gate U83C fails high	3.9 a) Subbit timer has wrong output for LSP and active seismic experiments	3.9 a) Timing pulse generator outputs DSHYP, HSLZN, m[illegible] clock will be at wrong ra[illegible] LSP and active seismic ex[illegible]iments	7.04	VI
	b) fails low	b) Subbit timer has wrong output for normal and slow modes	b) Timing [illegible] generator output DSHYP, HSLZN, modulator clock will be at wrong rate for normal [illegible] slow mode commands.		

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PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10[5]	CRITICALITY
4 Fram Counter U50	54L04 4.1 Inverter U50C fails low Inverter U50D fails low	.055	4.1 Frame counter stay reset and frame frame counter stops counting	4.1 Frame Counter stops counting and mode selection (3 word 10 digit) stays in last state	6.87	VI
	54L04 4.2 Inverter U50C fails high Inverter U50D fails high	.024	4.2 Frame counter will not reset after 90th frame	4.2 Control word generator will have wrong frame count after 90th word	3.00	VI
U56	54L73 4.3 F.F. U56A fails Q Q̄: 1 0; 1 1	.059	4.3 Frame counter stops counting	4.3 Control word generator stops producing control words, event frame marker counts 2 times as fast	7.37	VI
	54L73 4.4 F.F. U56A fails Q Q̄: 0 1; 0 0	.059	4.4 Frame counter stops counting	4.4 Control word generator stops producing control words, event frame marker stops	7.37	VI
	54L73 4.5 F.F. U56B fails Q Q̄: 0 1; 1 0; 0 0; 1 1	.118	4.5 Frame counter stops counting in 2d - 7th digits	4.5 Control word generator has wrong frame count	14.74	VI
U57	54L73 4.6 F.F. U57A fails Q Q̄: 0 1; 1 0; 0 0; 1 1	.118	4.6 Frame counter stops counting in 3d - 7th digits	4.6 Control word generator has wrong frame count	14.74	VI
	54L73 4.7 F.F. U57B fails Q Q̄: 0 1; 1 0; 0 0; 1 1	.118	4.7 Frame counter stops counting in 4th - 7th digits	4.7 Control word generator has wrong frame count	14.74	VI
U58	54L73 4.8 F.F. U58A fails Q Q̄: 0 1; 1 0; 0 0; 1 1	.118	4.8 Frame Counter stops counting in 5th - 7th digits	4.8 Control word generator has wrong frame count	14.74	VI

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁵	CRITICALITY
4 Fram Counter	4.9 54L73 F.F. U58B. fails Q/Q̄: 0 1; 1 0; 0 0; 1 1	.118	4.9 Frame counter stops counting in 6th - 7th digits	4.9 Control word generator has wrong frame count	14.74	VI
	54L73 4.10 F.F. U47B fails Q/Q̄: 0 1; 1 0; 0 0; 1 1	.118	4.10 Frame counter stops counting in 7th digit	4.10 Control word generator has wrong frame count	14.74	VI
U46G	54L20 4.11 2-Input gate U46G fails high, low	.058	4.11 Event frame marker stops working (EFMTN)	4.11 Event frame marker stops working (EFMTN)	7.26	VI
U50B	4.12 Inverter U50B fails high, low	.039	4.12 Frame counter stops counting	4.12 Control word generator has wrong words	4.87	VI
5 Control Word Generator U64A U45D	54L10 5.1 3-Input gate U64A fails high low; 54L04 Inverter U45D fails high or low	.040	5.1 Error in normal speed command in control word generator	5.1 Control word generator 3-word 10 digit mode selection will be in error for normal speed command	13.48	VI
U64B U45E	54L10 5.2 3-Input gate U64B fails high or low; 54L04 Inverter U45E fails high or low	.040	5.2 Error in slow speed command in control word generator	5.2 Control word generator 3-word 10 digit mode selection will be in error for slow speed command	13.48	VI
U66A U66B U46D U66C	54L10 5.3 3-Input gate U66A fails high or low; " " U66B " " "; " " U46D " " "; " " U66C " " "	.106	5.3 Error in normal speed command in control word generator	5.3 Control word generator 3-word 10 digit mode selection will be in error	35.73	VI
U64C U65A U65B U65C	54L10 5.4 3-Input Gate U64C fails high or low; " " U65A " " "; " " U65B " " "; " " U65C " " "	.112	5.4 Error in serial number command in control word generator	5.4 Control word generator 3-word 10 digit mode selection will be in error for serial number	37.75	VI

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PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁻⁵	CRITICALITY
5 Control Word Generator U59A	54L00 .054 5.5 4-Input Gate U59A fails high or low; 54L04 Inverter U45C fails high or low	5.5 Error in 3-word 10 digit mode selection	5.5 Control word generator 3-word 10 digit mode selection will be in error	18.20	VI
U60A U61A U62A U63A U53C	54L10 .138 5.6 3-Input Gate U60A fails high or low; " " U61A " " "; " " U62A " " "; 54L00 4-Input Gate U63A " " "; 54L04 Inverter U53C fails high or low	5.6 Error in frame count 3-word digits 6-9 in control word generator	5.6 Control word generator frame count 3-word digits 6-9 will be in error	46.52	VI
U62B U62C U61C U63B U53D	54L10 .138 5.7 3-Input gate U62B fails high or low; " " U62C " " "; " " U61C " " "; 54L20 4-Input gate U63B " " "; 54L04 6-Inverter U53D fails high or low	5.7 Error in frame count 3-word digits 3-5 in control sord generator	5.7 Control word generator frame count 3-word digits 3-5 will be in error	46.52	VI
U60C	54L10 .028 5.8 3-Input gate U60C fails high or low	5.8 Error in control word generator 3-word, 10 digit	5.8 Control word generator mode selection 3-word, 10 digit will be in error	9.44	VI
U52C	54L00 .021 5.9 2-Input gate U52C fails high or low	5.9 Error in control word generator 3-word, 1-2 digits	5.9 Control word generator mode selection 3-word, 1-2 digits will be in error	7.08	VI

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM	PREPARED BY	NO.	REV.
ALSEP E	J. G. Smith	ATM 950	
END ITEM: Data Processor	DWG NO.	PAGE 33 of 46	
ASS'Y: Timing and Control Word Gen.	DWG NO. 2349416	DATE 1/4/71	

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{5}$	CRITICALITY
5 Control Word Generator U60B U52D U53A	.061 54L10 5.10 3-Input gate U60B fails high or low 54L00 2-Input gate U52D " " " 54L04 Inverter U53A fails high or low	5.10 Error in control word generator 3-word	5.10 Control word generator mode selection 3-word will be in error	20.56	VI
U53E	.012 54L04 5.11 Inverter U53D fails high or low	5.11 3-word will be in error from control word generator	5.11 Control word generator 3-word output will be in error to multiformat commutator (THRZN)	4.05	VI
U51A U52A U52B U54A	.085 54L00 5.12 2-Input gate U51A fails high or low " " U52A " " " " " U52B " " " " " U54A " " "	5.12 1-word will be in error from control word generator	5.12 Control word generator 1-word output will be in error	28.65	VI
U53A	.012 54L04 5.13 Inverter U53A a) fails low b) fails high	5.13 a) 1-3 word will be in error b) 1-word will be in error	5.13 a) Control word generator 1-3 word will be in error b) Control word generator 1-word will be in error	4.05	VI
U51B U51C U51D U54B	.085 54L00 5.14 2-Input gate U51B fails high or low " " U51C " " " " " U51D " " " " " U54B " " "	5.14 2-word will be in error from control word generator	5.14 Control word generator 2-word will be in error	28.65	VI
U53B	.012 54L04 5.15 Inverter U53B a) fails low b) fails high	5.15 a) 1-3 word will be in error b) 2-word will be in error	5.15 a) Control word generator 1-3 word will be in error b) Control word generator 2-word will be in error	4.05	VI
U55B	.028 54L10 5.16 3-Input gate U55B fails high or low	5.16 1-3 word will be in error	5.16 Control word generator 1-3 word will be in error	9.44	VI
U55A	.028 54L10 5.17 3-Input gate U55A fails high or low	5.17 Product of 1-3 word commands to modulator will be in error	5.17 Control word generator output of product of 1-3 word commands to modulator will be in error	9.44	VI

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM ALSEP E	PREPARED BY J.G. Smith	NO. ATM 950	REV.
END ITEM Data Processor	DWG NO.	PAGE 34 of 46	
* ASS'Y Timing and Control Word Gen.	DWG NO. 2349416	DATE 1/10/71	

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{3}$	CRITICALITY
6 Bit Timer 6.1 U45A U45B	54L04 6.1 Inverters U45A fail low or high " U45B " " "	.080	6.1 Bit timer has error in counting	6.1 Control word generator has error in output due to bit timer timing pulse generator outputs DGTYN, DGTYP, FMZTN, PCLYN are in error	8.07	VI
6.2	54L00 6.2 2-Input gate U46A fails high	.071	6.2 Might cause error in bit timer if U48A, U48B, U49A flip flop do not reset properly	6.2 Control word generator might have error	7.16	VI
6.3 U47A	54L73 6.3 a) F.F. U47A fails Q / Q̄: 0 0; 0 1; 1 0; 1 1	.729	6.3 a) Divide by ten counter stops and bit timer stops timing pulses	6.3 a) Bit timer stops operating and (BPIZP) bit period of bit timer and control word generator stop operating	73.57	VI
U48A	F.F. U48A fails Q / Q̄: 1 0; 0 0					
U48B	F.F. U48B fails Q / Q̄: 1 0; 0 1; 0 0					
U49A	F.F. U49A fails Q / Q̄: 1 0; 0 1; 0 0					
U49B	F.F. U49B fails Q / Q̄: 1 0; 0 1; 1 1					

SYSTEM ALSEP E	PREPARED BY J.G. Smith	NO. ATM 950	REV.
END ITEM Data Processor	DWG NO.	PAGE 35 of 46	
ASSY Timing and Control Word Gen.	DWG NO. 2349416	DATE 1/21/71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁵	CRITICALITY
6.3 Bit Timer U48A	6.3 b) 54L73 F.F. U48A fails Q/Q̄: 0/1, 1/1	6.3 b) Divide by ten counter divides by two instead of by ten	6.3 b) Bit timer, (BPIZP) bit period of bit timer and control word generator will operate at pulse rate 5 times greater than normal		
U48B	F.F. U48B fails Q/Q̄: 1/1				
U49A	F.F. U49A fails Q/Q̄: 1/1				
U49B	F.F. U49B fails Q/Q̄: 1/1				
6.4 U46B	.071 54L00 6.4 2-Input gate fails high or low	6.4 Bit timer output (BPIZN) bit period of bit timer fails	6.4 Bit period of bit timer fails	7.16	VI
6.5 U50A	.049 54L04 6.5 a) Inverter fails low	6.5 a) Bit timer stops sending pulses to timing pulse generator	6.5 a) timing pulse generator outputs (DGTYP) data gate, (PMLZN) frame marker multiplex, and (PCLYN) multiformat command advance fail no output pulses	4.94	VI
	54L04 b) Inverter fails high	b) Bit timer stops sending pulses to timing pulse generator	b) Timing pulse generator outputs (DGTYP) data gate, (FMLZN) frame marker multiplex, and (PCLYN) multiformat command advance have false output pulses		
7 Modulator U82C	.063 54L00 7.1 a) 2-Input gate fails low	7.1 a) modulator loses active seismic data and all other serial data from experiments	7.1 a) Modulator outputs TAK, TBK, TCK lose active seismic data and all other serial data from experiments	7.13	VI
U82C	b) 2-Input gate fails high	b) Modulator loses active seismic data	b) Modulator output TAK, TBK, TCK lose active seismic data		

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM ALSEP E	PREPARED BY J. C. Smith	NO. ATM 950	REV.
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ASSY Timing and Control Word Gen.	DWG NO. 2349426	DATE 1/15/71	

PART/COMPONENT SYMBOL		FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁵	CRITICALITY
7 Modulator	U82D	54L00 7.2 2-Input gate fails low or high	.063	7.2 Modulator loses active seismic data and all other serial data from experiments	7.2 Modulator outputs TAK, TBK, TCK lose active seismic data and all other serial data from experiments	7.13	VI
	U88A	54L74 7.3 F.F. U88A fails high low (Q, Q̄: 1 0; 0 1)	.130	7.3 Modulator loses active seismic data and all other serial data from experiments	7.3 Modulator outputs TAK, TBK, TCK lose active seismic data and all other serial data from experiments	14.71	VI
	U86A	54L04 7.4 a) Inverter fails low	.046	7.4 a) Modulator loses active seismic data and all other serial data from experiments	7.4 a) Modulator outputs TAK, TBK, TCK lose active seismic data and all other serial data from experiment	5.21	VI
	U86B	b) Inverter fails high		b) Modulator will have errors in control word data if serial input data is presented simultaneously	b) Modulator outputs TAK TBK, TCK will have errors in control word data if serial input data is presented simultaneously		
	U54C	54L00 7.5 a) 2-Input gate fails low b) 2-Input gate fails high	.063	7.5 a) modulator loses all data b) modulator loses control word generator data	7.5 a) modulator output TAK, TBK, TCK loses all data b) Modulator outputs TAK, TBK, TCK lose control word generator data	7.13	VI
	U54D	54L00 7.6 a) 2-Input gate fails high b) 2-Input gate fails low	.063	7.6 a) Modulator loses serial data from experiments b) Modulator loses all data	7.6 a) Modualtor outputs TAK, TBK, TCK lose serial data from experiments b) Modulator outputs TAK, TBK, TCK lose all data	7.13	VI
	U87A	54L00 7.7 2-Input gate fails low, high	.063	7.7 Modulator loses all data	7.7 Modulator outputs TAK, TBK, TCK lose all data	7.13	VI
	U88B	54L74 7.8 F.F. U88B (Q, Q̄: 1 0; 0 1; 1 1; 0 0)	.130	7.8 Modulator loses all data	7.8 Modulator outputs TAK, TBK, TCK lose all data	14.71	VI

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SYSTEM ALSEP E	PREPARED BY J.G. Smith	NO. ATM 950	REV.
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ASS'Y Timing and Control Word Gen.	DWG NO. 2349426	DATE 1/15/71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^-9	CRITICALITY
Modulator U87B	54L00 7.9 a) 2-Input gate fails low b) 2-Input gate fails high	.063	7.9 a) Modulator loses all data b) Modulator loses all data which is logical zero	7.9 a) Modulator output TAK, TBK, TCK lose all data b) Modulator output TAK, TBK, TCK lose all data which is logical zero	7.13	VI
U87C	54L00 7.10 a) 2-Input gate fails low b) 2-Input gate fails high	.063	7.10 a) Modulator loses all data b) Modulator loses all data which is logical one	7.10 a) modulator output TAK, TBK, TCK lose all data b) Modulator output TAK, TBK, TCK lose all data which is logical one	7.13	VI
U87D	54L00 7.11 2-Input gate fails high, low	.063	7.11 Modulator loses all data	7.11 Modulator output TAK, TBK, TCK lose all data	7.13	VI
U86F	54L04 7.12 Inverter fails high, low	.046	7.12 Modulator loses TCK output data	7.12 Modulator output TCK fails loses all data	5.21	VI
U86E	54L04 7.13 Inverter fails high, low	.046	7.13 Modulator loses TBK, TCK output data	7.13 Modulator outputs TBK, TCK lose all data	5.21	VI
U86D	54L04 7.14 Inverter fails high, low	.046	7.14 Modulator loses TAK output data	7.14 Modulator output TAK loses all data	5.21	VI
U90A	54L74 7.15 F.F. fails Q / $\bar{Q}$: 1/0, 0/1, 1/1, 0/0		7.15 Modulator loses all data	7.15 Modulator output TAK, TBK, TCK lose all data	14.71	VI
					1155.34	

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SYSTEM ALSEP E	PREPARED BY J.G. Smith	NO. ATM 950	REV.
END ITEM Data Processor	DWG NO.	PAGE 38 of 46	
ASS'Y X-Card Interface module	DWG NO. 2349456	DATE 1/22/71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^5	CRITICALITY
Interface Module 1.1 U1	54L04 .064 1.1 Inverter	1.1	1.1	30.30	VI
	A) U1-A Fails High	A) Lose frame mark-B signal with +5VX Supply	A) (FMBZP) Frame mark B signal is lost when X interface module is on		
	B) U1-B " "	B) Lose frame mark-C signal with +5VX Supply	B) (FMCZP) Frame mark C signal lost when X interface module is on		
	C) U1-C " "	C) Lose frame Mark-D signal with +5VX supply	C) (FMDZP) Signal is lost same as A		
	D) U1-D " "	D) Lose frame Mark-E signal with +5VX supply	D) (FMEZP) Signal is lost same as A		
	E) U1-E " "	E) Lose frame Mark-G signal with +5VX supply	E) (FMEZP) Signal is lost same as A		
	F) U1-F " "	F) Lose 90th frame -G signal with +5VX supply	F) (NFGZP) Signal is lost same as A		
	G) U1-A Fails Low	G) 1. Lose frame marker-B signal with +5VX or +VY if U1-A sinking transistor fails shorted 2. Lose frame marker-B signal with +5VX if U1-A sinking transistor's drive circuit fails causing sinking transistor to stay in zero condition as long as 5VX is applied	G) 1. (FMBZP) Signal with +5VX or +5VY fails if U1-A sinking transistor fails shorted 2. (FMBZP) Signal with +5VX fails if U1-A sinking transistor's drive circuit fails causing sinking transistor to stay in 0 condition as long as X interface module is on		
	H) U1-B " "	H) Same as G) with U1-B	H) (FMCZP) Signal fails same as G		
	I) U1-C " "	I) " " G) " U1-C	I) (FMDZP) Signal fails same as G		
	J) U1-D " "	J) " " G) " U1-D	J) (FMEZP) Signal fails same as G		
	K) U1-E " "	K) " " G) " U1-E	K) (FMGZP) Signal fails same as G		
	L) U1-F " "	L) " " G) " U1-F	L) (NFGZP) Signal fails same as G		

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SYSTEM ALSEP E	PREPARED BY J. G. Smith	N/L ATM 950	REV.
END ITEM Data Processor	DWG NO.	PAGE 39 of 46	
ASS'Y X-Card Interface Module	DWG NO. 2349436	DATE 1/22/71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{3}$	CRITICALITY
1.2 U3	1.2 54L04 Inverter A) U3-A Fails High	.064	1.2 A) Lose data demand line-B signal with +5VX supply	1.2 A) (DDBZP) Data demand signal with +5VX supply is lost	30.30	VI
	B) U3-B " "		B) Lose Data demand lined signal with +VX supply	B) (DDDZP) Signal is lost like A)		
	C) U3-C " "		C) Lose data demand line-E signal with +5VX supply	C) (DDEZP) Signal is lost like A)		
	D) U3-D " "		D) Lose data demand line-G signal with +5VX supply	D) (DDGZP) Signal is lost like A)		
	E) U3-E " "		E) Lose data demand line-F signal with +5VX supply	E) (DDFZP) Signal is lost like A)		
	F) U3-F " "		F) Lose 90th from -C signal with +5VX supply	F) (NFCZP) Signal is lost like A)		
	G) U3-A Fails Low		G) 1. Lose data demand Line-B with +5VX or +5VY if U3-A sinking transistor fails shorted 2. Lose data demand line-B signal with +5VX if U1-A sinking transistor's drive circuit fails causing sinking transistor to stay in zero condition as long as 5VX is applied.	G) 1. (DDBZP) Data demand signal with +5VX or +5VY fails if U3-A sinking transistor fails shorted 2. (DDBZP) Signal with +5VX fails if U3-A sinking transistor's drive circuit fails causing sinking transistor to stay in zero condition as long as X interface module is on.		
	H) U3-B " "		H) Same as G) with U3-B	H) (DDDZP) Signal fails same as G)		
	I) U3-C " "		I) Same as G) with U3-C	I) (DDEZP) Signal fails same as G)		
	J) U3-D " "		J) Same as G) with U3-D	J) (DDGZP) Signal fails same as G)		
	K) U3-E " "		K) Same as G) with U3-E	K) (DDFZP) Signal fails same as G)		
	L) U3-F " "		L) Lose 90th from -C signal with +5VX supply	L) (NFCZP) Signal fails same as G)		
1.3 U4 U5	1.3 54L04 Inverter A) U4-A Fails High	.064	1.3 A) Same as U3-A A)	1.3 A) (NFBZP) 90th from signal with +5VX Supply is lost	30.30	VI

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ASS'Y X-Card Interface Module	DWG NO. 2349456	DATE 1/22/71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q × 10⁻⁵	CRITICALITY
1.3 Interface Module	1.3 54L04 Inverter	1.3	1.3		
	B) U4-B Fails High	B) Same as U3-A A)	B) (NFDZP) 90th from signal with +5VX Supply is lost		
	C) U4-C " "	C) " " " "	C) (NFEZP) " " " " "		
	D) U4-D " "	D) " " " "	D) (SLBZN) Shift line signal with +5VX Supply is lost		
	E) U4-E " "	E) " " " "	E) (SLCZN) " " " " "		
	F) U4-F " "	F) " " " "	F) (SLDZN) " " " " "		
	1.3 G) U5-A Fails Low	1.3 G) Same as U3-A G)	1.3 G) (NFBZP) Fails same as U3-A G)		
	| | |	| |	| |		
	L) U5-F " "	L) Same as U3-F L)	L) (SLDZN) Fails same as U3-F L)		
1.4 U7	1.4 .064	1.4	1.4	30.30	VI
	A) U7-A Fails High	A) Same as U3-A A)	A) (SLEZN) Fails same as U3-A A)		
	B) U7-B " "	B)	B) (DGBZP)		
	C) U7-C " "	C)	C) (EFBZP)		
	D) U7-D " "	D)	D) (SBJZP)		
	E) U7-E " "	E)	E) (ACJZP)		
	F) U7-F " "	F) Same as U3-F F)	F) (DGFZP) Fails same as U3-F F)		
	G) U7-A Fails Low	G) Same as U3-A G)	G) (SLEZN) Fails same as U3-A G)		
	| | |	| |	| |		
	L) U7-F " "	L) Same as U3-F L)	L) (DGFZP) Fails same as U3-F L)		

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM	PREPARED BY	NO.	REV.
ALSEP E	J. G. Smith	ATM 950	
END ITEM: Data Processor	DWG NO.	PAGE 41 of 46	
ASS'Y X-Card Interface Module	DWG NO. 2349456	DATE 1/22/71	

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
1.5* Resistor - R1 Capacitor - C1	1.5 A) R1 Fails Open C1 Fails Short B) R1 Fails Drift C1 Fails Drift	.011	1.5 A) Lose frame mark for LSG experiment B) 90th frame mark for LSG still works	1.5 A) (FMBZP) Frame E mark signal fails B) (NFBZP) 90 frame signal will still work	5.21	III
1.6* Resistor - R2 Capacitor - C2	1.6 A) R2 Fails Open C2 Fails Short B) R2 Fails Drift C2 Fails Drift	.011	1.6 A) Loss 90th frame mark for LSG experiment B) 90th frame mark for LSG still work	1.6 A) (NFBZP) 90frame signal fails B) (NFBZP) 90 frame signal will still work	5.21	III
1.7* R-3 C-3	1.7* A) R3 Fails Open C3 Fails Short B) R3 Fails Drift C3 Fails Drift	.011	1.7 A) Lose frame mark for C-experiment B) Frame mark for C-experiment still works	1.7 A) (FMCZP) Signal fails B) (NFBZP) Signal will still work	5.21	III
1.8* R4 C4	1.8 A) R4 Fails Open C4 Fails Short B) R4 Fails Drift C4 Fails Drift	.011	1.8 A) Lose 90th frame mark for LEAM experiments B) 90th frame mark for LEAM still works	1.8 A) (NFDZP) Signal fails B) (NFDZP) Signal will still work	5.21	III
1.9* R5 C5	1.9 A) R5 Fails Open C5 Fails Short B) R5 Fails Drift C5 Fails Drift	.011	1.9 A) Lose frame mark for LEAM expriment B) Frame mark for LEAM experiment still works	1.9 A) (FMDZP) Signal fails B) (FMDZP) Signal will still work	5.21	III
1.10* R6 C6	1.10 A) R6 Fails Open C6 Fails Short B) R6 Fails Drift C6 Fails Drift	.011	1.10 A) Lose 90th frame for LMS expriment B) 90th frame for LMS experiment still works	1.10 A) (NFEZP) Signal fails B) (NFEZP) Signal will still work	5.21	III
1.11* R8 C8	1.11 A) R8 Fails Open C8 Fails Short B) R8 Fails Drift C8 Fails Drift	.011	1.11 A) Lose shift line for LSG experiment B) Shift line for LSG Experiment still works	1.11 A) (SLBZN) Signal fails B) (SLBZN) Signal still works	5.21	III

* [illegible] redundant

SYSTEM ALSEP E	PREPARED BY J. G. Smith	NO. ATM 950	REV.
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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁻⁵	CRITICALITY
Interface Module 1.12* R7 C7	1.12 A) R7 Fails Open C7 Fails Short B) R7 Fails Drift C7 Fails Drift	.011	1.12 A) Loss frame mark for LMS experiment B) Frame mark for LMS experiment still works	1.12 A) (FMEZP) signal fails B) (FMEZP) signal still works	5.21	III
1.13* R9 C9	1.13 A) R9 Fails Open C9 Fails Short B) R9 Fails Drift C9 Fails Drift	.011	1.13 A) Lose frame mark for heat flow experiment B) Frame mark for heat flow experiment still works	1.13 A) (FMGZP) signal fails B) (FMGZP) signal still works	5.21	III
1.14* R10 C10	1.14 A) R10 Fails Open C10 Fails Short B) R10 Fails Drift C10 Fails Drift	.011	1.14 A) Lose data shift line for C-experiment B) Data shift line for C-experiment still works	1.14 A) (SLCZN) signal fails B) (SLCZN) signal still works	5.21	III
1.15* R11 C11	1.15 A) R11 Fails Open C11 Fails Short B) R11 Fails Drift C11 Fails Drift	.011	1.15 A) Lose 90th frame for G-experiment B) 90th frame for heat flow experiment still works	1.15 A) (NFGZP) signal fails B) (NFGZP) signal still works	5.21	III
1.16* R12 C12	1.16 A) R12 Fails Open C12 Fails Short B) R12 Fails Drift C12 Fails Drift	.011	1.16 A) Lose data shift line for leam experiment B) Data shift line for leam expt. still works	1.16 A) (SLDZN) signal fails B) (SLDZN) signal still works	5.21	III
1.17* R13 C13	1.17 A) R13 Fails Open C13 Fails Short B) R13 Fails Drift C13 Fails Drift	.011	1.17 A) Lose data demand line for LSG experiment B) Data damand line for LSG expt. still works	1.17 A) (DDBZP) signal fails B) (DDBZP) signal still works	5.21	III
1.18* R14 C14	1.18 A) R14 Fails Open C14 Fails Short B) R14 Fails Drift C14 Fails Drift	.011	1.18 A) Lose data shift line for LMS experiment B) Data shift line for LMS expt. still works	1.18 A) (SLEZN) signal fails B) (SLEZN) signal still works	5.21	III

*These items are non-redundant.

SYSTEM ALSEP E	PREPARED BY J. G. Smith	NO. ATM 950	REV.
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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁵	CRITICALITY
1.19* R15 C15	1.19 .011 A) R15 Fails Open; C15 Fails Short B) R15 Fails Drift; C15 Fails Drift	1.19 A) Lose data demand line for leam experiment B) Data demand line for leam expt. still works	1.19 A) (DDDZP) signal fails B) (DDDZP) signal still works	5.21	III
1.20* R16 C16	1.20 .011 A) R16 Fails Open; C16 Fails Short B) R16 Fails Drift; C16 Fails Drift	1.20 A) Lose data shift line for heat flow experiment B) Data shift line for heat flow expt. still works	1.20 A) (SLGZN) signal fails B) (SLGZN) signal still works	5.21	III
1.21* R17 C17	1.21 .011 A) R17 Fails Open; C17 Fails Short B) R17 Fails Drift; C17 Fails Drift	1.21 A) Lose data demand line for LMS experiment B) Data demand ;ine for LMS expt. still works	1.21 A) (DDEZP) signal fails B) (DDEZP) signal still works	5.21	III
1.22* R18 C18	1.22 .011 A) R18 Fails Open; C18 Fails Short B) R18 Fails Drift; C18 Fails Drift	1.22 A) Lose data shift line for LSP experiment B) Data shift line for LSP experiment still works	1.22 A) (SLJZN) signal fails B) (SLJZN) signal still works	5.21	III
1.23* R21 C19	1.23 .011 A) R21 Fails Open; C19 Fails Short B) R21 Fails Drift; C19 Fails Drift	1.23 A) Lose data demand pulse heat flow experiment B) Data demand pulse heat flow experiment still works	1.23 A) (DDGZP) signal fails B) (DDGZP) signal still works	5.21	III
1.24* R28 C22	1.24 .011 A) R28 Fails Open; C22 Fails Short B) R28 Fails Drift; C22 Fails Drift	1.24 A) Loss data demand signal for F experiment B) Data demand signal for F expt. still works	1.24 A) (DDGZP) signal fails B) (DDFZP) signal still works	5.21	III
1.25* R35 C26	1.25 .011 A) R35 Fails Open; C26 Fails Short B) R35 Fails Drift; C26 Fails Drift	1.25 A) Lose data gate signal for B experiment B) Data gate signal for B expt. still works	1.25 A) (DGBZP) signal fails B) (DGBZP) signal still works	5.21	III

*These items are non-redundant.

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁻⁵	CRITIC-ALITY
1.26* R36 C27	1.26 .011 A) R36 Fails Open C27 Fails Short B) R36 Fails Drift C27 Fails Drift	1.26 A) Lose event frame signal for B experiment B) Event frame signal for B-expt. still works	1.26 A) (EFBZP) signal fails B) (EFBZP) signal still works	5.21	III
1.27* R38 C29	1.27 .011 A) R38 Fails Open C29 Fails Short B) R38 Fails Drift C29 Fails Drift	1.27 A) Lose LSP clock signal B) LSP clock signal still works	1.27 A) (ACJZP) signal fails B) (ACJZP) signal still works	5.21	III
1.28* R39 C30	1.28 .011 A) R39 Fails Open C30 Fails Short B) R39 Fails Drift C30 Fails Drift	1.28 A) Lose data gate signal for F-expt. B) Data gate signal still works	1.28 A) (DGFZP) signal fails B) (DGFZP) signal still works	5.21	III
1.29* R40 C31	1.29 .011 A) R40 Fails Open C31 Fails Short B) R40 Fails Drift C31 Fails Drift	1.29 A) Lose 90th frame signal for C-experiment B) 90th frame signal for C-expt. still works	1.29 A) (NFCZP) signal fails B) (NFCZP) signal still works	5.21	III
1.30 C23	1.31 .002 A) C23 Fail Short B) C23 Fail Drift	1.31 A) Cause CR2 zener diode to fail B) Could allow noise to give a false signal	1.31 A) (PRSXN) signal give command to change supply sources from x to y B) (PRSXN) signal might be wrong due to noise	0.95	VI

*These items are non-redundant

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁵	CRITICALITY
1.31 R31	1.32 .010 A) R31 Fails Open B) R31 Fails Drift	1.32 A) Reset circuit still work in degrated mode B) Circuit still works	1.32 A) (PRSXN) signal still work if 5vx goes to zero volts B) (PRSXN) signal still works	4.74	VI
1.32 CR2	1.33 .118 A) CR2 Fails Short B) CR2 Fails Open C) CR2 Fails Drift	1.33 A) Reset circuit still work in degraded mode B) Circuit fails C) Circuit works in degraded mode	1.33 A) (PRSXN) signal still works if 5vx goes to zero B) (PRSXN) signal gives false signal C) (PRSXN) signal still works if 5vx goes to zero	55.87	VI
1.33 R29	1.34 .005 A) R29 Fails Open B) R29 Fails Drift	1.34 A) Reset circuit fails B) Circuit works in degraded mode	1.34 A) (PRSXN) signal gives false signal B) (PRSXN) signal still works if 5 vx goes to zero	4.26	VI
1.34 C24	1.35 .002 A) C24 Fails Short B) C24 Fails Open	1.35 A) Reset circuit fails B) Reset circuit loses delay on turn on	1.35 A) (PRSXN) signal gives false signal B) (PRSXN) signal loses the delay when signal goes from zero to one	0.95	VI

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁻⁵	CRITICALITY
1.35	1.36 .114	1.36	1.36	53.98	VI
Q1A R32 R30 R27 R35 R34 U9C, D	A) Q1A Fails Open Fails Short R32 Fails Open R30 Fails Open R27 Fails Open R35 Fails Open R34 Fails Open U9C Fails High U9D Fails High U9C Fails Low U9D Fails Low	A) Power on reset circuit fails to respond to lose of supply voltage X	A) (PRSXN) power on reset fails		
	B) Q1A Fails Drift R32 Fails Drift R30 Fails Drift R27 Fails Drift R35 Fails Drift R34 Fails Drift	B) Power on reset circuit works but with reduced sensitivity	B) (PRSXN) power on reset work in degraded mode		
				493.70	

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