Bendix Aerospace Systems Division

ALSEP Array E - Command Decoder
Failure Modes, Effects &
Criticality Analysis

ATM 949

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DATE 6-1-71

This ATM documents the Failure Modes, Effects and Criticality Analysis on the Bendix designed Command Decoder for the Array E ALSEP System. The analysis reflects analysis on those parts which are presently planned to be used in final flight configuration.

This document is prepared in accordance with the requirements of Section 5.2 of the Reliability Program Plan for Array E, ALSEP-RA-08, Bendix document number BSR 3024 dated 11-30-70.

Reliability prediction data are also documented herein in accordance with Section 5.5 of the Array E Reliability Program Plan.

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1.0 Introduction

The results of the Reliability Prediction and the Failure Mode, Effects, and Criticality Analysis for ALSEP E Command Decoder are documented in this report. This Command Decoder represents the Bendix Designed unit which makes extensive use of low power TTL integrated circuits.

The reliability prediction for the Command Decoder is .99928 which exceeds the specified goal of .99000.

2.0 Circuit Description

Figure 1 shows the block diagram of one side of the redundant portion of the Command Decoder, and also of the non-redundant (back-up) functions on the Command Sequencer board. This diagram is included to clarify the terms and descriptions given in the Failure Mode, Effects, and Criticality Analysis portion of this ATM (Table II).

The logical flow of a ground command is from the receiver to the Data Demodulator, where it is converted into digital form and passed to the Control Logic and then to the Decode Gate board. The form of this data is three seven bit words, the first being the ALSEP address, the second the command complement for parity checking purposes, and the third word is the command. The Command Sequencer board provides the back-up functions of generating the repeated commands, the uplink switch-over circuit, and the ripple-off circuit.

2.1 Data Demodulator

The Data Demodulator circuit converts biphase baseband data from the Command Receiver into "Non Return to Zero" (NRZ) digital data and also provides uplink clock and threshold signals for the control logic portion of the Command Decoder. The unit is designed to accept a composite waveform which is the sum of a 1 KHz clock and a 2 KHz data subcarrier. The 2 KHz subcarrier is phase modulated by a 1000 bit/second data stream. The Phase Lock Loop (PLL) section provides the signals both to detect the data and clock it out to the Command Register in the Control Logic Section by locking to the 1 KHz uplink clock generated at the ground station. The phase lock loop contains circuitry which generates 4 phases of a 1 KHz square wave. One

phase is used to drive the VCO to the phase lock condition while the other phases of the 1 KHz clock are gated together to produce the control logic clocks and provide 2 KHz signals for the data detector. The data detector consists of two detection chains, one to detect "1" bits and the other to detect "0" bits. The outputs of the two detection chains are connected to give a logic "1" output when a valid bit one is detected in the "1" chain and when a good bit zero is detected in the "0" chain. The outputs are clocked into the data flip flop by a short pulse generated near the end of each bit. Thus, NRZ data is obtained from the data flip flop, delayed by one bit from the baseband data. The threshold circuits are in two sections. Firstly, the analog threshold, described above, which ensures that output of the integrate and dump circuit is large enough before the comparators can produce data. Secondly, the digital threshold circuit which ensures that at least four valid data bits must be produced before the NRZ data is allowed into the Command Register in the Control Logic. The gate output of this circuitry is the digital threshold signal, and it is used to inhibit the data flip flop and also to reset the control logic, should a data dropout occur.

2.2 Control Logic

The Control Logic consists of an eight bit shift register, two counters, and reset circuitry. The shift register (Command Register) has the NRZ data passing through it at the rate of 1 KHz. A gate constantly samples the first seven bits of the shift register for the address of the particular ALSEP. Once an address is recognized, a timing sequence is initiated. After address recognition, the next seven pulses shift the command complement into the last seven bits of the shift register. The binary counter, ensures that the next seven bits of data (the command) clocked in are checked for parity. An exclusive OR gate sensing the first and last bits of the shift register performs a parity check on each bit of the command complement and the corresponding bit of the command. The command sequence pulse is gated with the parity flip flop to produce a command execute pulse. After command has been executed, a logical signal VWEZP is sent to the Data Processor and causes a data demand signal DDIZP to be sent back to the command decoder.

2.3 Decode Gates

The decode gate matrix decodes a seven bit binary command into individual command lines. A command execute pulse, CEXAN, is used

to create the correct command pulse length. The decoding takes place in two levels. The first level creates outputs from all combinations of the first four bits (16) and from all combinations of the remaining three bits (8). This is accomplished with four-input gates, with the fourth input of the group of eight used for the command execute pulse. The output decoding is carried out with two input gates, all having inputs associated with each of the two groups of first level gates. One hundred and four commands of a possible 128 are decoded, with resistors provided in 53 outputs for rise time control. The capacitors for this control are provided on the Control Logic board.

2.4 Command Sequencer

The Command Sequencer consists of a free running binary counter with decoding logic wired to Experiment Calibrate command lines. The sequencer also functions as an uplink switch-over timer to ensure a switch from one uplink chain to the other in case of an uplink failure. The clock for the counter is the 90th frame mark, NFIZP, a 118 us pulse appearing every 54 seconds, generated within the Data Processor. Once the commands are generated, they are "OR'd" with the experiment calibrate command lines in the redundant section of the command sequencer. Also, within this redundant section is an "enable/inhibit repeated commands" flip flop which, by means of two commands, lets the ground user of ALSEP decide whether the repeated calibrate commands should be provided to the experiments or not. This inhibit feature also permits the repeated command sequencer to be disabled in case of a failure in any of the non-redundant circuitry. The Ripple-off circuit consists of an 8-bit binary counter and decoding gates producing the commands. The counter is clocked by the CWE clock, a 1060 Hz clock generated within the Data Processor. The loss of a "Reserve Power" signal from the PCU causes seven power loads to be switched sequentially to standby after a predetermined length of time.

3.0 Reliability Prediction

The reliability prediction for the Command Decoder operating in standby redundant configuration is calculated to be .99928 for launch, deployment and two years of lunar operation. The predicted reliability exceeds the specified goal of .99000 as stated in ATM 889, Section 4.2.

Figure 2 defines the Reliability Block Diagram and Mathematical Model for the Command Decoder. Two identical channels are represented by "A" in operation, and "B" in standby redundancy. The components associated with switching and located on the only non-redundant module represent the third reliability function. The fourth block represents the single point failures in the Control Logic and Decode Gate Modules.

The probability failures for each functional component identified in Figure 2 are tabulated in Table I. The probability failures shown represent composite totals derived from the parts application stress ratios of each electronic piece part modified by the failure mode apportionment.

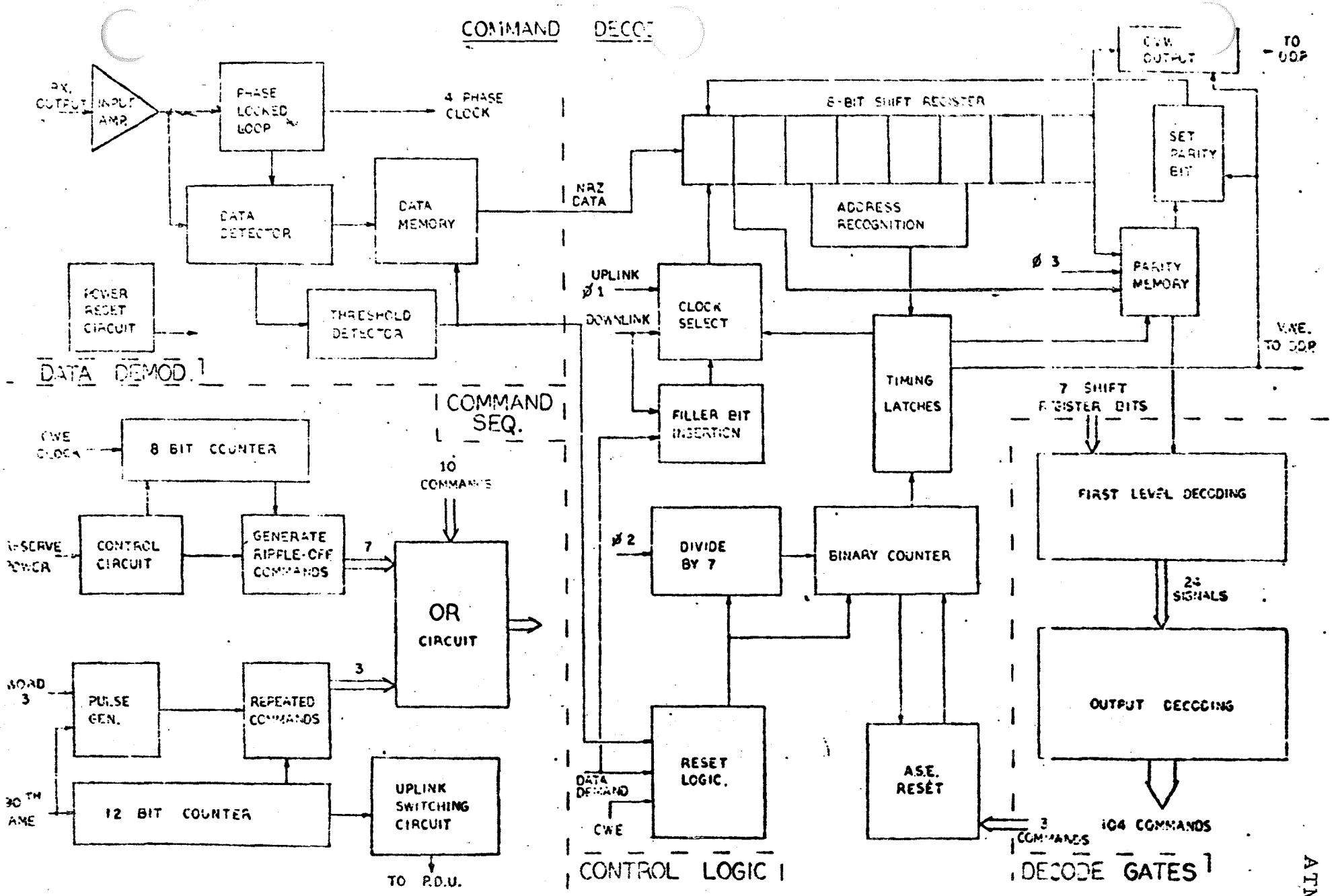
COMMAND DECOD
R.X. OUTPUT
INPUT AMP.
PHASE LOCKED LOOP
4 PHASE CLOCK
DATA DETECTOR
DATA MEMORY
NRZ DATA
POWER RESET CIRCUIT
THRESHOLD DETECTOR
DATA DEMOD.
8-BIT SHIFT REGISTER
C.W. OUTPUT
TO D.D.P.
SET PARITY BIT
ADDRESS RECOGNITION
PARITY MEMORY
UPLINK ø1
DOWNLINK
CLOCK SELECT
ø3
V.N.E. TO D.D.P.
TIMING LATCHES
7 SHIFT REGISTER BITS
COMMAND SEQ.
FILLER BIT INSERTION
C.W.E. CLOCK
8 BIT COUNTER
10 COMMANDS
FIRST LEVEL DECODING
RESERVE POWER
CONTROL CIRCUIT
GENERATE RIPPLE-OFF COMMANDS
7
ø2
DIVIDE BY 7
BINARY COUNTER
24 SIGNALS
OR CIRCUIT
BOARD 3
PULSE GEN.
REPEATED COMMANDS
3
OUTPUT DECODING
30TH ANE
12 BIT COUNTER
UPLINK SWITCHING CIRCUIT
RESET LOGIC.
A.S.E. RESET
DATA DEMAND
C.W.E.
3 COMMANDS
104 COMMANDS
TO P.D.U.
CONTROL LOGIC
DECODE GATES

FIGURE 1

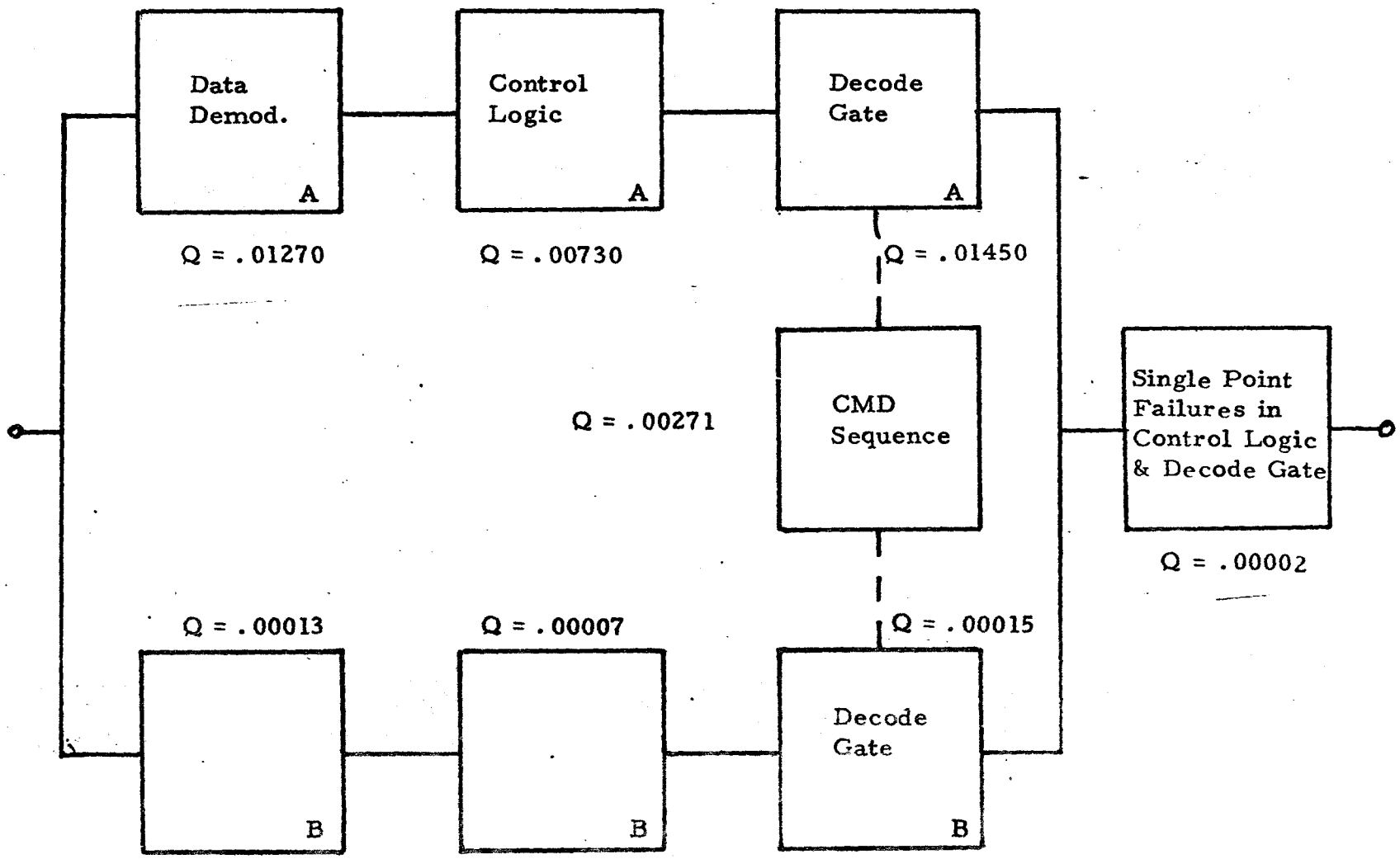

Figure 2 Command Decoder Reliability Block Diagram

TABLE I

PROBABILITY FAILURE SUMMARY

Assembly	Operating	Standby
Data Demodulator A*	.01270	.00013
Control Logic A	.00730	.00007
Control Logic SPFS	.00001	
Decode Gates A	.01450	.00015
Decode Gates SPFS	.00001	
Totals	$Q_1 = .03450$	$Q_2 = .00035$
Sequencer (Switching)	$Q_s = .00271$	

*B Boards have same failure rates as A Boards.

3.1 Reliability Calculations

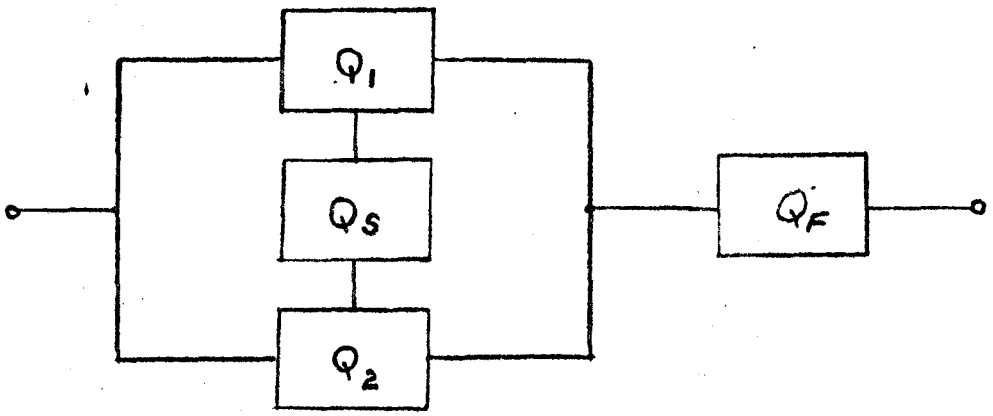

Figure 2 RELIABILITY MODEL

3.1.1

Q_1 = Probability Failure in Operation

Q_2 = Probability Failure in Standby

Q_S = Probability Failure in Switching

Q_F = Probability Failure in Single Point Failures

$$Q_T = \frac{Q_1 \cdot Q_1}{2} + \frac{Q_1 \cdot Q_2}{2} + Q_1 R_2 Q_S + Q_F$$

$$Q_T = \frac{Q_1^2}{2} + \frac{Q_1 \cdot Q_2}{2} + Q_1 R_2 Q_S + Q_F$$

3.1.2

$$R_T = 1 - Q_T$$

$$R_T = 1 - \frac{Q_1^2}{2} - \frac{Q_1 \cdot Q_2}{2} - Q_1 R_2 Q_S - Q_F$$ Reliability Equation for Command Decoder

3.1.3 $Q_2 = 1 - R_2$

$R_2 = 1 - Q_2$

$R_2 = 1 - .00035$

$R_2 = .99965$

$Q_1 = .03450$

$Q_2 = .00035$

$Q_S = .00271$

$Q_F = .00002$

$$Q_T = \frac{(Q_1)^2}{2} + \frac{Q_1 \cdot Q_2}{2} + Q_1 \cdot R_2 \cdot Q_S + Q_F$$

$$Q_T = \frac{(.03450)^2}{2} + \frac{(.03450)(.00035)}{2} + (.03450)(.99965)(.00271) + .00002$$

$Q_T = .00060 + .00001 + .00009 + .00002$

$Q_T = .00072$

3.1.4 $R_T = 1 - Q_T$

$R_T = 1 - .00072$

$R_T = .99928$

4.0 FAILURE MODES, EFFECTS AND CRITICALITY ANALYSIS

The failure mode and effects analysis for the Command Decoder are documented in Table II. The failure probabilities reflect the identified line item. The criticality column lists in descending order the criticality as applied to the ALSEP system failure modes. This column will provide criticality rankings in accordance with BSR 3024, Section 5.2.2. The criteria for criticality rankings is listed in 4.1.

The format of Table II is designed to provide the reader with a narrative description of the varying types of failures that could occur, combined with the resultant performance characteristics. This information is useful to system support in performing fault isolation should any anomally occur.

There are two ALSEP-E single point failures within the Command Decoder itself. They are the two single lines between the Data Processor and Command Decoder. The CL0011ZN signal is a single point failure which will result in loss of all data except for LSPE, while the EXFZN signal will cause the system to go into the ASE Data Mode and remain there. The circuitry required to eliminate the two single point failures is extremely complex and reliability trade-off studies have shown that the increased complexity makes the circuitry less reliable.

The failure probability figures were derived using the data contained in ATM-954, the Command Decoder Parts Application Analysis. ATM 605A was used to derive the component α's (open, short, drift, etc. apportionments). Some failure modes, such as drift of a resistor in a digital circuit, do not affect the operation. The failure modes which do not affect the operation are not included in the FMECA. For this reason, the sum of α's for some circuit/function items do not always equal one. However, all Command Decoder piece-part failure modes which do not affect the operation of the Command Decoder or any other unit in ALSEP are included in the FMECA (Table II).

4.1 The criticality code to be used in the criticality column of Table II is listed below according to the following criteria:

I Loss of system

II Loss of system control

III Loss of one experiment

IV Loss of housekeeping channel(s)

V Loss of redundant element

VI Degradation of a redundant element

5.0 Reliability Assessment

The purpose of performing a reliability prediction and failure modes analysis is to identify inherent design weaknesses. From the results of these analyses it has been concluded the reliability and design objectives have been fully satisfied.

SYSTEM ALSEP	PREPARED BY M. Papaioan	NO. A 949	REV.
END ITEM Command Decoder	DWG NO.	PAGE 13 of 27	
ASS'Y Decode Gates	DWG NO 2367626	DATE 6-1-71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE			(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
1.0 Input Buffer and Inverter: U1A, U1B	1.1	U1A, U1B,	Fail	Low .70	1.1 U1A will act as an enable signal to 4-input nand gates, U3B, U4B, U5B, U6B, U7B, U8B, U9B, and U10B. U1B will act as an inhibit signal to 4-input nand gates.	1.1 Failure of U1A will permit one (1) possible wrong command to be executed when commanded. When U1B fails, fifty-three (53) commands will be inoperative and not capable of being executed.	1.1 7.36	VI
	1.2	U1A, U1B	Fail	High .30	1.2 U1A will act as an inhibit signal to 4-input nand gates U1B will act as an enable signal to 4-input nand gates.	1.2 When U1A fails, fifty-three (53) commands will be inoperative and not capable of being executed. Failure of U1B will permit one (1) possible wrong command to be executed when commanded.	1.2 3.15	V
2.0 Input Buffer: U1C	2.1	U1C	Fail	Low .70	2.1 Acts as an inhibit signal to 4-input nand gates, U3A, U4A, U5A, U6A, U7A, U8A, U9A, and U10A.	2.1 Fifty-one (51) commands will be inoperative and not capable of being executed.	2.1 3.68	V
	2.2	U1C	Fail	High .30	2.2 Acts as an enable signal to 4-input nand gates.	2.2 One (1) possible wrong command will be executed when commanded.	2.2 1.58	VI
3.0 Input Buffer and Inverter: U1D, U1E	3.1	U1D, U1E	Fail	Low .70	3.1 U1D will act as an enable signal to 4-input nand gates, U7A, U7B, U8A, U8B, U9A, U9B, U10A, U10B. U1E will act as an inhibit signal to 4-input nand gates.	3.1 Failure of U1D will permit one (1) possible wrong command to be executed when commanded When U1E fails, fifty-one (51) commands will be inoperative and not capable of being executed.	3.1 7.36	VI
	3.2	U1D, U1E	Fail	High .30	3.2 U1D will act as an inhibit signal to 4-input nand gates. U1E will act as an enable signal to 4-input nand gates.	3.2 When U1D fails, fifty-one (51) commands will be inoperative and not be capable of being executed. Failure of U1E will permit one (1) possible wrong command to be executed when commanded.	3.2 3.15	V

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL		FAILURE MODE			(α)	EFFECT OF FAILURE: ASSEMBLY		EFFECT OF FAILURE: END ITEM		FAILURE PROBABILITY Q x 10^{-5}		CRITICALITY
4.0	Input Buffer: U1F	4.1	U1F	Fail	Low .70	4.1	Acts as an inhibit signal to 4-input nand gates, U3A, U3B, U4A, U4B, U5A, U5B, U6A and U6B.	4.1	Fifty-one (51) commands will be inoperative and not capable of being executed.	4.1	3.68	V
		4.2	U1F	Fail	High .30	4.2	Acts as an enable signal to 4-input nand gates.	4.2	One (1) possible wrong command will be executed when commanded.	4.2	1.58	VI
5.0	Input Buffer And Inverter: U2A, U2B	5.1	U2A, U2B	Fail	Low .70	5.1	U2A will act as an enable signal to 4-input nand gates, U4A, U4B U6A, U6B, U8A, U8B, U10A, and U10B. U2A will act as an inhibit signal to 4-input nand gates.	5.1	Failure of U2A will permit one (1) possible wrong command to be executed when commanded. When U2B fails, fifty-four (54) commands will be inoperative and not capable of being executed.	5.1	7.36	VI
		5.2	U2A, U2B	Fail	High .30	5.2	U2A will act as an inhibit signal to 4-input nand gates. U2B will act as an enable signal to 4-input nand gates.	5.2	When U2A fails, fifty-four (54) commands will be inoperative and not capable of being executed. Failures of U2B will permit one (1) possible wrong command to be executed when commanded.	5.2	3.15	V
6.0	Input Buffer: U2C	6.1	U2C	Fail	Low .70	6.1	Acts as an inhibit signal to 4-input nand gates, U3A, U3B, U5A, U%B, U7A, U7B, U9A and U9B.	6.1	Sixty (60) commands will be inoperative and not capable of being executed.	6.1	3.68	V
		6.2	U2C	Fail	High .30	6.2	Acts as an enable signal to 4-input nand gates.	6.2	One (1) possible wrong command will be executed when commanded.	6.2	1.58	VI
7.0	Input Buffer and Inverter U2D, U3E	7.1	U2D, U2E	Fail	Low .70	7.1	U2D will act as an enable signal to 4-input nand gates, U3A, U3B, U4A, U4B, U7A, U7B, U8A, and U8B U2D will act as an inhibit signal to 4 input nand gates.	7.1	Failure to U2D will permit one(1) possible wrong command to be executed when commanded. When U2D fails, sixty-three (63) commands will be inoperative and not capable of being executed.	7.1	7.36	VI

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
7.0 (Continued)	7.2 U2D, U2E Fail High	.30	7.2 U2d will act as an inhibit signal to 4-input nand gates. U2E will act as an enable signal to 4-input nand gates.	7.2 When U2D fails, sixty-three (63) commands will be inoperative and not capable of being executed. Failure of U2E will permit one (1) possible wrong command to be executed when commanded.	7.2 3.15	V
8.0 Input Buffer: U2F	8.1 U2F Fail Low	.70	8.1 Acts as an inhibit signal to 4-input nand gates, U5A, U5B, U6A, U6B, U9A, U9B, U10A, and U10B.	8.1 Fifty-one (51) commands will be inoperative and not capable of being executed.	8.1 3.68	V
	8.2 U2F Fail High	.30	8.2 Acts as an enable signal to 4-input nand gates.	8.2 One (1) possible wrong command will be executed when commanded.	8.2 1.58	VI
9.0 Input Buffer: U11A	9.1 U11A Fail Low	.70	9.1 Acts as an inhibit signal to 4-input nand gates, U13A, U13B, U15A, and U15B.	9.1 Fifty-three (53) commands will be inoperative and not capable of being executed.	9.1 3.68	V
	9.2 U11A Fail High	.30	9.2 Acts as an enable signal to 4-input nand gates.	9.2 One (1) possible wrong command will be executed when commanded.	9.2 1.58	VI

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE		(α)	EFFECT OF FAILURE: ASSEMBLY		EFFECT OF FAILURE: END ITEM		FAILURE PROBABILITY $Q \times 10^{-5}$		CRITICALITY
10.0 Input Buffer: U11B	10.1	U11B fail low	.70	10.1	Acts as an inhibit signal to 4-input nand gates, U14A, U14B, U15A and U15B.	10.1	Fifty-four (54) commands will be inoperative and not capable of being executed.	10.1	3.68	V
	10.2	U11B fail high	.30	10.2	Acts as an enable signal to 4-input nand gates.	10.2	One (1) possible wrong command will be executed when commanded.	10.2	1.58	VI
11.0 Input Buffer: U11C	11.1	U11C fail low	.70	11.1	Acts as an inhibit signal to 4-input nand gates, U12B, U13B, U14B and U15B.	11.1	Fifty-four (54) commands will be inoperative and not capable of being executed.	11.1	3.68	V
	11.2	U11C fail high	.30	11.2	Acts as an enable signal to 4-input nand gates.	11.2	One (1) possible wrong command will be executed when commanded.	11.2	1.58	VI
12.0 Input Buffer: U11D	12.1	U11D fail low	.70	12.1	Acts as an inhibit signal to 4-input nand gates, U12A, U12B, U13A, U13B, U14A, U14B, U15A, and U15B.	12.1	One hundred-four (104) commands will be inoperative and not capable of being executed.	12.1	3.68	V
	12.2	U11D fail high	.30	12.2	Acts as an enable signal to 4-input nand gates.	12.2	Possible random command will be executed.	12.2	1.58	VI
FIRST TIER										
13.0 U3A, U3B, U4A, U4B, U5A, U5B, U6A, U6B, U7A, U7B, U8A, U8B U9A, U9B, U10A, U10B	13.1	Fail low U3A, U3B, U4A, U4B, U5A, U5B, U6A, U6B, U7A, U7B, U8A, U8B, U9A, U9B, U10A, U10B	.70	13.1	Acts as an inhibit signal to 2nd tier gate.	13.1	A possible eight (8) wrong commands will be executed when commanded.	13.1	176.60	VI
	13.2	Fail high U3A, U3B, U4A, U4B, U5A, U5B, U6A, U6B, U7A, U7B, U8A, U8B, U9A, U9B, U10A, U10B	.30	13.2	Acts as an enable signal to 2nd tier gate.	13.2	A maximum of eight (8) commands will be inoperative and not capable of being executed.	13.2	75.69	VI

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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
14.0 U12A, U12B, U13A, U13B, U14A, U14B, U15A, U15B	14.1 Fail low U12A, U12B, U13A, U13B, U14A, U14B, U15A, U15B	.70	14.1 Acts as an inhibit signal to 2nd tier gate.	14.1 A possible eight (8) wrong commands will be executed when commanded.	14.1 88.30	VI
	14.2 Fail high U12A, U12B, U13A, U13B, U14A, U14B, U15A, U15B	.30	14.2 Acts as an enable signal to 2nd tier gate.	14.2 A maximum of fourteen (14) commands will be inoperative and not capable of being executed.	14.2 37.84	VI
SECOND TIER						
15.0 U11E, U11F, U16A, U16B, U17A, U17B, U18A, U18B, U19A, U19B, U20A, U20B, U20C, U20D, U20E, U20F	15.1 Fail low U11E, U11F, U16A, U16B, U17A, U17B, U18A, U18B, U19A, U19B, U20A, U20B, U20C, U20D, U20E, U20F	.70	15.1 Acts as an inhibit signal to 3rd tier gate.	15.1 A maximum of eight (8) commands will be inoperative and not capable of being executed.	15.1 58.87	VI
	15.2 Fail high U11E, U11F, U16A, U16B, U17A, U17B, U18A, U18B, U19A, U19B, U20A, U20B, U20C, U20D, U20E, U20F	.30	15.2 Acts as an enable signal to 3rd tier gate.	15.2 A maximum of eight (8) wrong commands will be executed when commanded.	15.2 25.23	VI
16.0 U16C, U16D, U16E, U16F, U17C, U17D, U17E, U17F, U18C, U18D, U18E, U18F, U19C, U19D, U19E, U19F	16.1 Fail low U16C, U16D, U16E, U16F, U17C, U17D, U17E, U17F, U18C, U18D, U18E, U18F, U19C, U19D, U19E, U19F	.70	16.1 Acts as an inhibit signal to 3rd tier gate.	16.1 A maximum of eight (8) commands will be inoperative and not capable of being executed.	16.1 58.87	VI
	16.2 Fail high U16C, U16D, U16E, U16F, U17C, U17D, U17E, U17F, U18C, U18D, U18E, U18F, U19C, U19D, U19E, U19F	.30	16.2 Acts as an enable signal to 3rd tier gate.	16.2 A maximum of eight (8) wrong commands will be executed when commanded.	16.2 25.23	VI

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	M. Papaioan	ATM 949	
END ITEM: Command Decoder	DWG NO.	PAGE 18 of 27	
ASS'Y: Decode Gate	DWG NO. 2367626	DATE 6-1-71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
17.0 104 Two-Input Nand Gates (Exclusively on sheets 4, 5 & 6 of Dwg. 2349326)	17.1 Fail low	.68	17.1 Permanent Command	17.1 Switch to redundant unit to regain functions.	17.1 565.76	V
	17.2 Fail high	.30	17.2 No commands will be executed.	17.2 Switch to redundant unit to regain functions.	17.2 245.98	V
	17.3 Fail low (short)	.01	17.3 Permanent Command	17.3 Cannot be removed by switching to redundant unit.	17.3 8.20	II
	17.4 U25A - Fail Low except for pulldown transistor	.01	17.4 Permanent Command	17.4 Same as 17.2	17.4 4.08	V
	17.5 U25A - Pulldown transistor on chip U25A fails low		17.5 Permanent Command	17.5 Single point failure - loss of all data except for LSPE.	17.5 1.36	I

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	M. Papaioan	949	
END ITEM	DWG NO.	PAGE 19 of 27	
Command Decoder			
ASS'Y	DWG NO.	DATE	
Control Logic	2367636	6-1-71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
1.0 Counter M/Program Counter Circuitry and Input and Output Buffers: U5, U9A, U9B, U1A, U1B, U7A, U7B, U7C, U8A, U4B	1.1 Low - U5, U9A, U9B, U4B High - U8A	.324	1.1 No Counter Output	1.1 Permanent Low Level Out	38.3	V
	1.2 Low - U8A High - U4B	.076	1.2 No Counter Output	1.2 Permanent High Level Out	8.99	V
	1.3 Low - U1A, U1B High - U1A, U1B	.133	1.3 No Clock Input	1.3 Permanent Low Level Out	15.73	V
	1.4 High - U5, U9A	.200	1.4 Erroneous Count	1.4 Output - Count of 3	23.65	V
	1.5 Low - U7A, U7C High - U7B, U9B	.180	1.5 Erroneous Count	1.5 Output - Count of 4	21.29	V
	1.6 Low - U7B High - U7A, U7C	.087	1.6 Erroneous Count	1.6 Output - Count of 8	10.29	V
2.0 Counter M/Program Counter Circuitry and Input and Output Buffers: U12A, U14A, U14B, U10A, U11A, U16A, U13C, U11B, U13A, U13B	2.1 Low - U10A, U11A High - U10A, U11A	.120	2.1 No clock input to counter Gate U13A permanently high.	2.1 No Command Executed	15.77	V
	2.2 U12A Q $\bar{Q}$ 1 1 1 0 0 1 0 0	.240	2.2 Gate U13A permanently high.	2.2 No Command Executed	31.54	V
	2.3 U14A Q $\bar{Q}$ 1 1 1 0 0 1 0 0	1.20	2.3 Counter keeps cycling to a count of 2. Gate U13A permanently high.	2.3 No Command Executed	15.77	V
	2.4 U14B Q $\bar{Q}$ 1 1 1 0	.060	2.4 Counter becomes inhibited after first count.	2.4 Random Commands Executed	7.88	V
	2.5 U14B Q $\bar{Q}$ 0 1 0 0	.060	2.5 Flip-Flops U12A and U14A operate continuously. Gate U13A permanently high.	2.5 No Command Executed	7.88	V

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	M. Papaioan	ATM 494	
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Command Decoder			
ASS'Y	DWG NO.	DATE	
Control Logic	2367636	6-1-71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
	2.6 Low - U16A High - U16A	.120	2.6 No Gated Parity Clock	2.6 No parity check is made and command will be executed.	15.77	VI
	2.7 Low - U13C, U13A, U13B High - U13C, U11B, U13B	.228		2.7 No Command Executed	29.96	V
	2.8 Low - U11B	.028		2.8 No Command Executed in ASE Mode.	3.68	VI
	2.9 High - U13A	.024		2.9 Random commands are executed.	3.15	V
3.0 Address Recognition Gate and Counter Enable Flip-Flop: U2 U1C, U1D	3.1 Low - U2 High - U1C	.620	3.1 Counter enable F.F. will permanently enable Counter Clock input to M Counter.	3.1 Counter M and N reset lines are inhibited.	24.44	V
	3.2 High - U2 Low - U1D	.380	3.2 Counter enable F.F. permanently inhibits Counter Clock input.	3.2 Counter M will not operate.	14.98	V
4.0 Address Recognition Flip-Flop and Buffers: U3A, U3B, U3C U6A	4.1 Low - U3A, U3C High - U3B, U6A	.500	4.1 A permanent low level ADDRESS RECOGNITION SIGNAL.	4.1 Will inhibit the resetting of M and N counters.	15.77	V
	4.2 Low - U3B, U6A High - U3A, U3C	.500	4.2 A permanent high level ADDRESS RECOGNITION SIGNAL.	4.2 Will permit erratic resetting of M and N counters.	15.77	V
5.0 Uplink Shift Enable Flip-Flop: U6B, U6C	5.1 Low - U6C High - U6B	.500	5.1 Permanent low level of U6C.	5.1 No Command Executed	7.88	V
	5.2 Low - U6B High - U6C	.500	5.2 Permanent high level of U6C.	5.2 Random Commands are Executed	7.88	V
6.0 Command Verification Enable Flip-Flop and Buffer: U15B, U8C, U7D, U4C	6.1 Low - U4C, U15B High - U7D, U8C	.467	6.1 Permanent low level of VWEZP signal to Data Processor.	6.1 Partial Failure - System Will Operate	14.73	VI
	6.2 Low - U7D, U8C High - U4C, U15B	.533	6.2 Permanent high level of VWEZP signal to Data Processor.	6.2 Complete Loss of System Control Until Automatic Switchover Occurs.	16.81	V

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	M. Papaioan	ATM-949	
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ASS'Y	DWG NO.	DATE	
Control Logic	2367636	6-1-71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
7.0 Input Buffers for Shift Register Clock: U6D, U17A, U17B, U16B	7.1 Failures of U6D, U17A, U17B, and U16B.	1.00	7.1 Permanent inhibit of Shift Pulse (clock input) to Shift Register.	7.1 Shift register will not operate.	39.42	V
8.0 Shift Register and Data Input Buffer: U19, U20A, U20B, U22A, U22B, U23A, U23B, U24A, U24B, U4D	8.1 Failure - U19.	.222	8.1 Parity Flip-Flop U24A will respond to erroneous signals.	8.1 Parity Check will not function.	31.50	VI
	8.2 Failure - U20A, U20B, U22A, U22B, U23A, U23B, U24B.	.778	8.2 U2 Gate Output - Erroneous	8.2 Failure of Address Recognition	110.41	V
9.0 Parity Bit Reset Gates: U17C U17D	9.1 Failure - U17C, U17D.	1.00	9.1 Parity Bit Flip-Flop U19 "reset" and "clear" erratic.	9.1 Parity Check will not function properly.	15.77	VI
10.0 Parity Check Gates and Flip-Flop: U10C, U10D, U18C, U11C, U24A	10.1 Failure - U10C, U10D, U18C.	.529	10.1 Input to Flip-Flop U24A erratic.	10.1 Parity Check - Erratic	23.63	VI
	10.2 Failure - U11C	.118	10.2 Loss of clock input to Flip-Flop U24A.	10.2 Parity Check-Erratic	5.27	VI
	10.3 Failure - U24A	.353	10.3 Permanent inhibit of Gate U18D.	10.3 No commands executed.	15.77	V
11.0 ASE Flip-Flop and Gate: U26A, U27A, U26B	11.1 Failure - U26A, U26B.	.726		11.1 ASE commanded - Faulty Reset	20.98	VI
	11.2 Failure - U27A			11.2 System will go into ASE Data Mode and remain there.	0.83	I
12.0 Normal Reset Gates: U11D, U25A, U25B, U25C, U25D, U26C U4F	12.1 Failure - U11D, U25A, U25B, U25C, U25D, U26C, U4F	1.00	12.1 Normal Reset Operation	12.1 Master Reset, between data demand and CWE signal, is not produced.	52.56	V

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	M. Papaioan	STM 949	
END ITEM	DWG NO.	PAGE 22 of 27	
Command Decoder			
ASS'Y	DWG NO.	DATE	
Control Logic	2367636	6-1-71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
13.0 Threshold Lost Gates: U27B, U27C, U4E	13.1 Failure - U27B, U27C, U4E.	1.00		13.1 Threshold lost reset state does not operate.	21.02	V
14.0 Address Recognition Reset Gates: U27D, U11E, U11F	14.1 Failure - U27D, U11E, U11F.	1.00		14.1 Failure of ADDRESS RECOGNITION which resets M and N Counters.	18.40	V
15.0 Power Supply Decoupling Capacitors C1, C2, C3, C4, C5, C6, C7, C8	15.1 OPEN - C1, C2, C3, C4, C5, C6, C7, C8	0.90		15.1 Loss of some Decoupling on power supply line.	0	VI
	15.2 SHORT - C1, C2, C3, C4, C5, C6, C7, C8			15.2 Increased Decoupling on Power Supply Line.	7.01	
16.0 Rise Time Control Capacitors C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28 C29, C30, C31, C32, C33, C34, C35, C36.	16.1 Failure - C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36			16.1 Potential Loss of one experiment.	24.53	III

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	R. Dallaire	GTM 949	
END ITEM: Command Decoder	DWG NO.	PAGE 23 of 27	
ASS'Y: Demodulator A	DWG NO. 2367646	DATE 6-1-[illegible]	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
1.0 Input Buffer AR1, R1, R2, C1, C2, C8, VR1, VR2	1.1 Short C2, C8, Open C1, R1, R2, or Output Failure of AR1.	.188	1.1 Loss of Receiver Signal	1.1 Loss of Command Decoder A	22.63	V
	1.2 Open VR1, VR2, C2, C8, or Drift R1, R2, AR1.	.203	1.2 Degraded Received Signal	1.2 Occasional Bit Loss	24.43	VI
2.0 Phase Sensitive Rectifier: NH0019	2.1 Either Gate Failing On or Off	.90	2.1 False Inputs to the Loop (Filter)	2.1 Loss of Command Decoder A	28.38	V
	2.2 Either Gate Becomes Leaky	.10	2.2 Degraded Inputs to the Loop Filter	2.2 Occasional Bit Loss	3.15	VI
3.0 Loop Filter: R4, R5, R6, R7, R9, R12, R13, R14, C3, C7, C9, C10, C11, AR2, AR3	3.1 Open R4, R5, R6, R7, R9, R12, R13, R14, Short C3, C9, C11, C10, C7, C12, or Output Failure of AR2, AR3.	.515	3.1 Loss of Control to VCO	3.1 Loss of Command Decoder A	48.27	V
	3.2 Open C3, C7, C9, C10, C11, C12, or Drift R4, R5, R6, R7, R9, R12, R13, R14, AR2, AR3.	.479	3.2 Degraded Control of VCO	3.2 Occasional Bit Loss	44.90	VI
4.0 Voltage Controlled Oscillator: R10, R11, R15, R17, R18, C13, C14, Q1A, Q1B, Q2, Q3	4.1 Any Failure of C13, Q1A, Q1B, Q2, Open R10, R11, R15, R17, C14, Q3, or Short C14, Q3.	.880	4.1 Loss of Clock Pulses to Timing Circuitry	4.1 Loss of Command Decoder A	394.69	V
	4.2 Open R18, or Drift of R10, R11, R15, R17, Q3.	.113	4.2 Degrated Pulses to Timing Circuitry	4.2 Occasional Bit Loss	50.68	VI
5.0 Timing Circuitry: U2A, U2B, U2F, U3, U4A, U5, U6, U7A, U8A, U14B, R19	5.1 U4A = 1	.015	5.1 Possible Inability to Initialize Timing Circuitry.	5.1 Switch to Demodulator B and back again to Initialize.	2.33	VI
	5.2 Any other Failure of U2A, U2B, U2F, U3, U5, U6, U7A, U8A, U14B.	.947	5.2 Loss of Timing to Bit Detector.	5.2 Loss of Command Decoder A.	147.12	V
	5.3 Open R19	.002	5.3 Lack of Noise Immunity to Count Down Register	5.3 Occasional Bit Loss	0.31	VI

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	R. J. Dallaire	GTP 949	
END ITEM: Command Decoder A	DWG NO.	PAGE 24 of 27	
ASS'Y: Demodulator	DWG NO. 2367646	DATE 6-1-71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
6.0 4 Phase Clock Decoders: U4B, U4C, U4D, U2C, U2D, U2E	6.1 Any Failure of U4B or U2C.	.333	6.1 Loss of Clock to 3 x 7 Counters in Decoder (GCKAP).	6.1 Loss of Command Decoder A	13.13	V
	6.2 Any Failure of U4C or U2D.	.333	6.2 Loss of Parity Clock (PCKAB).	6.2 Loss of Command Decoder A	13.13	V
	6.3 Any Failure of U4D or U2E.	.333	6.3 Loss of Shift Register Clock (UCKAB).	6.3 Loss of Command Decoder A	13.13	V
7.0 Bit Detector: R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, C25, C26, VR3, VR4, U9, U10, AR4, AR5 U8C, U8D	7.1 Open R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, VR3, VR4, Short C25, C26, VR3, VR4, or any failure of AR4, AR5, U8C, U8D.	.628	7.1 Inability to detect bit stream.	7.1 Loss of Command Decoder A	224.89	V
	7.2 Open C25, C26, all resistors, or AR4, AR5.	.136	7.2 Occasional Bit Loss	7.2 Occasional Bit Loss	48.70	VI
8.0 Threshold Register: U7B U8B, U8E, U12 U13, U14A.	8.1 U17A = 0, U7B Failure During Period Uplink is Established, or U12A, U12B, U13A, U13B failing as shown: $\frac{Q \quad \bar{Q}}{1 \quad 0}$ 1 1	.510	8.1 Loss of Threshold Protection	8.1 Significant increase in false executions with uplink not established.	53.61	V
	8.2 U7B failure during period uplink is not established, U8B, U14A = 1, U8E = 0, or U12A, U12B, U13A, U13B fails as shown. $\frac{Q \quad \bar{Q}}{0 \quad 0}$ 0 1	.475	8.2 Data F.F. continually reset and TH DAN = 1.	8.2 Unable to execute commands.	49.93	VI
	8.3 U8E = 1.	.015	8.3 Data F.F. not reset with uplink unestablished.	8.3 Slightly higher chance of false execution with uplink unestablished.	1.58	VI

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	R. Dallaire	71-949	
END ITEM: Command Decoder A	DWG NO.	PAGE 25 of 27	
ASSY: Demodulator	DWG NO. 2367646	DATE 6-1-71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
9.0 Data Flip-Flop U11	9.1 Any Failure of U11.	1.00	9.1 All 1's or all 0's will be shifted into the decoder shift register.	9.1 Unable to execute commands.	31.54	V
10.0 Power Reset: R32, R33, R34, R35, C31, VR5, AR6, U8F	10.1 Open R4, Short C31, Drift AR6, U8F = 0.	.115	10.1 Reset stays continually low.	10.1 Unable to execute commands.	15.78	V
	10.2 Open C31, R32, R33, Short VR5, Drift AR6, U8F = 1.	.288	10.2 No reset occurs during power on period.	10.2 A few commands will be executed upon power turn-on the number determined by the chance initial staff of the decoder circuitry.	39.51	V
	10.3 Open VR5.	.064	10.3 Output of AR6 not limited to 5.1V, thus damaging U8F unpredicably: U8F = 1 or 0 (50 - 50 chance).	10.3 Either 10.1 or 10.2 (see 10.3 effect of failure assembly).	8.78	V
	10.4 Open R35, or Drift of AR6.	.083	10.4 Occasional Reset	10.4 Occasional Loss of a Command.	11.39	VI
11.0 Thermistor TM: R36, R37, RT1	11.1 Open R37 or Short RT1.	.004	11.1 High voltage on Telemetry Line.	11.1 Demodulator Board Temperature appears too high.	3.04	VI
	11.2 Open R36, RT1.	.096	11.2 Low Voltage on Telemetry Line.	11.2 Demodulator Board Temperature appears too low.	7.30	VI
12.0 Test Point Isolator: C6, R8	12.1 Short C6.	.205	12.1 Loss of AC isolation on TP	12.1 Possible damage to demodulator by accidental probing on the ground.	.79	VI
	12.2 Open C6, R8.	.077	12.2 Loss of signal on TP	12.2 Receiver's output appears to be non-functioning.	2.96	VI
13.0 Power Supply	13.1 Open C15, C16, C17, C18, C19, C20.	0		13.1 Loss of Decoupling on Power Supply Line	0	VI
Decoupling Capacitors C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C27, C28, C29, C30	13.2 Open C21, C22, C23, C24, C27, C28, C29, C30	0		13.2 Loss of some decoupling on power supply line	0	VI
	13.3 Short C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C27, C28 C29, C30	.381		13.3 Increased decoupling on Power Supply line	8.61	

SYSTEM ALSEP	PREPARED BY	NO. ATM 949	REV.
END ITEM Command Decoder	DWG NO.	PAGE 26 of 27	
ASS'Y Command Sequencer	DWG NO. 2367616	DATE 6-1-71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
1.0 U1B, U1D, U2A, U6B, U6C, U6D, U8A	1.1 LOW - U2A HIGH - U2A	.273	1.1 Loss of Clock Pulse to Counters.	1.1 Cannot ripple off Experiments.	15.78	VI
	1.2 LOW - U1B, U6C HIGH - U1B, U6D	.233	1.2 Clock-disabled	1.2 Cannot ripple off experiments.	13.47	VI
	1.3 HIGH - U8A	.045	1.3 Resets all counters to original state.	1.3 Cannot ripple off experiments.	2.60	VI
	1.4 HIGH - U6B	.045	1.4 Resets last five counters to zero.	1.4 Cannot ripple off experiments.	2.60	VI
	1.5 LOW - U1D	.064	1.5 Resets first three counters to one and clock disabled.	1.5 Cannot ripple off experiment.	3.70	VI
	1.6 LOW - U6B	.094	1.6 Loss of reset ability, clock.	1.6 Loss of reset ability, clock.	5.44	VI
2.0 U1C, U1D, U6C, U6D, U8A	2.1 LOW - U6D HIGH - U6C	.238	2.1 Clock continues to count.	2.1 All experiments ripple off once.	8.13	VI
	2.2 LOW - U1C HIGH - U1C, U1D	.200	2.2 Clock enabled	2.2 All experiments ripple off once.	6.83	VI
	2.3 LOW - U8A	.162	2.3 Counters cannot be reset.	2.3 All experiments ripple off once.	5.53	VI
3.0 U2B	3.1 LOW - U2B	1.00	3.1 Resets last five counters to zero and enables clock.	3.1 Count sequence repeats.	15.77	VI
4.0 U1A, U5E	4.1 HIGH - U1A	.188	4.1 Cannot clear 4th binary counter.	4.1 Ripple off count retained.	1.58	VI
	4.2 HIGH - U5E	.113	4.2 Cannot clear last 5 counters to zero.	4.2 Ripple off count retained.	0.95	VI
	4.3 LOW - U1A	.437	4.3 Clears 4th binary bit.	4.3 Interupts one count cycle only.	3.68	VI
	4.4 LOW - U5E	.262	4.4 Clears last 5 counters once.	4.4 Counters cannot be cleared again.	2.20	VI
5.0 U12A, U17A, U20A, U17B, U12B, U23A, U20B, U13A, U18A, U13B, U18B, U13C, U18C, U13D, U14A, U14B, U14C, U22A, U14D, U14E, U14F	5.1 HIGH - U12A, U17A, U20A, U17B, U12B, U23A, U20B, U14A, U14B, U14C, U22A, U14E, U14F, U14D	.409	5.1 Cannot shut off experiment output.	5.1 Experiment is commanded but has no effect.	82.76	VI

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ALSEP		70939	
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Command Decoder			
ASS'Y	DWG NO.	DATE	
Command Sequencer	367616	6-1-71	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE		(α)	EFFECT OF FAILURE		FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
				ASSEMBLY	END ITEM		
		LOW- U13A, U18A, U13B, U18B, U13C, U18C, U13D	.591				
	5.2	HIGH- U13A, U18A, U13B, U18B, U13C, U18C, U13D		5.2 Experiment output shut off.	5.2 Switches experiment to standby permanently.	119.59	III
		LOW- U12A, U17A, U20A, U17B, U12B, U23A, U20B, U14A, U14B, U14C, U22A, U14D, U14E, U14F					
6.0 U1F, U1E	6.1	LOW- U1E, U1F	1.00	6.1 Gates permanently enabled.	6.1 Experiment is commanded but has no effect.	10.51	VI
		HIGH- U1E, U1F					
7.0 Power Supply Decoupling Capacitors	7.1	OPEN C1, C2, C3, C4, C6, C7, C8, C9	0		7.1 Loss of some decoupling on power supply line	0	VI
C1, C2, C3, C4, C6, C7, C8, C9	7.2	SHORT - C1, C2, C3, C4, C6, C7, C8, C9	.90		7.2 Increased decoupling on power supply line	7.01	