CODED COMMUNICATIONS CORPORATION

TECHNICAL PROPOSAL

FOR

MULTIPLE STREAM PCM DECOMMUTATION SYSTEM

Prepared for:

The University of Texas
Marine Science Institute
Geophysics Laboratory
Galveston, Texas

1. INTRODUCTION

1.1   This proposal for a Multiple Stream PCM Decommutation System has been prepared by Coded Communications Corporation for the University of Texas, Marine Science Institute, Geophysics Laboratory.

1.2   It is understood by Coded Communications that it is desired to decommutate data presently being received from five moon stations. At Range Stations, fourteen channel tapes have this data recorded on five channels and a time code is inserted on two additional channels at the time of recording.

1.3   Coded Communications Corporation is proposing equipment in this document that will decommutate the five channels of data and the time code, present the data in an orderly means to the University of Texas PDP 15/20 Computer, and prepare a computer program that will output data to a Digital Tape Drive that will create a digital working tape of the data from the prerecorded analog tapes.

1.4   The majority of the equipment presented in this proposal is off-the-shelf with minor modifications. The equipments proposed are in use at present in systems previously supplied by Coded Communications to the government and aerospace contractors.

1.5   In order to keep costs to a minimum, Coded Communications has attempted to remove unnecessary features where practicable.

1.6   Coded Communications Corporation is a California based company dedicated to the development of PCM Telemetry and Mobile Digital Communications Equipment.

1.6.1   The products we manufacture are:

              PCM: Decommutator Systems
                              Bit Synchronizers
                              Word Selectors
                              Bit Error Test Sets
                              Encoder Checkout Units

Mobile Digital   Digital Interrogation and Display
Communications: Modems for Fleet Vehicles

                           :   Police Departments
                           :   Fire Departments
                           :   Delivery Services
                           :   Taxis
                           :   Schools

1.6.2 Typical customers:

Aacom, Inc.
Argosystems, Inc.
Atkins and Merrill
The Boeing Company
Canadian Ministry of Defence
Control Data Corporation
Edwards AFB Flight Research Center
General Electric, Mobile Radio Department
General Dynamics, Convair Aerospace Division
Government of India
Government of Israel
Grumman Aerospace Corporation
Hewlett Packard
Hughes Aircraft Corporation
ITT Federal Electric (WTR)
Leasametric
Lockheed Missiles & Space Co.
LTV
McDonnell Douglas
NASA - Ames Research Center
NASA - Goddard Space Flight Center
NASA - Johnson Space Center
Naval Research Laboratory
Naval Weapons Center, China Lake
New Mexico State University
Patrick Air Force Base (AFETR)
Philco-Ford
Quintron Systems
RCA
Rockwell International
Sandia Corporation
Sangamo Electric Company
Scripps Oceanographic Institute
Smithsonian Astronomical Observatory
Teledyne Controls
Teledyne Ryan
Teledyne Telemetry
Univac

2. SYSTEM DESCRIPTION

2.1 General. The proposed Multiple Stream PCM Decommutation System is shown in Figure I, Overall System Block Diagram. The block diagram is comprised of proposed new equipment and customer (University of Texas) furnished equipment (CFE). Optional equipment of both types is also shown.

2.2 Overall System Block Diagram. Five channels of PCM data in Manchester Code are recovered from analog range tape by the Ampex FR-2000A Analog Tape Recorder at a rate of 33.92 kbps.

2.2.1 The Ampex FR-2000A Multiband Instrumentation Recorder is a 14-track unit of which six tracks are utilized, five for data and one channel for time code. These six channels will input five each to the Coded Communications Model 7101 Decommutators and one to the Moxon Model 520 Time Code Translator. The time code is the NASA 36-bit time code, see Figure II.

2.2.2 The Coded Communications Model 7101 Decommutators perform bit synchronization, and format synchronization of the incoming bit stream. It is proposed that there will be five units plus one spare, for a total of six. Five of the decommutators will be Model 7101-4000's, which will contain only the Bit Synchronizer and Format Synchronizer with card reader control. The sixth decommutator will be a Model 7101-0100 and will contain, in addition to the above, a simulator and two word selectors. The simulator will be connected to all six decommutators through rack cabling. The data output of the decommutator is a synchronized serial bit stream inputting to the 5-Channel Multiplexer Memory.

2.2.3 The Moxon Model 520 Time Code Translator accepts standard NASA 36-bit Time Code and translates it into a parallel BCD output word in milliseconds, seconds, minutes, hours and days. This unit obtains its input from the analog tape recorder and outputs to the 5-Channel Multiplexer Memory.

2.2.4 The 5-Channel Multiplexer Memory, Coded Communications Model 7151, is a unit that organizes the five data channels for input to the PDP 15/20 Computer. Each data channel has status and time code words added to each 64 word frames of incoming data. The overall length of a frame entering memory will be 70 words. The added words contain channel identifier, status of the decommutator and time code information. Refer to Figure III, Timing Chart, for detail description of these words.

2.2.4.1 The output of the 5-Channel Multiplexer Memory is then entered into a Special Interface, part of the PDP 15/20.

2.2.5 A program will be prepared for the PDP 15/20 that will write a working tape on a Digital Tape Drive connected to the PDP 15/20. This tape will be representative of all of the input data channels with time code.
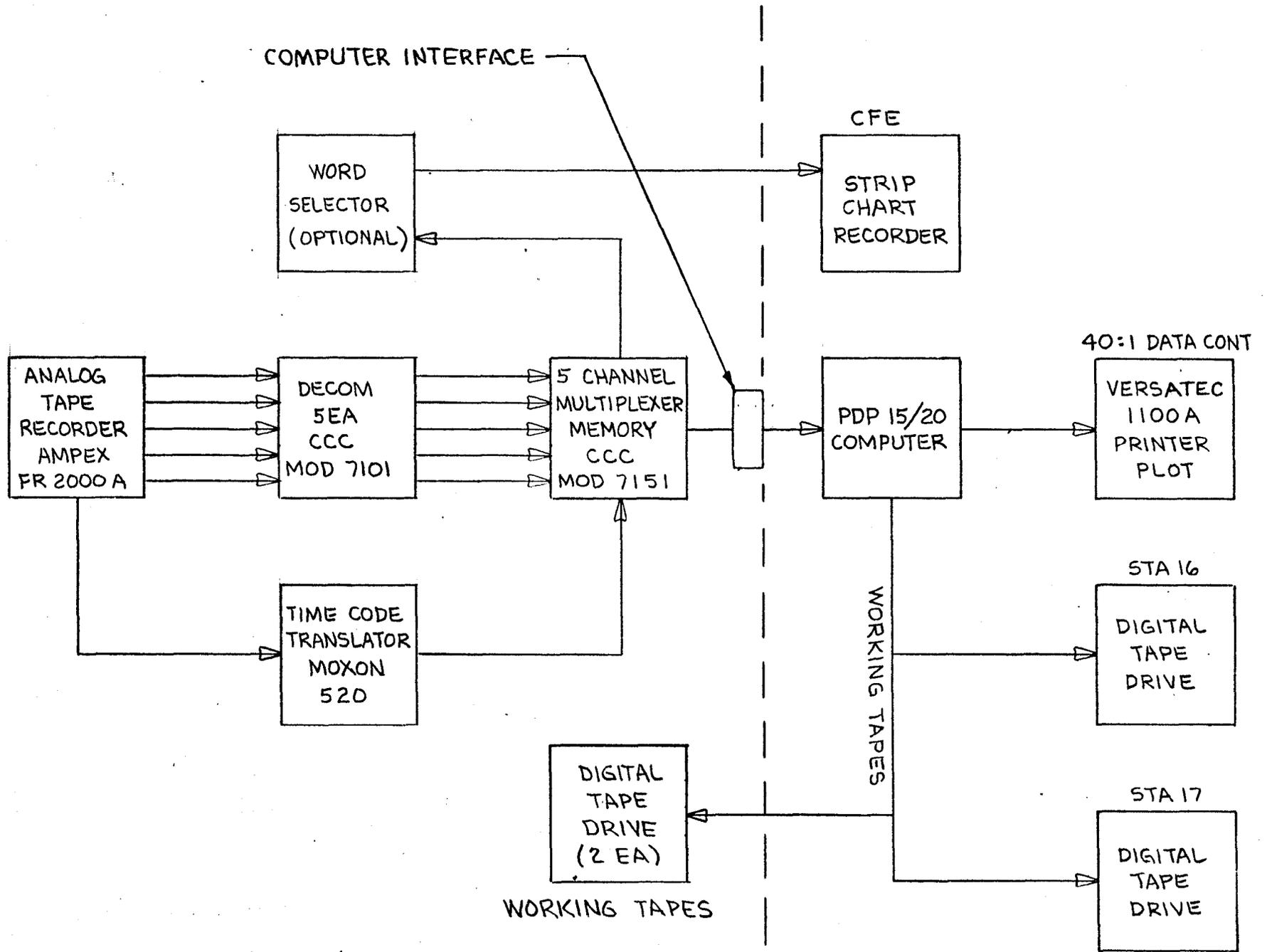
BLOCK DIAGRAM - OVERALL SYSTEM
FIGURE I

2 - 2

The NASA 36-Bit Time Code is a 100 pps pulse width modulated time code. This code may be used to amplitude modulate a 1000 cps sine wave carrier.

The code is composed of a Reference Marker and nine sub-code words, which describe time-of-year in seconds, minutes, hours and days. Each sub-code is weighted in binary-coded decimal fashion. The leading edge of all pulses are precisely spaced at 10 milliseconds intervals. The Time Frame is completed by 100 pps index markers and by index markers occurring every 100 milliseconds from 100 milliseconds to 900 milliseconds.

The frame Reference Marker is described by five binary one's followed by a binary zero. The leading edge of the binary zero is the reference time.

The Time Frame provides for the insertion of control functions for identifying the recording station.
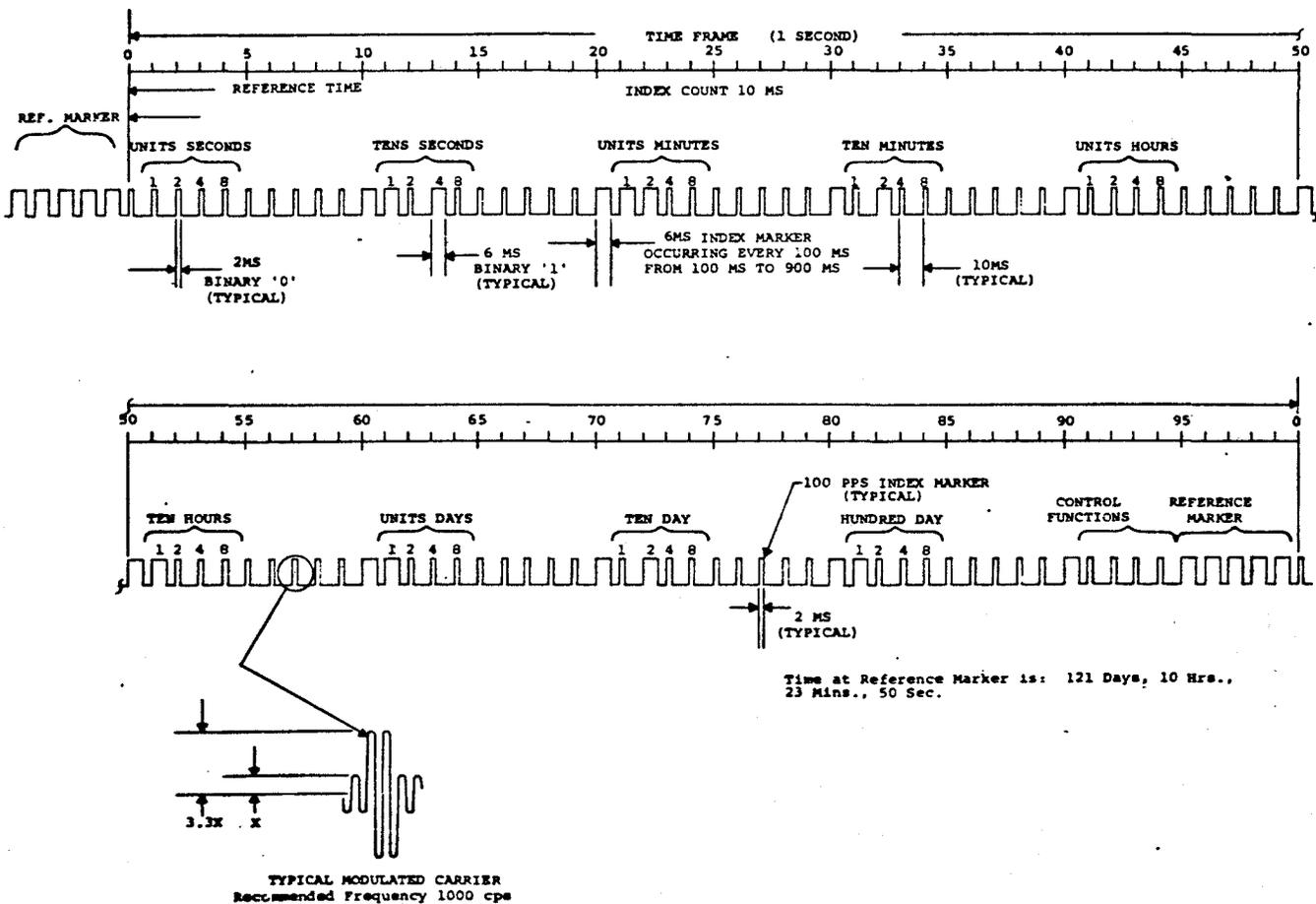
NASA 36-BIT TIME CODE—Reference IRIG Document 104-59

FIGURE II

2 - 3

Ideal Memory Output

| MEM 1 | MEM 2 | MEM 3 | MEM 4 | MEM 5 |

Beginning of Memory Group

| 1 | | 2 | | 3 | | 4 | | 5 |

Typical Memory Output

| MEM 2 | MEM 4 | | MEM 1 | MEM 3 | MEM 5 |

(70 WDS/MEM (10 BIT WDS)

| WD 1 | WD 2 | WD 3 | WD 4 | WD 5 | WD 6 | ⧓ | WD 68 | WD 69 | WD 70 |

Word Strobe (Data Ready)
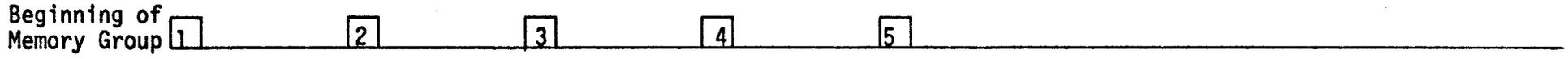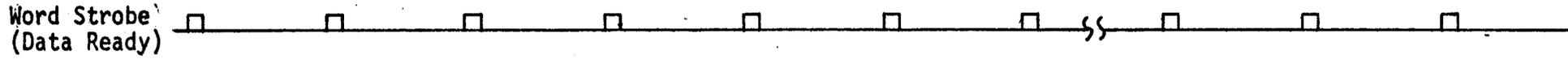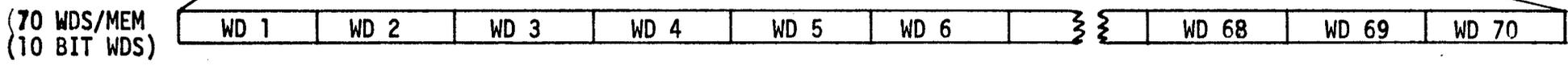
Word Identification: WORD 1 (Words are 10 bits each)

Bit 1, 2 & 3	Channel Ident	Channel		Bits 4, 5, 6 & 7	Synchronization Status
	001	1			
	010	2		Bit 8	Input Level Indicator
	011	3			
	100	4		Word 2	Not Used
	101	5			
	110	Simulator		Word 3, 4, 5 & 6	Time Code

FIGURE III - TIMING DIAGRAM

2.3   Detailed Description

2.3.1   The following paragraphs describe the detailed operation of the PCM
           Decommutator, Model 7101, and the 5-Channel Multiplexer Memory, Model
           7151.

2.3.2   The PCM Decommutator Model 7101 (refer to Figure 4) operates in
           accordance with the standard specification sheet, refer to Appendix, with
           the following exceptions.

2.3.2.1   A circuit shall be added to all decommutators that will identify the
           position of input data switch. The input data switch shall be expanded
           to five positions for incoming data plus simulator. Each switch position
           shall be assigned a channel number that directly identifies it to the
           analog tape recorder channel. This number is shown in the following
           table.

Tape Recorder Channel #	Switch Pos.	Binary ID
1	1	001
2	2	010
3	3	011
4	4	100
5	5	101
Simulator	6	110

           The binary ID will become part of the status word for each channel in the
           5-Channel Multiplexer Memory.

           The most important feature of this switch is that it allows any decom-
           mutator to be siwtched to any channel, including the spare decommutator.
           The operator must verify before starting the system that there is a
           decommutator switched to each of the five channels. In the event that
           a decommutator or portion thereof fails, the spare takes over with just
   a change in switch position.

2.3.2.2   There shall be an output connector added to the rear panel which shall
           output serial PCM data plus clock, word strobes, channel ident and status
           necessary to input the data into the 5-Channel Multiplexer Memory Unit.

2.3.3   The 5-Channel Multiplexer Memory (refer to Figure V). This unit is
           designed to increase the frame length from 64 words to 70 words and to
           output time correlated data at a higher rate than received in a format
           compatible with a PDP-15 interface.

2.3.3.1   The basic 64-word frame that is being decommutated on any one of the five
           channels is to be prefixed with six additional words. The content of
           these words is as follows.

2.3.3.1.1 Word 1 (10 bits) will contain in Bits 1 through 3, the channel identi-
           fier (refer to paragraph 2.3.2.1) plus sync status Bits 4 through 7.
           Bit 8 indicates input signal presence by monitoring the level indicator
           circuit of the Decommutators/Bit Synchronizer.
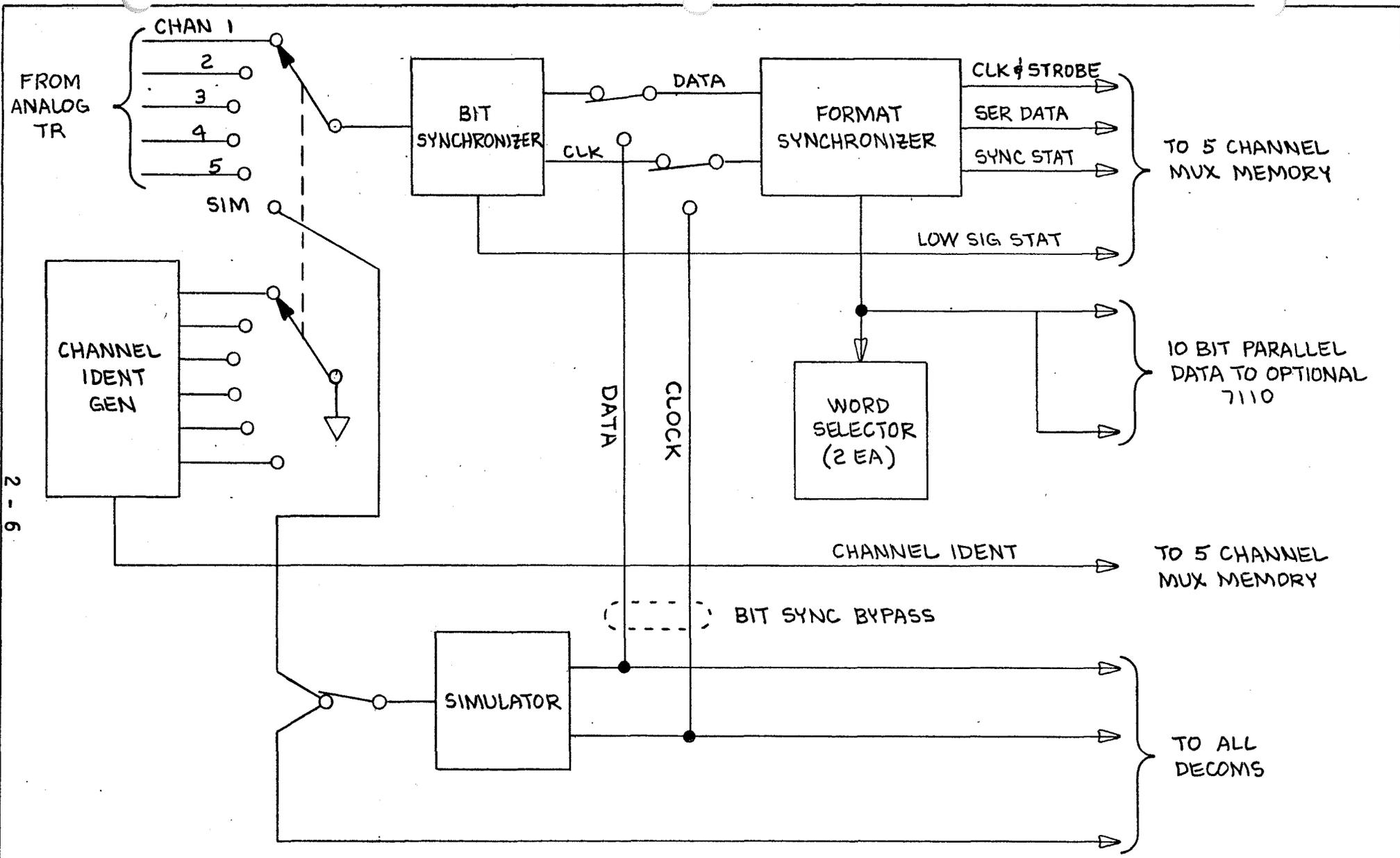
TYPICAL PCM DECOMMUTATOR BLOCK DIAGRAM

FIGURE IV

SER PCM FROM DECOM

WORDS 7-70

CLK & STRB

3×1 MUX

3×1 MUX

MEM A CHAN 1

MEM B CHAN 1

IN/OUT CONTROL

CLOCK

STATUS LINES FROM DECOM

WORDS 1 & 2

WORDS 3-6

STATUS & CHAN IDENT CODE REG

TIMING CONTROL

OUTPUT REG

OUTPUT DATA

CHANNEL IDENT FROM INPUT SWITCH DECOM

LOAD & SHIFT

IN CLK   OUT CLK   MEM LOADED

TO DMA

TO STROBE

36 BIT TIME CODE FROM TIME CODE TRANSLATOR

TIME CODE REG

MASTER TIMER

NEXT DATA FRAME READY

FROM CHANNEL 2-5

* COMMON TO ALL 5 INPUT CHANNELS

2 - 7

5 CHANNEL MULTPLEXER MEMORY BLOCK DIAGRAM (ONE CHANNEL DEPICTED)
FIGURE V

2.3.3.1.2 Word 2 is not used at present and will contain all zeros.

2.3.3.1.3 Words 3 through 6 contain the NASA 36-Bit Time Code translated by the Time Code Translator into milliseconds, seconds, minutes, hours, and time of year in BCD. The 36 bits shall be divided into four equal parts and occupy the first nine bits of each word. The 10th bit shall be a zero in all cases.

2.3.3.2 The status words 1 and 2 and the time code words 3 through 6 shall then be multiplexed into memory in their proper order.

2.3.3.2.1 When a decommutator notifies the 5-Channel Multiplexer Memory that a new frame is about to be inputted, the appropriate memory is loaded with the time code present on the time code translator input lines immediately before the first data word is loaded.

2.3.3.3 The memory is divided into two sections, A and B. Each data channel shall have its own dual memory. Theoretically Memory A for a particular channel would receive all odd numbered frames and Memory B all even numbered frames. Each individual memory will have a 1k capability.

2.3.3.3.1 Memory A shall be filling at a rate of 34 kbs approximately. When Memory A has one frame of data (70 words) inputted, Memory B shall start to fill with the second frame of data. Memory A has now signalled the master timer that it is full and ready to output data to the computer.

2.3.3.3.2 During the time Memory A of Channel One is filling, the memories of Channels Two through Five shall also be filling. Therefore, when a memory is full it must wait until the Master Timer acknowledges this fact and sequences through other filled memories, outputting only when commanded to do so.

Frames are outputted to the computer in the order in which the memory loading is completed. Therefore, the output sequence will vary occasionally due to bit rate variations.

The memories will output in accordance with the Timing Diagram, Figure III, Typical Memory Output, rather than Ideal Memory Output. The computer will recognize which channel is outputting by the Channel Ident Code in the first word of each output group. The output rate from the memory will be at a rate of approximately 255 kbs or greater. The interface will see 25.5 words/sec (based on 10-bit words).

2.3.4 Programming and PDP-15 Hardware Changes.

2.3.4.1 Interface PDP-15/20. The interface will become a part of the PDP-15/20. The interface will allow Direct Memory Access to the PDP-15/20 by the 5-Channel Multiplexer Memory. Software changes required by the PDP-15/20 to accept the interface will also be accomplished as part of the interface installation.

2.3.4.2   A Program will be prepared for the PDP-15/20 that will create a working
           tape on the 75 ips Tape Drive that represents the data being input on the
           5 channels from the analog tapes. This working tape will be in bursts
           of data with a time code preamble.

2.3.4.3   Consideration shall be given in the preparation of new routines for the
           PDP-15/20 with routines presently in use on the PDP-15/20.

2.3.5   Optional Word Selector Output. The Word Selector shall be used to sample
           asynchronous words in each data channel for conversion to analog for
           strip chart recording.

2.3.5.1   The Word Selector will accept data words from any one selected channel
           at a time. The channel ident (refer to Paragraph 2.3.2.1) will be
           decoded by the channel selector on the Word Selector. Words from the
           selected channel that is desired to output to the strip chart recorder
           will have their word position preprogrammed into a PROM. The PROM will
           cause these words to be sent to the appropriate D/A for conversion.

2.3.5.2   There will be a separate PROM in the Word Selector for each of the four
           channels. If it is desired to select a different group of words in a
           channel, a new PROM will have to be programmed on a PROM programmer,
           and inserted in its proper location in the Word Selector.

2.3.5.3   There will be 4 channels of analog outputs available. Any of the
           following outputs may be specified by the University of Texas, Geo-
           physics Lab at the time of purchase.

                        0 to +10 volts
                        + 5 volts   @ 5 ma
                        + 10 volts

   or adjustable + 1 volt to + 10 volts, 100 ma.

2.4   Physical Characteristics.

2.4.1.1   The proposed equipment as described herein will be housed in a two-bay
           cabinet assembly, refer to Figure VI. The approximate dimensions are:

                        Height   63"
                        Width   46"
                        Depth   24"

2.4.1.2   The Ampex FR-2000A Multichannel Instrumentation Recorder is housed in
   its own single cabinet, the dimensions of which are:

                        Height   77-1/4"
                        Width   23"
                        Depth   25"

BLANK		BLANK
DECOMMUTATION SYSTEM CODED MODEL 7101-0100		TIME CODE TRANSLATOR MOXON MODEL 520
DECOMMUTATION SYSTEM CODED MODEL 7101-4000		FIVE-CHANNEL MULTIPLEXED MEMORY CODED MODEL 7151
DECOMMUTATION SYSTEM CODED MODEL 7101-4000		WORD SELECTOR CODED MODEL 7110 ✳
DECOMMUTATION SYSTEM CODED MODEL 7101-4000		BLANK
DECOMMUTATION SYSTEM CODED MODEL 7101-4000		
DECOMMUTATION SYSTEM CODED MODEL 7101-4000 ✳		
POWER CONTROL		POWER CONTROL
BLOWER		BLOWER

✳ OPTIONAL

MULTIPLE STREAM
PCM DECOMMUTATION SYSTEM

FIGURE VI

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┌─────────────────────────────────┐
│  ┌───────────────────────────┐  │
│  │     TAPE CONTROLLER       │  │
│  │                           │  │
│  │   DATUM MODEL 5091        │  │
│  ├───────────────────────────┤  │
│  │                           │  │
│  │                           │  │
│  │        DIGITAL            │  │
│  │         TAPE              │  │
│  │       RECORDER            │  │
│  │                           │  │
│  │                           │  │
│  │    BUCODE MODEL 4025      │  │
│  │                           │  │
│  ├───────────────────────────┤  │
│  │                           │  │
│  │        DIGITAL            │  │
│  │         TAPE              │  │
│  │       RECORDER            │  │
│  │                           │  │
│  │                           │  │
│  │    BUCODE MODEL 4025      │  │
│  │                           │  │
│  ├───────────────────────────┤  │
│  │     POWER CONTROL         │  │
│  ├───────────────────────────┤  │
│  │                           │  │
│  │        BLOWER             │  │
│  │                           │  │
│  └───────────────────────────┘  │
└─────────────────────────────────┘
```
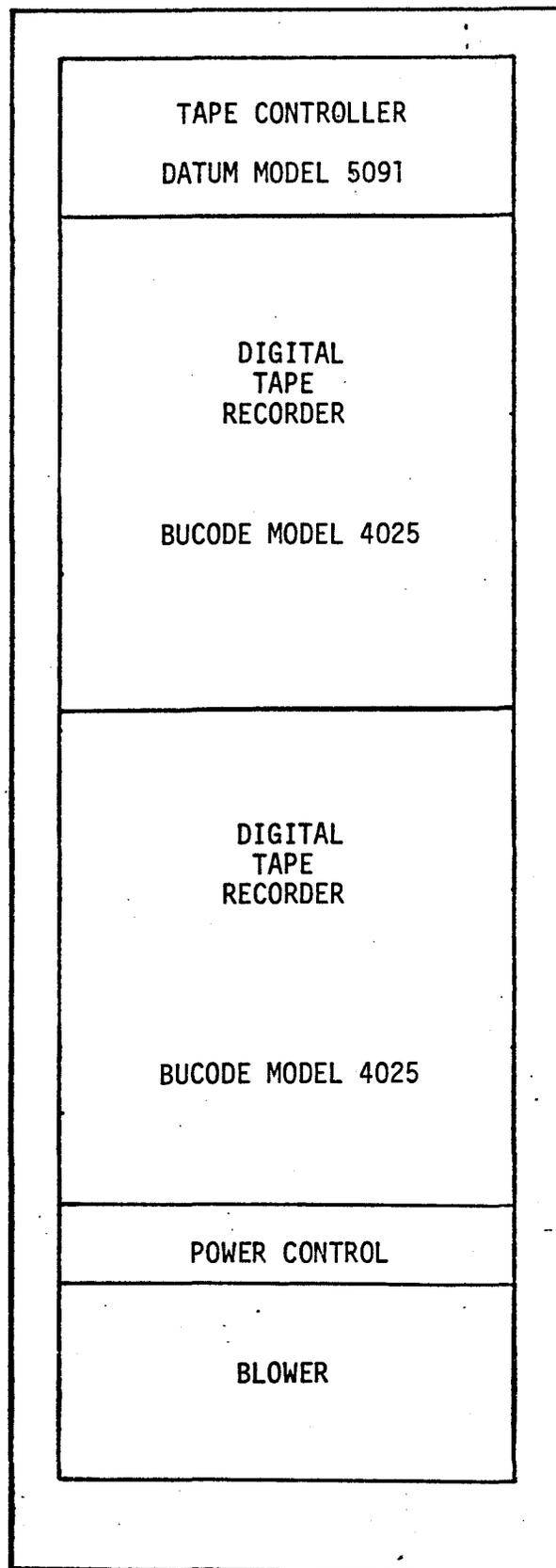
DIGITAL TAPE RECORDER

FIGURE VI a

2-11

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┌─────────────────────────────────────────┐
│  ┌───────────────────────────────────┐  │
│  │                                   │  │
│  │           MULTIBAND               │  │
│  │        INSTRUMENTATION            │  │
│  │          RECORDER                 │  │
│  │                                   │  │
│  │                                   │  │
│  │      AMPEX MODEL FR-2000          │  │
│  │                                   │  │
│  │                                   │  │
│  │                                   │  │
│  │                                   │  │
│  ├───────────────────────────────────┤  │
│  │         POWER CONTROL             │  │
│  ├───────────────────────────────────┤  │
│  │                                   │  │
│  │           BLOWER                  │  │
│  │                                   │  │
│  └───────────────────────────────────┘  │
└─────────────────────────────────────────┘
```

ANALOG TAPE RECORDER

FIGURE VI b

2-12

3.   DOCUMENTATION

3.1   Acceptance Test Procedure (ATP) - An ATP will be provided for selloff of
        the system at the University of Texas. This will include a demonstration
        of the equipment producing a working tape from analog range tapes.

3.2   Manual - A system instruction manual covering the individual units within
        the overall system will be provided. The system manual will cover system
        operation, parts lists and schematic diagrams.

APPENDIX I

INDIVIDUAL EQUIPMENT SPECIFICATION SHEETS

CODED COMMUNICATIONS

PCM DECOMMUTATION SYSTEM
MODEL 7101
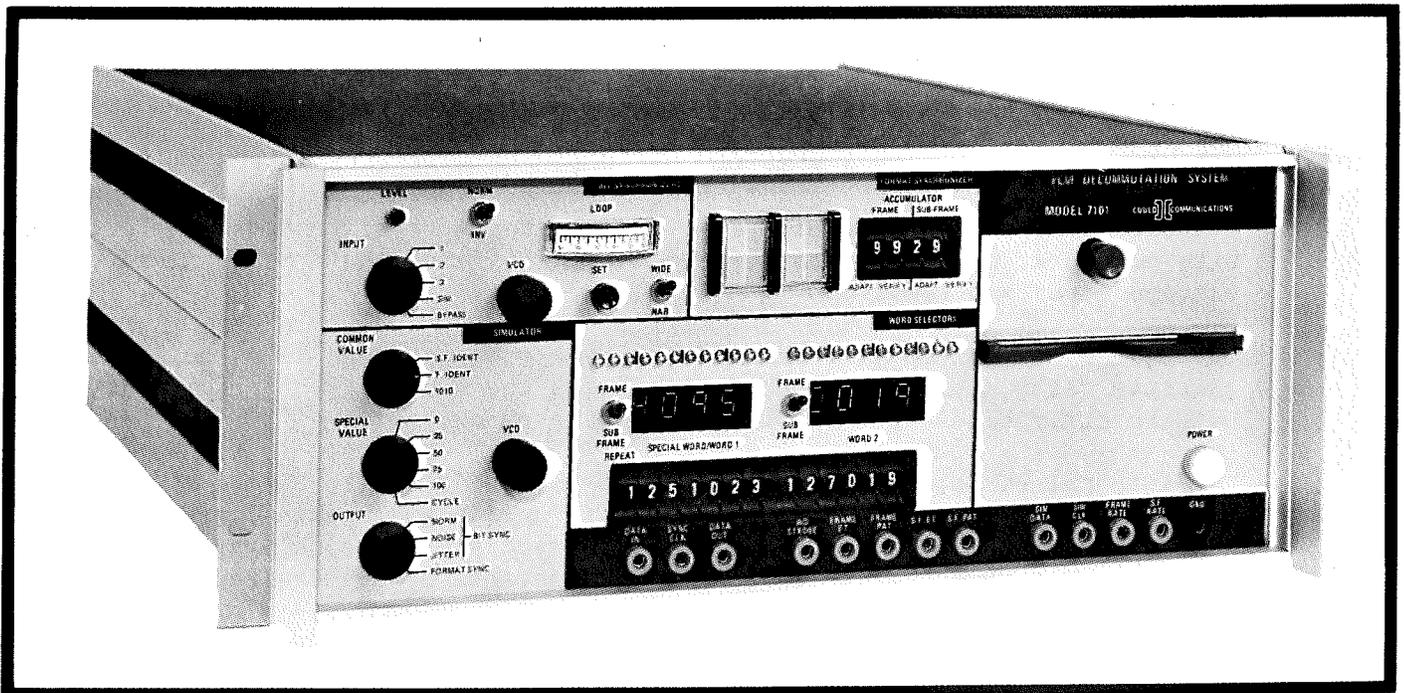
FEATURES:

- Punch Card Programmable Bit Rates and Formats
- Adaptive Frame and Subframe Synchronization
- Full Computer Control Option
- Simulator with Internal Noise Source
- Two Word Selectors with Analog and Binary Displays
- Automatic Data Ambiguity Resolution
- Computer Compatible Outputs
- Decimal Selection of Words Regardless of Format Structure

APPLICATIONS:

- The Model 7101 PCM Decommutation System is completely punch card programmable, providing bit, frame and subframe synchronization and serial to parallel conversion. In addition to these normal functions, the unit also contains a fully programmable PCM Simulator and two Thumbwheel Word Selectors.

- Real Time and Playback Data Monitoring and Stripout

- Data Alignment for Computer Input

- PCM Encoder and Telemeter Testing

BIT SYNCHRONIZER SPECIFICATIONS (Continued)

INPUT LEVELS: 0.5 volts to 15 volts peak-to-peak without adjustment. Signals up to 40 volts p-p will not damage unit.

INPUT DYNAMIC RANGE: Full range (30:1) without adjustment.

*BIT CODE FORMAT: NRZ-L, -M, -S, Bi-Phase-L, -M, -S, RZ and DM.

INPUT POLARITY: Normal or inverted, front panel switch selectable. For "L" codes, ambiguity may be resolved by punch card programming which utilizes sync pattern polarity.

BIT DETECTION: Integrate and reset method. Utilizes full bit period for NRZ and Bi-Phase integration.

LOOP RESPONSE: Front panel switch selection of 0.2% (Narrow), and 2.0% (Wide) of the octave center bit rate clock. (4.0% available upon request).

BASE LINE SHIFT: Data baseline may be shifted by a super-imposed triangular waveform with an amplitude of up to 100% peak-to-peak signal level; with a frequency of up to 0.1% of the nominal data clock rate, and minimum transition density of 50%. Maximum excursion of shifted data is ±10.0 volts.

ACQUISITION: Within 100 bit periods for NRZ data with maximum transitions and 15 db signal to noise, with noise filtered at the bit rate.

TRANSITION DENSITY: Up to 64 consecutive, transitionless bit periods with a loop width of 0.2%, 15db S/N ratio with noise filtered at the bit rate, without loss of synchronization (defined as ±1 clock cycle in 10,000 bit periods).

CAPTURE: Capture signal within ±5% of bit rate with wide loop filter, and within ±2% of bit rate with narrow loop filter.

TRACKING: Tracks signal over ±5% of preset bit rate.

BIT JITTER: Non cumulative ±20% displacement of bit period from nominal position; rate not in excess of nominal Bit Rate.

BIT ERROR PROBABILITY: No greater than:

S/N RATIO (db)		Bit Error Probability
1KB-1.5MB	1.5MB-2MB	
6	8	4×10^{-2}
9	12	6×10^{-3}
12	15	2×10^{-4}

3

*WORDS (SYLS) PER FRAME: Up to 512 words or syllables per frame.

*FRAMES (WORDS) PER
          SUBFRAME: Up to 512 frames (or words) per subframe with Frame Code Complement (FCC) or Unique Recycling Code (URC). Up to 256 frames (or words) per subframe with 8-bit Subframe Identification (SFID).

*FRAME SYNC PATTERN: Up to 32 bits with any combination of "1"s and "0"s. Pattern may be static (remains the same in all frames), or may be Frame Alternating Complement (FAC – pattern is complemented in alternate frames).

*SUBFRAME SYNC PATTERN: Frame Code Complement (FCC):
        The Frame Sync Pattern is complemented in one frame, at the longest subframe cycle rate.

    Unique Recycling Code (URC):
        A Unique Pattern, of up to 32 bits is inserted in one frame, in any word position at the subframe cycle rate.

    Subframe Identification (SFID):
        Up to 8 successive bits contain a binary number, incrementing to, or decrementing from a binary number appropriate to the number of frames per subframe. Incrementing first count may be a "1" or "0"; decrementing last count, "0" only. Most Significant Bit (MSB) first for incrementing count and Least Significant Bit (LSB) first for decrementing count.

WORD ALIGNMENT: Most Significant Bit (MSB) first. (LSB first processing optional).

*PARITY CHECK: Checks for either even or odd parity if contained in format in LSB position. Outputs parity check status with each parallel data word.

*PARITY GENERATION: If parity is not contained in format, the unit will generate a parity bit (either odd or even) for each output parallel word.

*SYNC APERATURE: 1 or 3 bits.

*PARALLEL DATA OUTPUTS: Up to 16 bits.

*DATA OUTPUT INHIBIT: Data output load pulses may be inhibited during the word times that Frame Sync is present in the data output register.

SYNCHRONIZATION MODES: Unit utilizes adaptive sync strategy with five modes of operation.

Subframe synchronization commences after the frame sync has entered the Verify/Search Mode. At this time the frame location of subframe sync is known. The unit therefore investigates this location for the proper subframe pattern on a frame-by-frame basis. Operation for FCC and URC is similar to that accomplished in the frame sync modes.

SUBFRAME IDENTIFICATION (SFID:

Search Mode:	After the unit enters the Frame Verify/Search Mode, the pattern contained within the SFID location is stored and the frame counter is updated to this count. The unit then advances to the Subframe Verify/Search Mode.
Verify/Search Mode:	Each time the frame pattern is recognized, the frame counter is updated one count. With the appearance of the SFID count, the frame counter is compared with it. If they are identical, an accumulation of such comparisons is made to the number specified on the Subframe Verify/Search Accumulator thumbwheel. The unit then enters the Subframe Lock Mode. If during this accumulation, one SFID count containing one or more bit errors appears, the unit returns to the Search Mode.
Lock Mode:	In the Lock Mode the unit compares the internal frame counter against the data SFID in each frame. If they are identical, the unit remains in Subframe Lock. If they are dissimilar, the unit enters the Subframe Verify/Lock Mode.
Verify/Lock Mode:	In the Subframe Verify/Lock Mode the unit compares the internal count against the data SFID pattern. Accumulation of dissimilar patterns takes place to that specified on the Subframe Verify/Lock Accumulator thumbwheel. If this number is reached the unit reverts to the Search Mode. If during this accumulation, one perfect data SFID pattern appears, the unit re-enters the Lock Mode.
*OUTPUT DATA MASK:	Output data register may be masked to the basic word (syllable) length.

OUTPUTS:

Data Word (Syl.):	Parallel data of up to 16 bits.
Format Sync. Strobe:	End of Word (EOW). End of Frame (EOF). End of Subframe (EOSF).
Format Sync. ID:	Frame ID (binary, 9 lines)

FORMAT SYNCHRONIZER SPECIFICATIONS   (Continued)

Special Word/Word 1:   Six thumbwheels specify selected word for display
and also specify simulated special word location.
A seventh thumbwheel (not associated with word
selection) specifies the number of successive
words in which the special word is to be inserted.

PCM SIMULATOR SPECIFICATIONS:

*FORMAT GENERATION: Generates identical PCM Format to which the For-
mat Synchronizer is punch card programmed including
bit rate, bit code, word, frame and subframe
lengths, sync types and patterns.

*BIT RATE: From 1 Kilobit to 2.0 Megabits per Second NRZ
and 500 BPS to 1 MBPS RZ, Bi-Phase and DM to
within 3% by punch card. Front panel fine ad-
justment.

SPECIAL WORD INJECTION: One special word value may be inserted in the
format in any word location in the Frame or Sub-
frame. The location of this word is determined
by six thumbwheels (shared with one of the data
select words). A seventh thumbwheel allows re-
peating this special value on a consecutive
basis for up to 9 words. The repeat feature
utilization includes testing of bit synchronizers
over periods of consecutive non-transient NRZ data.

SPECIAL WORD VALUE: One of the following values may be placed in the
special word location:

1.   000.0% Data (All"0"s)
2.   025.0% Data
3.   050.0% Data
4.   075.0% Data
5.   100.0% Data
6.   Cycle: Johnson counter contents are inserted
     into special word at longest cycle rate. If
     the format contains frames only, the count
     will be incremented at the frame rate. If the
     format contains subframes, the count will be
     incremented at the longest subframe.

COMMON WORD: All words which do not contain the special word
value or a sync pattern will contain the common
word value.

COMMON WORD VALUES:

SF Ident.:   The word contains the binary equivalent of the
frame (or word) number in the subframe.

F Ident.:   The word contains the binary equivalent of the
word position in the frame.

9

PHYSICAL SPECIFICATIONS

SIZE: 7.0 inches high, 20 inches deep. 19 inch relay
                     rack mounting.

WEIGHT: Not more than 45 pounds.

POWER: 117 VAC ±10%, 47 to 63 Hz at 1.5A.

COLOR: Gray, #26440 per Fed Std 595, with black lettering.
                     Other colors available at extra cost.

ENVIRONMENTAL SPECIFICATIONS

TEMPERATURE: Operating: 0°C to $+55^{\circ}$C.
                     Non-Operating: -35°C to $+70^{\circ}$C.

HUMIDITY: Operating/Non-Operating: 0% to 90%, Non-Condensing.

ALTITUDE: Operating/Non-Operating: -2000 feet to +15,000 feet.

COOLING: No cooling necessary over specified temperature range.

CODED COMMUNICATIONS

PCM WORD SELECTOR

MODEL 7110
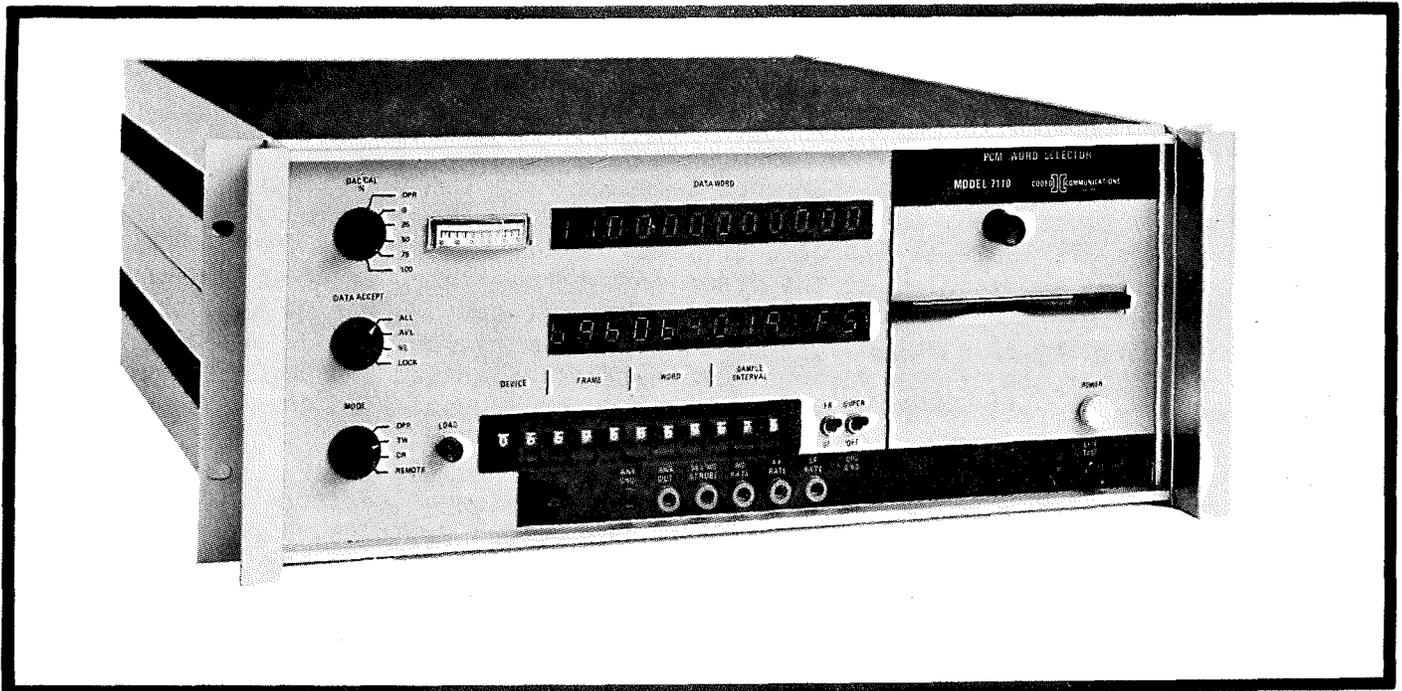
FEATURES

32 Channel Word Selection

Punch Card Programmable

Decimal Thumbwheel Selection

Analog and Binary Data Display

Super- and Sub-Commutated Word Selection

8, 10, or 12 Bit D/A Conversion

Up to 100ma Output Available

Computer Control Option

Memory Content Display

10 Bit Lamp Drivers Available

APPLICATIONS

Quick look and stripchart recording of analog and digital PCM words.

Dynamic closed loop data analysis under computer control.

Discrete event monitoring and recording.

Data word through-put for computer entry.

Word selection and control for printer interface.

MODEL 7110 ELECTRICAL SPECIFICATIONS

Unless otherwise specified a binary "1" = +4.0 ±1.0 volt and a binary
"0" = +0.4 ±0.4 volt.

INPUTS

WORD RATE STROBE: (EOW)	A one-bit wide "1" pulse, coincident with last bit of each word time.
FRAME STROBE: (EOF)	A one-word wide "1" pulse, coincident with the last word of each frame.
SUBFRAME STROBE: (EOSF)	A one-frame wide "1" pulse, coincident with the last frame of each subframe.
FRAME IDENT, START:	If first frame in subframe is identified as "one", this line should be held at a "1" level, if first frame is identified as "zero", this line should be held at a "0" level.
SYNC STATUS MODE:	4 input lines are available for sync status mode signals for use in inhibiting loading strobes during Search, Adapt, and Verify Modes.
PARALLEL DATA:	Up to 12 parallel data lines.

WORD SELECTION

THUMBWHEELS:	The entire unit may be programmed by the thumbwheels, one word at a time. 11 Thumbwheels specify output device, word and frame indent, and supercom sample interval.
CARD READER OPTION:	Any group of eight words may be programmed on a single punch card by specifing the format ident and sample interval of each data word. The first word ident is loaded into memory as specified on the device thumbwheels. The remaining seven word indents are then loaded sequentially into the next seven consecutive device locations. The punched card is not used as memory, and is therefore removed after group loading. The second, third, and fourth groups of words are loaded in a similar manner.
COMPUTER CONTROL OPTION:	The memory may be loaded from an external device such as a computer, through an interface. Selected word strobe outputs are available for pre-selected data processing applications.
DATA ACCEPT	The unit will accept data and update the D/As and lamp displays only in the sync status modes desired by the operator. Front panel selectable as follows:
ALL:	The unit accepts data during all modes.

Output Voltages:	Option	Voltage for all "1"s	Voltage for all "0"s
	1	+10 volts	0 volts
	2	+ 5 volts	-5 volts
	3	+10 volts	-10 volts

Capacitive Load: 1000 pF.

DC Output Impedance: 0.1 ohm.

Full Scale Adjustment: ±10%.

Offset Adjustment: ±40 mV.

OUTPUTS, HIGH DRIVE D/A:

Output Drive: 100 mA, short circuit proof.

Output Voltage: Adjustable from ± 1.0 Volts FSR to ± 10.0 Volts FSR. (Minus voltage = all "0"s, Plus voltage = all "1"s)

Capacitive Load: 10,000 pF.

DC Output Impedance: Less than 0.1 ohm.

Full Scale Adjustment: ±1.0 volts to ±10.0 volts.

Offset Adjustment: ±4 mV to ±40 mV.

LAMP DRIVERS   Lamp drivers provide 10-bit outputs for each word selected.

STANDARD OUTPUT: "1" = +4.0 ±1.0 volt, "0" = +0.4 ±0.4 volt.

SPECIAL OUTPUT: The following open collector transistor output is available on special order:

"1" = 0.0 volt, sink -40 mA, "0" = Hi V, Max 30 V.

INPUT SIGNAL BUFFERS: All input signals are buffered and are available for driving additional word selectors.

FRONT PANEL CONTROLS

POWER: 2-position toggle switch.

DATA ACCEPT: 4-position rotary switch.

CALIBRATE: 6-position rotary switch.

MODE: 4-position rotary switch.

LOAD: Momentary pushbutton.

DEVICE: Two, 10-position thumbwheel switches.

WORD SELECT: Nine, 10-position thumbwheel switches.

FRAME/SUBFRAME: 2-position toggle.

Output Voltages:	Option	Voltage for all "1"s	Voltage for all "0"s
	1	+10 volts	0 volts
	2	+ 5 volts	-5 volts
	3	+10 volts	-10 volts

Capacitive Load: 1000 pF.

DC Output Impedance: 0.1 ohm.

Full Scale Adjustment: ±10%.

Offset Adjustment: ±40 mV.

OUTPUTS, HIGH DRIVE D/A:

Output Drive: 100 mA, short circuit proof.

Output Voltage: Adjustable from ± 1.0 Volts FSR to ± 10.0 Volts FSR.
(Minus voltage = all "0"s, Plus voltage = all "1"s)

Capacitive Load: 10,000 pF.

DC Output Impedance: Less than 0.1 ohm.

Full Scale Adjustment: ±1.0 volts to ±10.0 volts.

Offset Adjustment: ±4 mV to ±40 mV.

LAMP DRIVERS   Lamp drivers provide 10-bit outputs for each word selected.

STANDARD OUTPUT: "1" = +4.0 ±1.0 volt, "0" = +0.4 ±0.4 volt.

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MODE: 4-position rotary switch.

LOAD: Momentary pushbutton.

DEVICE: Two, 10-position thumbwheel switches.

WORD SELECT: Nine, 10-position thumbwheel switches.

FRAME/SUBFRAME: 2-position toggle.

MODEL 7110 ORDERING INFORMATION

The 7110 Model Number is followed by a 7-digit standard option number which specifies which options are desired.

MODEL - OPTION DIGITS
7110 - 12345678

Basic Unit 7110 - 00000000 (Provides 32 strobes for computer)

DIGIT NUMBER OPTION ORDERING INFORMATION

1   CARD READER. If desired enter "1", if not desired enter "0".
2   COMPUTER CONTROL. If desired enter "1", if not desired enter "0".
3   NUMBER OF D/A CONVERTERS. Packaged four per D/A Board. Enter the number of boards desired as follows:

Number of D/As	Enter in Digit 3
0	0
4	1
8	2
12	3
16	4
20	5
24	6
28	7
32	8

4   D/A DRIVE. 5 mA (or if no D/As) enter a "0". 100 mA, enter a "1".

5   D/A VOLTAGE.

| VOLTAGE	Enter in Digit 5
If Digit 4 is a "0":	
No D/As Desired	0
0 to +10 Volts	1
± 5 Volts	2
± 10 Volts	3
If Digit 4 is a "1":	
Adjustable ±1 Volt to ± 10 Volts	3

6   NUMBER OF LAMP DRIVERS. Packaged four per LD board. Enter the number of boards desired in a similar manner to the D/A boards. NOTE: The sum of the numbers entered in digits 3 and 6 must not exceed a total of 8 (Maximum number of boards possible in unit).

7   DECIMAL DISPLAY. If desired enter "1", if not desired enter "0".

8   PRINTER INTERFACE: If desired enter "1", if not desired enter "0". (Interface requires 4 board locations.)

SRC

TRANSDUCERS □ SYSTEMS □ INSTRUMENTS

MOXON INC.
SRC DIVISION

TIME CODE TRANSLATOR

MODEL 520
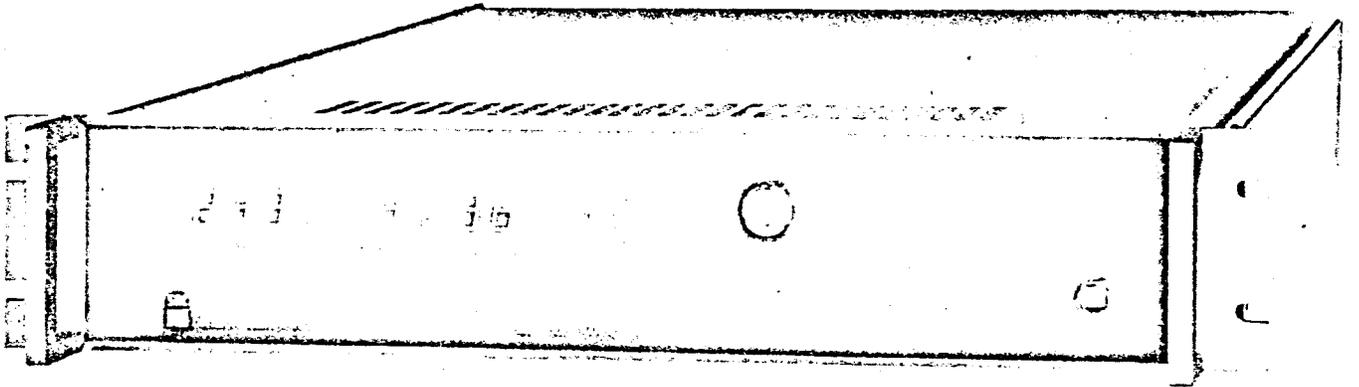
FEATURES:
RELIABLE TTL LOGIC ELEMENTS
"DAYS" DISPLAY STANDARD
AUTOMATIC GAIN CONTROL INPUT CIRCUITRY
WIDE BANDWIDTH, HIGH SENSITIVITY
PARALLEL AND PULSE OUTPUTS STANDARD
LARGE SELECTION OF OPTIONS AND ACCESSORIES AVAILABLE
MODULAR PLUG-IN CIRCUITS — NO "MOTHER BOARDS"
OUTSTANDING READABILITY — SPERRY GAS DISCHARGE DISPLAY
WIRE-WRAP INTERCONNECTION — EASILY EXPANDED OR MODIFIED
TRANSLATES ANY TIME CODE FORMAT
LOW COST BUY — ONLY — WHAT — YOU — NEED
EXTENSIVE LIBRARY OF PLUG-IN "OFF THE SHELF" FUNCTIONS

STANDARD UNIT FEATURES

1. IRIG B 123 Seconds thru Days Input
   - 1.1 100 mv to 15V p/p
     50 Hz to 20 kHz B/W
2. Forward Direction Translation

3. Parallel BCD (S,M,H,D) (30 Bits)

4. 1K, 100, 10, 1 Hz Pulse Rates.
5. 9 Digit (S,M,H,D)

OPTIONAL FEATURES

1. Any standard and Most Special Codes
   - 1.1 20 mv to 50V p/p
     1MHz B/W
2. Forward/Reverse Translation, Automatic Polarity Switching, Error By-Pass
3. 17 Bit Binary Seconds, Grouped Binary.
4. Many Special Pulse Rates available.
5. Other Decades (.1 sec) STOD, etc.
   Control Function Decode
   Error By-Pass (Sync Mode)
   Filters
   Generator Mode
   Slow Code Output 9 Rate
   Computer Interface
   Tape Search Interface

Many other special features available
to adapt to your unique requirements.

GENERAL DESCRIPTION

Designed for use in computer or data reduction systems where Time Codes are to be read from magnetic tape or other sources. The Model 520 is capable of translating all standard time codes. The instrument may be configured to translate many unique codes.

Single-Cycle drop-out protection is provided in the digital decoding process. The noise or the drop-out of a single cycle or less,of the carrier frequency occurring on the input,will not affect the decoding process or the output information.

The front panel display is useful as a guide while manually re-positioning the tape prior to data reduction. The 520 is easily mated to a Model 524 Tape Search and Control Unit to form a completely automatic tape search system when the Forward/Reverse Translate option is specified.

Parallel and Serial outputs in many formats and levels are available to allow maximum system integration and usage. These optional outputs may be specified at the time of order or are easily added as field modifications. Extensive use of field proven TTL, SSI, and MSI silicon integrated circuitry in the Model 520 insures efficient and reliable operation. All circuitry is mounted on plug-in circuit boards, with edge-mounted test points providing easy access to critical points in the circuitry.

SPECIFICATIONS
Basic Unit:

Input Time Code	IRIG "B" 123
Automatic Gain Control	100 Millivolts to 15 volts peak-to-peak dynamic range during mark condition within a bandwidth of 50 Hz to 20 kHz.
Parallel Outputs	Days, Hours, Minutes, and Seconds (30 Bits BCD 8-4-2-1 Code)
Binary Zero	±0.5 VDC (25 mA to Ground)
Binary One	≥+2.5 VDC into 15 TTL Loads (+5.0 VDC from 3.9K ohm Source)
Rise and Fall Times	Less than 1 microsecond
	All outputs are short circuit proof and are available at a rear panel multi-pin connector.
Pulse Rate Outputs	1 Hz, 10 Hz, 100 Hz and 1 kHz 20% duty cycle available at a rear panel multi-pin connector. Trailing edge "ON TIME." Voltage levels are the same as specified for the parallel outputs. Complementary outputs are available in lieu of the above at no charge.
Physical Description	
Visual Display	Decimal-Days: Hours: Minutes: Seconds Display utilizing Sperry long-life, planar gas discharge readouts.
Controls	All standard operating controls are located on the front panel.
Power	115/208/230V, 50-70 Hz, Single Phase, 380-440 Hz optionally available 35 Watts Nominal
Cooling	Forced Air from Integral Fan for 50-70 Hz Operation
Size	3-1/2" High, 19" Wide, 21" Deep (Including Mating Connectors)
Weight	35 lbs. Nominal

Environmental
    Operating Temperature   0° to +50°C
    Storage Temperature   -65°C to +85°C
    Humidity   95% Relative without condensation.

NOTE: Other operating environments are available on request.

Manuals
One copy of SRC's Standard Instruction Manual is furnished at no charge with each unit.

Mating Connectors
All Multi-pin mating connectors are included.

OPTIONAL FEATURES

Slow Code
A serial slow code Type B for oscillograph and strip chart recordings. Frame rates vary from one per second to one per hour in nine switch selectable steps.

Amplitude
Binary zero "0" = +6 volts
(Nominal into 100 ohms to ground)

Binary one "1" = +10 volts
(Nominal into 100 ohms to ground)

Parallel Outputs

    Type 1
Hours, Minutes, Seconds, Milliseconds (32 Bits BCD)

    Type 2
Days, Hours, Minutes, Seconds, Milliseconds (42 Bits BCD)

    Type 3
Group Binary — Hours, Minutes, Seconds, (5,6,6 Bits)

    Type 4
Group Binary — Days, Hours, Minutes, Seconds (9,5,6,6 Bits)

    Type 5
10 Bits Binary Milliseconds

    Type 6
17 Bits Binary Seconds Time-of-Day

    Type 7
14 Bits Binary Tenths milliseconds.

All parallel outputs and pulse rates may be supplied in complementary form.

    Logic Levels
As specified for standard parallel outputs. Other Logic Levels available.

    Sample Inhibit
All parallel outputs can be supplied with a sample inhibit pulse which begins approximately 1μ sec before t_o and lasts approximately 2μ sec after t_o to indicate to external devices when data is changing.

    Buffer Register
The parallel outputs may be provided through a buffer register. This register may be loaded by internal or external commands. When this option is taken, an inhibit pulse is provided to indicate when the contents of the register are changing.

Two way communication between the buffer register and the external sampling device is also optional. In this configuration the buffer may be sampled asynchronously.

Reverse Translate

Reads input code in reverse, as well as forward direction. Reverse command and input code polarity are selected by front panel toggle switches. Direction sensing is automatic when connected to the Model 524 Tape Search and Control Unit. AGC Option #1 and Error By-Pass are also provided.

Automatic Polarity Selection

Eliminates polarity setting errors without the need of operator attention.

Carrier Filters

Bandpass filters may be selected by two front panel switches. One switch selects the proper filter for the desired playback speed. The other switch selects the proper filter for the desired search speeds. Playback or search filter setting is selected automatically when used in conjunction with the Model 524 Tape Search and Control Unit. An additional position on each switch permits by-passing the filter section.

Tape Search Interface

This option provides interface to the Model 524 Tape Search and Control Unit for automatic tape search operation. The 524 then automatically sends forward and reverse commands and filter selection to the Model 520.

AGC (Option)
Supplied when FORWARD/REVERSE
Translation is specified

20 millivolts to 50 volts peak-to-peak dynamic range during mark condition within a bandwidth of 20 Hz to 1 MHz.

NOTE: All AGC circuits accept modulation ratio of between 2:1 to 6:1 with an input impedance of greater than 10 K ohms.

Input Time Codes Available

a—	IRIG A	g—	NASA 28
b—	IRIG C	h—	NASA 36
c—	IRIG D	i—	AMR B-2
d—	IRIG E	j—	AMR C-2
e—	IRIG G	k—	AMR D-5
f—	IRIG H	l—	XR-3

Unit is supplied with IRIG B capability unless otherwise specified.

Error Bypass Switch

The rotary selector switch allows the operator to bypass 1, 2, or 3 consecutive erroneous time frames without affecting the output information. An additional switch position (infinite bypass) allows continuing update of the translator using the input carrier as the clock frequency source. Error by-pass functions in both the Forward and Reverse directions.

· QUOTATION ·

CODED][COMMUNICATIONS
CORPORATION
1620 LINDA VISTA DRIVE, SAN MARCOS, CALIFORNIA 92069
714-744-3710

QUOTATION NO	124-016-06A
DATE	March 25, 1975
YOUR INQUIRY	Letter
DATED	December 12, 1974
F.O.B. :	San Marcos, California

The University of Texas
Marine Science Institute
Geophysics Laboratory
700 - The Strand
Galveston, Texas   77550

TERMS : ☒ NET 30 DAYS _____
☐ _____

WARRANTY PERIOD One year after
date of shipment

Attention: Dr. Gary V. Latham

Gentlemen: We are pleased to offer the following quotation.

ITEM	DESCRIPTION	QUANTITY	UNIT	EXTENSION	DELIVERY
1	Model 7101-0100 PCM Decommutation System	1	11,000.00	11,000.00	✓
2	Model 7101-4000 PCM Decommutation System	4	8,200.00	32,800.00	
3	Model 7101-4000 PCM Decommutation System (Optional Spare)	1	8,200.00	8,200.00	
4	Model 7110-1010 Word Selector (Optional)	1	7,115.00		
	a) hi current driver	1	375.00		
	b) modification for asymmetrical sampling recurring	1	1,250.00		
	c) above - non-recurring	1	1,800.00		
			10,540.00	10,540.00	No
5	Multiplexer-Memory - Recurring	1	10,510.00	10,510.00	
	- Non-Recurring	1	10,350.00	10,350.00	
6	Rack & Systems Engineering - Recurring	1	14,874.00	14,874.00	
	- Non-Recurring	1	9,900.00	9,900.00	
7	Program Management	1	7,650.00	7,650.00	
8	PDP-15 Interface & Software for working tape		16,960.00	16,960.00	
9	System Installation & Acceptance at the University of Texas		2,400.00	2,400.00	
	TOTAL			continued...	

See reverse side for Terms and Conditions.

The prices and delivery shown will remain valid for a period of ___90___ days from date.

BY _____

TITLE _____

·QUOTATION·

CODED][COMMUNICATIONS
CORPORATION
1620 LINDA VISTA DRIVE, SAN MARCOS, CALIFORNIA 92069
714-744-3710

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The University of Texas
Marine Science Institute
Geophysics Laboratory
700 - The Strand
Galveston, Texas   77550

Attention: Dr. Gary V. Latham

Gentlemen: We are pleased to offer the following quotation.

TERMS :   ☒ NET 30 DAYS _____
          ☐ _____
WARRANTY PERIOD   One year after
                  date of shipment

ITEM	DESCRIPTION	QUANTITY	UNIT	EXTENSION	DELIVERY
10	Ampex Tape Recorder, Model FR-2000 2 speed, playback only	1	39,969.00	39,969.00	✓
10A	Record capability and 3rd speed (Optional)	1	2,637.00	2,637.00	✓
11	Moxon Time Code Model 520 Time Code Translator with Flywheel Clock	1	3,436.00	3,436.00	✓
12	Bucode Tape Recorder Model 4025	2	8,021.00	16,042.00	No
13	Datum Tape Controller Model 5091	1	7,271.00	7,271.00	No
14	Spares Kit		1,613.00	1,613.00	✓

TOTAL $172,299.00

See reverse side for Terms and Conditions.

The prices and delivery shown will remain valid for a period of __90__ days from date.

BY J. A. Robinson
    Vice President, Operations
TITLE

PROPOSED ALSEP SYSTEM - 6/2/75

ASSUMPTIONS FOR PROPOSED ALSEP SYSTEM

O   PROVIDE THE H/W TO IMPELMENT A SINGLE PASS SYSTEM FOR DIGITIZING
    ANALOG DATA FROM RANGE TAPES.

O   PROVIDE THE S/W TO DIGITIZE, FORMAT, TIME EDIT & MERGE DATA
    FROM RANGE TAPES

O   GE WILL PROVIDE AN INTERDATA COMPUTER AND DISC.

O   TWO FR-1400'S AND TWO BRUSH RECORDERS WILL BE GFE'D

O   REMAINDER OF PROPOSED EQUIPMENT WILL BE PROCURED UNDER CONTRACT

O   SEVEN RANGE TAPES PER DAY FOR EACH DAY OF THE YEAR WILL BE PRO-
    CESSED TO OBTAIN P.I. TAPES. ANALOG RANGE TAPES PER YEAR WILL
    BE 2500.

O   PROCESSING OF RANGE TAPE IS BASED ON 1 1/2 SHIFTS PER DAY, 5
    DAYS PER WEEK. THIS INCLUDES A 20 PERCENT RERUN FACTOR FOR
    ANOMALIES.

O   THE EXPERIMENT DATA TO BE PROCESSED FOR PI TAPES ARE:

ALSEP STATION

EXPERIMENT	12	14	15	16	17
PSE	X	X	X	X	
LEAM					X
LSM				X	
SIDE	X	X	X		

THE QUANTITY OF DIGITAL TAPE PER YEAR WILL BE 4000 REELS

O   TRANSPORTATION COSTS FOR 2500 ANALOG TO ARCHIVE STORAGE, 2000
    DIGITAL TO ARCHIVE STORAGE, AND 2000 DIGITAL TO PI LOCATION
    HAVE BEEN INCLUDED FOR EACH YEAR.

O   PROCUREMENT OF 4000 DIGITAL TAPES PER YEAR IS INCLUDED.

O   S/W AND PROCESSING CAPABILITY FOR LSG-17; DTREM-14, 15; LSPE-17;
    AND LUNAR EPHEMERIS DATA IS PRESENTLY PROVIDED BY DSAD BUT IS
    NOT INCLUDED IN THE PROPOSED SYSTEM DUE TO LACK OF FUTURE
    REQUIREMENT.

O   HARDWARE EXPANSION CAPABILITY FOR PROCESSING LSG, DTREM, LSPE, AND
    LUNAR EPHEMERIS DATA HAS BEEN INCLUDED AND CAN BE AUGMENTED BY SOFT-
    WARE UPDATE IF REQUIRED IN THE FUTURE.

PROPOSED ALSEP SYSTEM

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┌──────────┐                                    ┌──────────┐                                              ┌────────┐
│8 CHAN.   │◄─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ │UNIV.     │                                              │DIG.    │
│          │                                    │I/O       │                                              │TAPE    │
│BRUSH     │◄───────────────────────────────┐   │BIPOLAR   │◄──┐                                          │XPORT   │
│RECORD    │                                │   │OUTPUTS   │   │                                          │800     │
│(2 EA)    │◄──────────────────────────┐    │   │(3)       │   │                                          │BPI     │
└──────────┘                           │    │   └──────────┘   │   ┌────────┐ ┌────────┐ ┌────────┐       └────────┘
                                       │    │                  │   │VIDEO   │ │        │ │        │
             ┌──────────┐              │    │                  │   │DISPLAY │ │PRINTER │ │CARD    │       ┌────────┐
             │34KBPS    │              │    │                  │   │& KYBD  │ │        │ │READER  │       │DIG.    │
             │DECOM     │──────────────┘    │                  │   └────────┘ └────────┘ └────────┘       │TAPE    │
┌──────────┐ │(5 EA)    │                   │   ┌──────────┐   │        │         │          │            │XPORT   │
│MAG       │ └──────────┘                   │   │UNIV.     │   │   ┌────────┐    ┌──────────┐              │800     │
│TAPE      │                                │   │LOGIC     │──►│COMP.   │◄───┤TAPE      │              │BPI     │
│P/B       │──►                             │   │I/F       │   │+       │    │CONTROL   │              └────────┘
│UNIT      │                                │   │          │   │MEMO.*  │    │800       │
│FR1400    │                                │   └──────────┘   │48KBYTE │    │BPI       │──►    ┌────────┐
└──────────┘                                │                  └────────┘    └──────────┘       │DIG     │
                                            │   ┌──────────┐                                     │TAPE    │
┌──────────┐ ┌──────────┐                   │   │          │                                     │XPORT   │
│MAG       │ │32KC      │                   │   │UNIV.     │   ┌────────┐                         │800     │
│TAPE      │ │TIME      │───────────────────┘   │LOGIC     │──►│DISC.   │                         │BPI     │
│PLAY-     │ │CODE      │                       │I/F       │   │&       │                         └────────┘
│BACK      │ │XLATOR    │                       │          │   │CONTR.  │
│UNIT      │ └──────────┘                       └──────────┘   │     *  │
│FR1400    │                                                   └────────┘        ┌──────────┐    ┌────────┐
└──────────┘                                                                     │TAPE      │◄──►│DIG.    │
                                                                                 │CONTROL   │    │TAPE    │
                                                                                 │556BPI    │    │XPORT   │
                                                                                 └──────────┘    │556     │
                                                                                                 │BPI     │
                                                                                                 └────────┘

      GFE                              *GE PROVIDED                                               ┌────────┐
                                                                                                 │DIG.    │
                                                                                                 │TAPE    │
                                                                                                 │XPORT   │
                                                                                                 │556     │
                                                                                                 │BPI     │
                                                                                                 └────────┘
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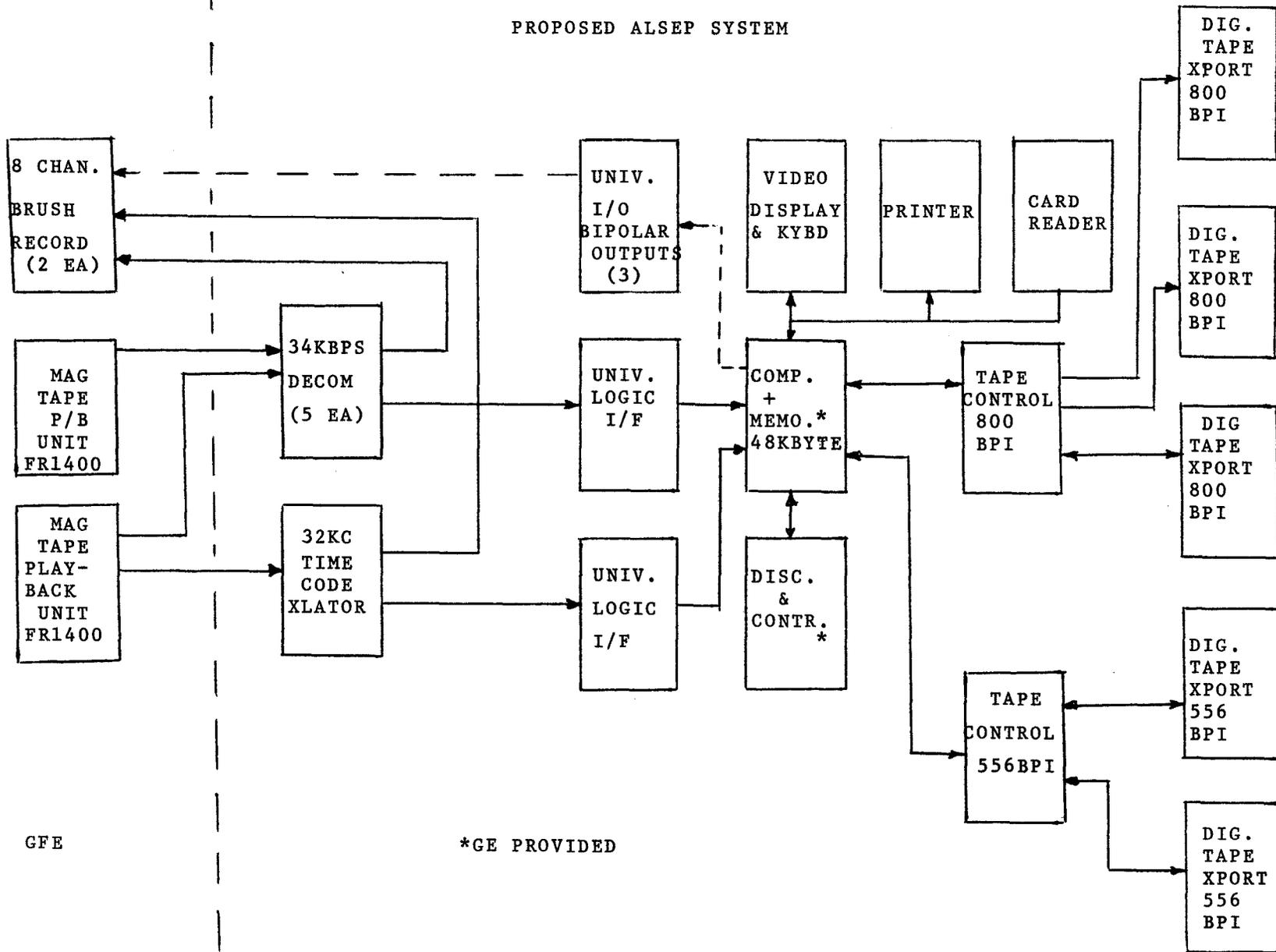
PROPOSED ALSEP SYSTEM

O SYSTEM HARDWARE PROVIDES:

   o   ANALOG RECORDER WITH BACK UP

   o   FIVE CHANNELS OF DATA ACQUISITION

   o   TIME CODE TRANSLATION

   o   COMPUTER SYSTEM CAPABLE OF 5 CHANNELS OF DATA REDUCTION
       SIMULTANEOUSLY AND GENERATION OF 800 AND 556 BPI TAPES.

   o   BRUSH RECORDERS FOR HARD COPY PLOTS

   o   MEETS ALL DATA FORMAT REQUIREMENTS

   o   DECOMMUTATES ALSEP PCM DATA FASTER THAN REAL TIME (X32)

O AVOIDS SCHEDULING CONFLICTS

   o   DEDICATED SYSTEM NOT DEPENDENT ON SCHEDULING PRIORITIES

   o   REALTIME OPERATING SYSTEM ALLOWS FOR TIME SHARED OPERATION
       AND S/W DEVELOPMENT

   o   HARDWARE IS ALL "OFF THE SHELF" (90 DAY DELIVERY)

O USES EXISTING HW/SW EXPERIENCE

   o   NO HARDWARE DEVELOPMENT COSTS/ONLY RACK AND STACK

   o   S/W EXPERIENCE ON MIST (NASA-MIUS) IS APPLICABLE

INTERDATA CAT. NO.	ITEM DESCRIPTION	GE SUPPLIED	NEW PROCUREMENT
M70-002	ID-70 W 32K BYTE MEM	*	
M70-100	POWER FAIL DETECT	*	
M70-103	SELECTOR CHAR	*	
M71-303	16K BYTE EXT. STORAGE	*	
M48-000	UNIV. CLOCK MODULE	*	
M48-013	UNIV. LOGIC INTERFACE (3)	*	*
M46-250	PAPER TAPE R/P I/F	*	
M46-416	DISC DRIVE & I/F (10M BYTES)	*	
M47-102	PASLA	*	
M49-020	SYSTEM CHASSIS	*	
M49-024	POWER SUPPLY	*	
M70-101	AUTO MEMORY PROTECT		*
M70-104	LOADER STORAGE UNIT		*
M70-105	STORAGE MODULE		*
M46-474	7 TRACK 800 BPI CONTROL		*
M46-476	(3) 7 TRACK TRANSPORTS 800 BPI		*
M46-473	7 TRACK 556 BPI CONTROL		*
M46-476	(2) 7 TRACK TRANSPORTS 556 BPI		*
M46-100	ALPHA VIDEO DISPLAY		*
M46-235	CARD READER I/F (400 CPM)		*
M46-234	HOLERITH TO ASCII CONVERTER		*
M46-230	CARD READER (400 CPM)		*
M46-202	LINE PRINTER I/F		*
M46-204	200 LPM PRINTER (132 CPL)		*
M48-608	UNIV. I/O SYSTEM CHASSIS		*
M48-350	BI-POLAR OUTPUT CARD (3)		*
MOXON			*
MOD.520	TIME CODE TRANSLATOR - ID70 I/F		*
MON SYST.			
MOD.1023A	(5 EA) BIT SYNCH, FRAME SYNCH, ID70 I/F		*

INTERDATA CAT. NO.	ITEM DESCRIPTION	GE SUPPLIED	NEW PROCUREMENT
M70-002	ID-70 W 32K BYTE MEM	*	
M70-100	POWER FAIL DETECT	*	
M70-103	SELECTOR CHAR	*	
M71-303	16K BYTE EXT. STORAGE	*	
M48-000	UNIV. CLOCK MODULE	*	
M48-013	UNIV. LOGIC INTERFACE (3)	*	*
M46-250	PAPER TAPE R/P I/F	*	
M46-416	DISC DRIVE & I/F (10M BYTES)	*	
M47-102	PASLA	*	
M49-020	SYSTEM CHASSIS	*	
M49-024	POWER SUPPLY	*	
M70-101	AUTO MEMORY PROTECT		*
M70-104	LOADER STORAGE UNIT		*
M70-105	STORAGE MODULE		*
M46-474	7 TRACK 800 BPI CONTROL		*
M46-476	(3) 7 TRACK TRANSPORTS 800 BPI		*
M46-473	7 TRACK 556 BPI CONTROL		*
M46-476	(2) 7 TRACK TRANSPORTS 556 BPI		*
M46-100	ALPHA VIDEO DISPLAY		*
M46-235	CARD READER I/F (400 CPM)		*
M46-234	HOLERITH TO ASCII CONVERTER		*
M46-230	CARD READER (400 CPM)		*
M46-202	LINE PRINTER I/F		*
M46-204	200 LPM PRINTER (132 CPL)		*
M48-608	UNIV. I/O SYSTEM CHASSIS		*
M48-350	BI-POLAR OUTPUT CARD (3)		*
MOXON			*
MOD.520	TIME CODE TRANSLATOR - ID70 I/F		*
MON SYST.			
MOD.1023A	(5 EA) BIT SYNCH, FRAME SYNCH, ID70 I/F		*

ALSEP SOFTWARE PROCESSES

O   DATA ACQUISITION

    o   CREATES DIGITAL IMAGE OF ANALOG PCM DATA AS RECORDED AT

       TRACKING NETWORK - BY ALSEP STATION.

O   TIME EDITS

    o   CORRECTS OR RECONSTRUCTS TIME TRACK ANOMALIES. A CONTINUOUS

       DATA VERSUS TIME (GMT) CORRELATION WILL RESULT.

O   FORMAT

    o   COMPRESS AND RECORDS ARCHIVAL AND PRINCIPAL INVESTIGATOR

       EXPERIMENTAL DATA ON TO DIGITAL IBM COMPATIBLE TAPE IN

       PRESCRIBED RECORD FORMATS WITH PROPER CHARACTER DENSITY.

O   MERGE

    o   MERGES MULTIPLE 24 HOUR DATA ON A SINGLE REEL.

O   QUALITY CHECK

    o   SUMMARIZES DATA ERRORS OF DIGITAL TAPES RECORDED DURING

       FORMAT PROCESS.

SYSTEM DATA FLOW

SYSTEM DATA FLOW

(A)   (B)   (C)

PRINCIPAL		PRINCIPAL		PRINCIPAL
INVESTIGATOR		INVESTIGATOR		INVESTIGATOR
FORMAT/MERGE		FORMAT/MERGE		FORMAT/MERGE
PROCESSING		PROCESSING		PROCESSING

24   PSE   72   SIDE   24   PSE   72   LSM   96   LEAM

| DATA |
| QUALITY |
| PROCESSING |

TO PRINCIPAL INVESTIGATORS

	FY	FY	FY	
ALSEP DATA PROCESSING SYSTEM	CY 75	CY 76	CY 77	CY 78
	J F M A M J J A S O N D	J F M A M J J A S O N D	J F M A M J J A S O N D	J F M A M J J A S O N D
1 CONTRACT AWARD	▲			
2				
3				
4 HWD. PROCUREMENT	▲——▲			
5				
6				
7 S/W DEVELOPMENT	▲——▲			
8				
9				
10 ACCEPTANCE TEST	▲▲			
11				
12				
13 OPERATIONS	▲———————————————————————————————▲			
14				
15				
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32				
33				
34				
35				
36				
37				
38				
39				
40				
	J F M A M J J A S O N D	J F M A M J J A S O N D	J F M A M J J A S O N D	J F M A M J J A S O N D

NOMINAL BUDGET COST

I. SYSTEM DEVELOPMENT - START/UP (5 MONTHS)

- H/W PROCUREMENT/INTEGRATION

                                                    230K
- S/W DEVELOPMENT

II. OPERATIONS (36 MONTHS)

- LABOR   495K

- MATERIALS/CONSUMABLES   15K

- TRANSPORTATION   40K

- DIGITAL TAPE   170K

                                                    720K

                        TOTAL ESTIMATE   -   950K

FA/Director of Data Systems and Analysis

TA/Acting Director of Science and
     Applications

                                        Owen K. Garriott

A Proposal for Processing ALSEP Data in an Offsite Facility

The present ALSEP data processing system at JSC was established for continuous produc-
tion of lunar data for a large number of experiments and users, with differing format
requirements. It has served the lunar science community well; however, with the recent
decline in users and operating experiments, reevaluation of processing techniques was
considered. In addition to the decline in principal investigators being funded by S&AD,
there has been an appropriate reduction in the budget. The FY75 and FY76 data process-
ing and operations costs exceed the scientific analysis costs being incurred by the
PI's. Without a substantial reduction in the cost of ALSEP data processing, the future
of the entire ALSEP program may be short-lived due to budgetary limitations.

With declining budgets and number of PI's in mind, a study was implemented by S&AD,
jointly with the Geophysics Working Group, to evaluate different techniques and/or
options for processing ALSEP data. Enclosure 1 contains the results of the Geophysics
Working Group evaluation.

Based on the working group recommendations, the University of Texas at Galveston (UTG)
was directed to further study and define a processing system which could be combined
with the PI's facility. UTG was selected because this PI is the user of approximately
60% of all returned lunar data. In addition, based on the presently funded PI's,
Dr. Gary Latham would probably be maintained throughout the lunar program. UTG has pre-
pared a proposal for a "Multiple Stream PCM Decommutation System," defined in enclo-
sures 2 and 3.

The Science and Applications Directorate submits, for your evaluation, a method to per-
form the ALSEP data processing using offsite University of Texas modified facilities,
beginning January 5, 1976. The hardware proposed and the development cost of this
method are estimated to be approximately 300 to 400K the first year, with an annual
operating cost of about 150K.

The proposal required that hardware be purchased by UTG (defined in enclosures 2 and 3).
The procurement, installation, and checkout of this system will require 6 months. Dur-
ing the processing development time, the DSAD would continue normal ALSEP processing.

All ALSEP analog range tapes would be sent directly from the GSFC/STDN to the UTG for
cataloging, processing, and reshipping to NASA storage. Enclosure 4 shows the flow of
data at UTG.

PI tapes in a compatible digital format for the LSI and LEAM experiments, or any two
experiments, and digital work tapes for federal records storage will be generated by
UTG. The digital work tape will contain all ALSEP stations on one tape, time sequenced.
Overlapping between range tapes would not be eliminated.

A major cost saving item would be the use of five simultaneous seismic station event plotting and monitoring techniques during the first analog tape pass by which the PSE PI could select which periods of data he wished to analyze in detail. Present data methods require the PI to scan all digital tapes sent from JSC to determine if any critical science data exists.

The simultaneous data processing of five ALSEP stations in parallel and the direct plotting of PSE event data are the main reasons for the low cost of this proposal. Another factor involved is that the portion of hardware and personnel needed to perform this task already exist and are performing data processing and analysis under the current PSE PI contract with NASA/JSC. The UTG computer system would be modified for analog-to-digital conversion, with two to three persons added for this task. As stated before, a substantial reduction in the cost of ALSEP data can be realized by this data processing technique.

It is requested that the Multiple Stream PCM Decommutation System be evaluated for technical adequacy and feasibility of the proposed technique. If additional information and/or further clarification are required, please contact Jim Bates at extension 2711. With the concurrence of SSAD for offsite ALSEP data processing, appropriate implementation action will be initiated by S&AD.

NEW CONSIDERATIONS IN ALSEP DATA PROCESSING

I.   INTRODUCTION

Several changes have occurred since the beginning of the processing
of ALSEP data that make it necessary to seriously reconsider the current
mode of processing. In this reconsideration it should be emphasized that
there is strong scientific justification for processing the data from all
currently operating ALSEP's (see enclosure 1 on ALSEP Science Rationale).
Processing of only one ALSEP is not a scientifically viable alternative
(see enclosure 2). The main reason for considering this mode has been
that it would effect a cost reduction. However, processing all ALSEP
station data using one of the options suggested below would effect at
least as great a cost saving and would make available data from all stations.

Regardless of the option selected it is important to continue to
generate and archive the 24 hour work tapes from all ALSEP stations in the
event that new results from lunar investigations should dictate the retrieval
of data from presently operating instruments whose data are no longer
being routinely analyzed.

Consideration of alternative processing modes is timely because of
three factors that have changed since ALSEP processing began. These are:
1) the changes in the processing requirements brought about by a reduction
in the number of operating experiments and active PI's; 2) the potential
impact of other JSC programs on the current method of ALSEP data processing
and; 3) the improvements in processing hardware.

II. REDUCTION IN PROCESSING REQUIREMENTS

At the height of the Apollo program several experiments at each of 5 ALSEP sites were operating. It was necessary to generate PI tapes for about a dozen PI's (see Table I in Appendix A for a listing of the experiments) At present, PI's are actively working on new data from only three experiments - the Lunar Ejecta and Micrometeoroid Experiment at Apollo 17, the Lunar Surface Magnetometer Experiment at Apollo 16 and the Seismic Experiments at Apollos 12, 14, 15, 16 and 17 (PSE, LSPE and LSG). The seismic data constitutes the large majority of the total ALSEP data received. Only two other PI's are being supplied data tapes from the 35 range tapes being processed each week. All other data are archived on 24-hour work tapes. The capability of a CDC 3200 system which is now being used at JSC is greater than now required to provide these PI tapes.

III. FUTURE PROGRAM IMPACT ON ALSEP DATA PROCESSING

Processing of ALSEP data in the current mode is likely to be increasingly impacted by other NASA programs. ASTP will likely result in backlog of one-two months in ALSEP processing this summer. An estimate for the continued operations of the ALSEP program is at least three years. Thus, software development such as for Shuttle and other JSC program needs may impact the ALSEP processing well before the end of the ALSEP program.

IV. IMPROVEMENTS IN DATA PROCESSING HARDWARE

The past several years have seen a rapid growth and expansion in the capability of minicomputers and other peripherals to the extent where any of a number of models would quite adequately handle the job of analog

range tape digitization and production of 24-hour digital work tapes as well as PI tapes. Simultaneous decommutation of the 5 ALSEP signals is also quite feasible, thus eliminating the necessity of making five passes of each range tape through the computer to strip out the different station data. Thus, the several options described below are feasible today, whereas at the time the original ALSEP processing program was developed, these technical advancements were not readily available.

V. SUGGESTED NEW PROCESSING MODES

Two alternatives appear as viable options to take advantage of the new developments. These are to either streamline the present JSC processing operations or to transfer the data processing to a dedicated new computer.

A. Updating JSC Processing Program

The present mode of passing the range tapes through the computer five times to serially decommutate the data from five ALSEP stations could be replaced, using updated decommutators, by a single pass with parallel decommutation (see Appendix B). A reduction in computer time possibly by a factor of five would be effected. This option would have the advantage of maintaining the present tape flow and distribution procedure. However, it will also require some modification of existing software.

B. Dedicated Minicomputer System

The use of a dedicated minicomputer system, programmed in assembly language to efficiently process the ALSEP data, could effect significant cost savings since nearly the entire capacity of the system would be used.

The minicomputer, such as a PDP 15 or 11/45, when properly programmed in assembly language would process the data at tape drive speed. Two possible systems are outlined in Appendix B.

Two options in establishing a minicomputer facility suggest themselves. One is to utilize the existing PDP 15 computer currently processing PSE data at the PI's institution (UT, Galveston). Somd additional hardware is required, i.e., an analog tape drive and FM/PCM converter as well as a time-code translator (see Figure B2 of Appendix B). Range tapes would be used directly as the input, rather than PI tapes. Analog to digital conversion, decommutation into the five ALSEP station bit streams, processing of the PSE data, stripping of the LEAM (Apollo 17) and LSM (Apollo 16) data onto separate PI tapes and generation of 24 hour work tapes would be accomplished during one pass of the range tape data through the computer. Highly efficient use of the computer would be effected since a large majority of the ALSEP data is from the seismic instruments and most of the ALSEP data tapes generated at JSC are currently being processed at this PI's facility. The passage of the large majority of the ALSEP data through two computers, once to make 24 hour work tapes and PI tapes, and once to process the PSE PI tapes would be eliminated.

The other option is a dedicated minicomputer at JSC or at another facility (see Figure B3 of Appendix B). This option has the advantages described above of a dedicated computer using range tape input, except the efficiency accrued from processing seismic data simultaneously with range tape digitization. However, if the facility were within JSC all of the ALSEP data processing to the point of producing

PI tapes would remain contained within the JSC organization. Operation of the geophysical data curatorial program within S&AD would be facilitated by the existence of the minicomputer which could be implemented during an additional shift for this program.

VI. RECOMMENDATIONS

It is recommended that one of the suggested options be implemented in a timely fashion. Regardless of the option selected it is most important to continue to generate and archive 24 hour work tapes and to process the data from all ALSEP's.

APPENDIX A

Number	Experiment	Apollo Mission				
		12	14	15	16	17
S-031	Passive Seismic	X	X	X	X	
S-033	Active Seismic		0		0	
S-034	Lunar Surface Magnetometer	0		0	X	
S-035	Solar Wind Spectrometer	@		0		
S-036	Suprathermal Ion Detector	X	0	X		
S-037	Heat Flow			@		@
S-038	Charged Particle		@			
S-058	Cold Cathode Gage	0	@	@		
S-202	Lunar Ejecta and Meteorites					@
S-203	Lunar Seismic Profiling (As Identified)					@
S-205	Lunar Atmospheric Composition					0
S-207	Lunar Surface Gravimeter					0
M-515	Dust Detector	X	X	X		

X - PI tapes being processed

0 - Non-Operating Experiments

@ - Reduced on 24-hour tapes
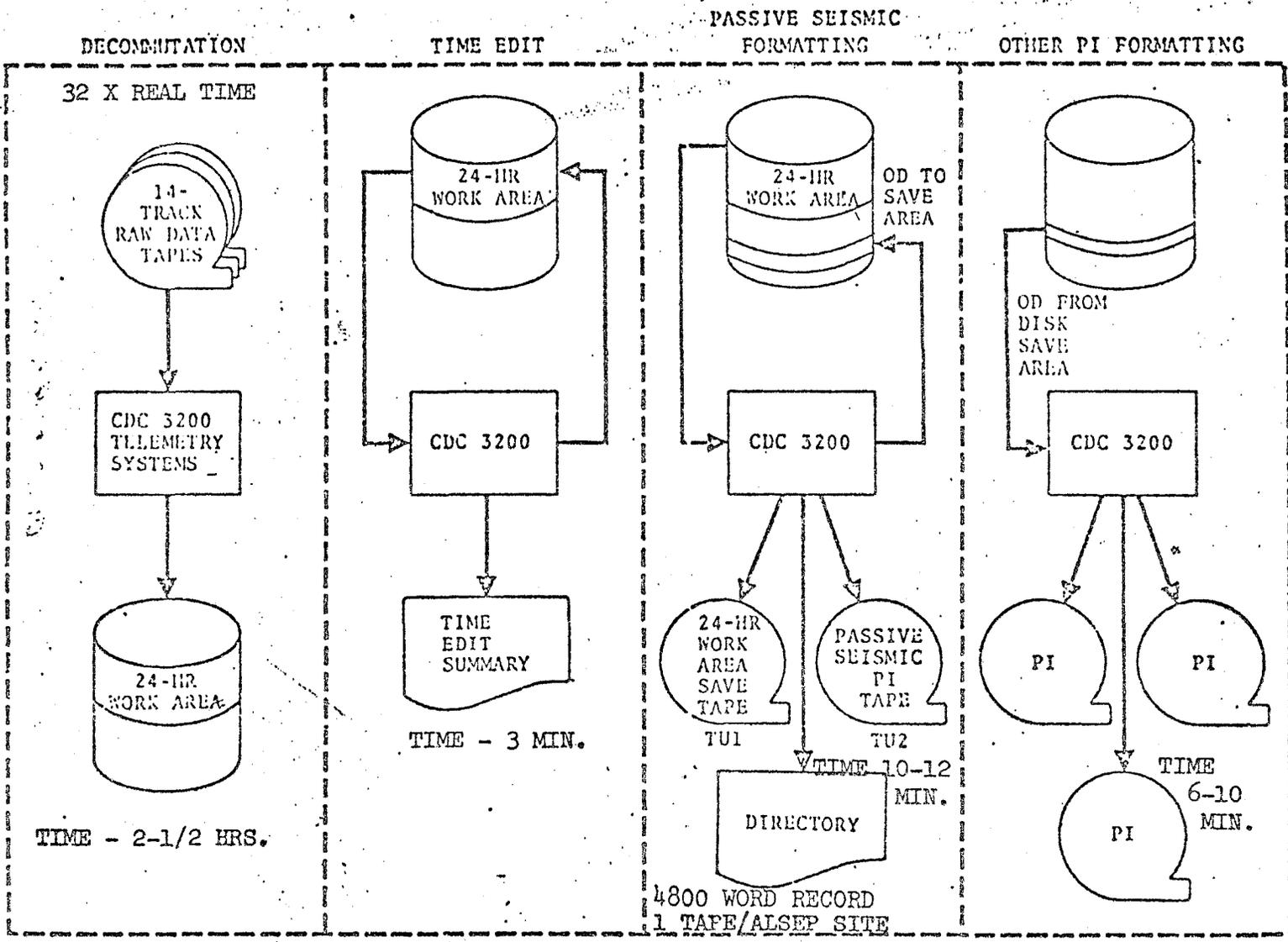
Figure B.1a: Flow diagram of JSC ALSEP range tape processing to produce 24-hour work tapes and PI tapes. The decommutation process is depicted in detail in Fig. B. 1b.
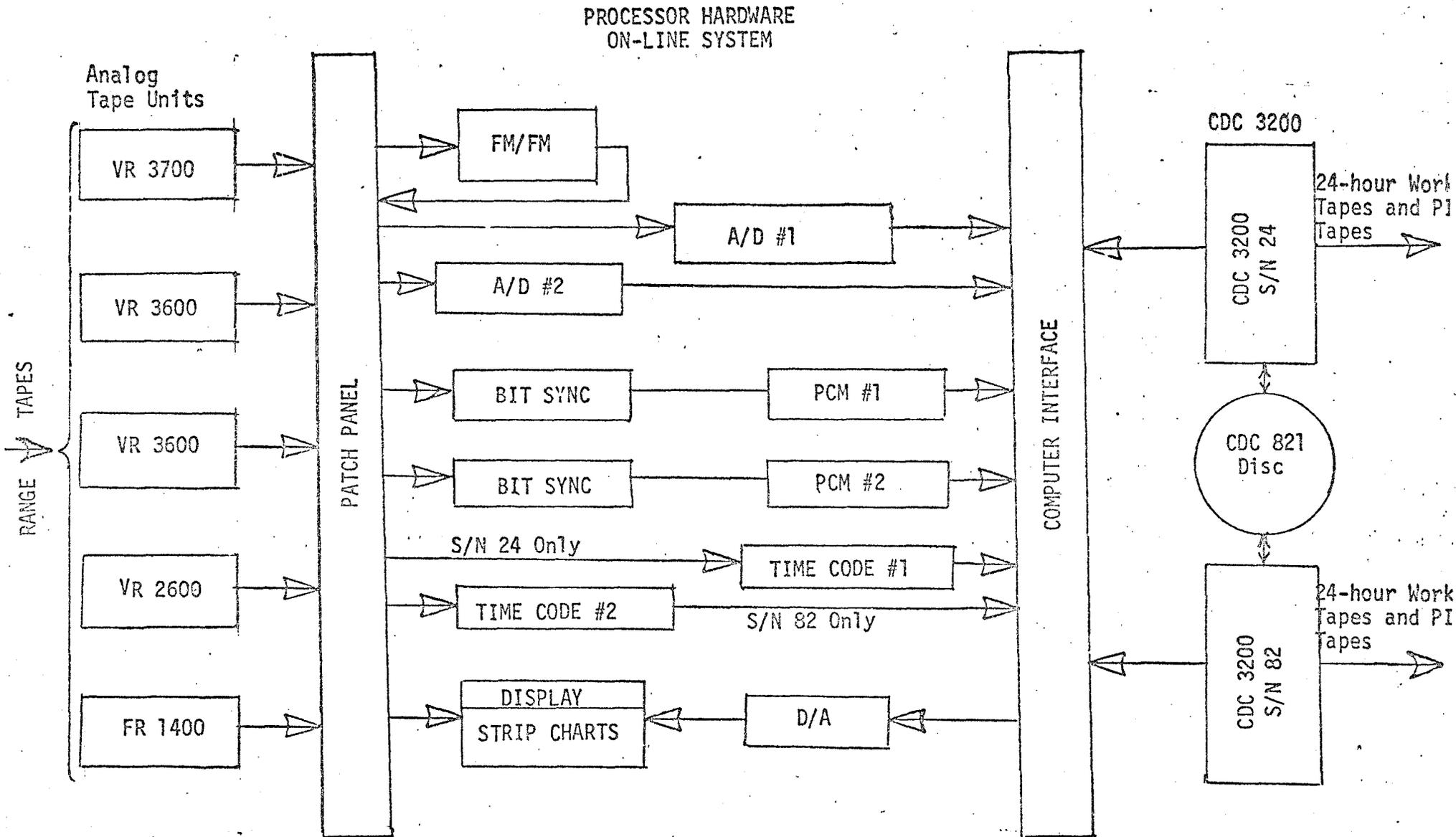
Figure B.1b: Decommutation, A/D conversion and computer interface at JSC. The patch panel allows only one ALSEP station to be processed at a time.
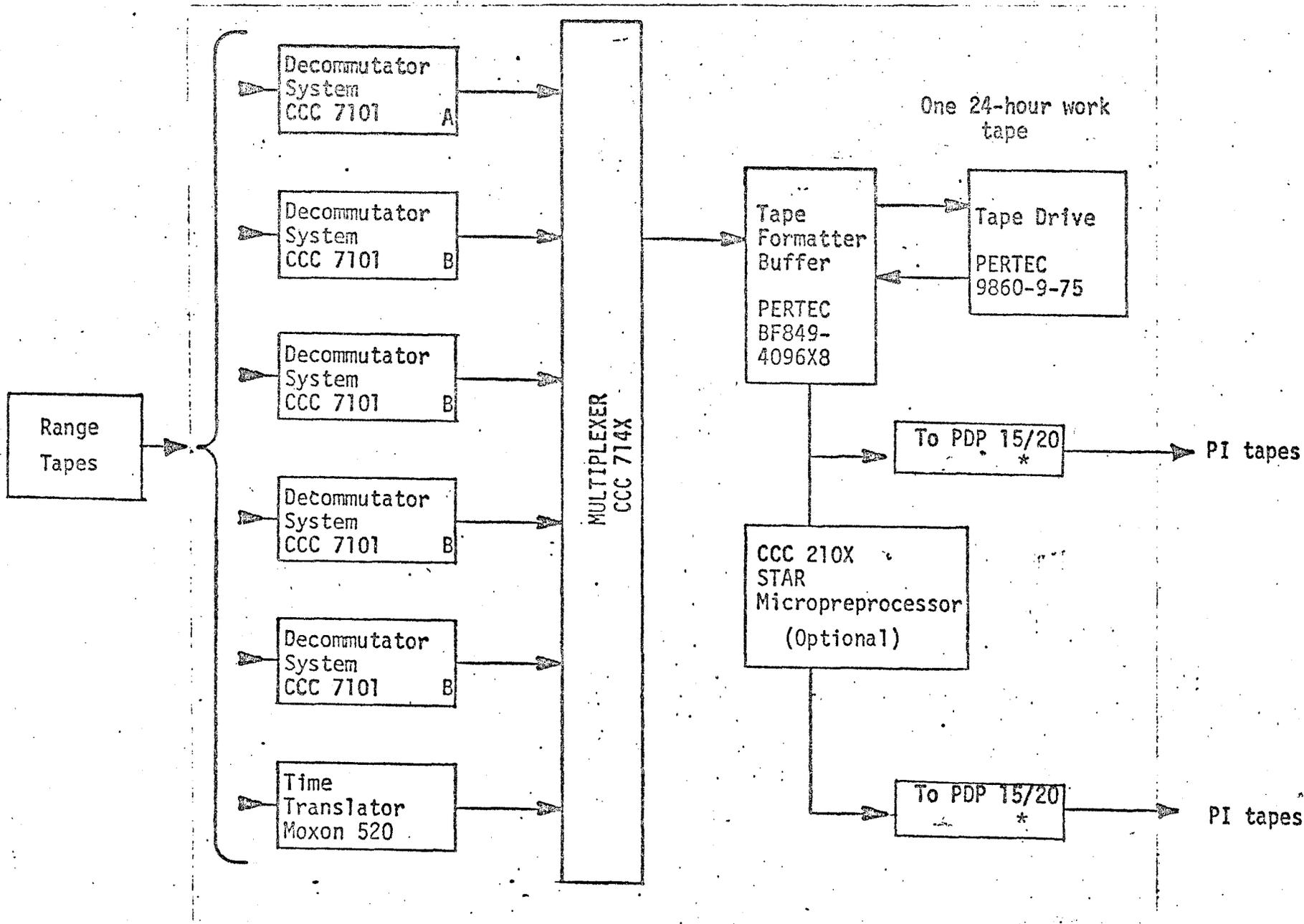
Figure B2: Flow chart of ALSEP data processing at a PI facility. Equipment that exists at the facility is shown by an asterisk. This system uses one tape format buffer and a multiplexer to produce one 24-hour work tape for all five ALSEPS.

```
┌──────────┐      ┌─────────────────────┐          ┌──────────────┐
│          │      │ Tape Recorder with  │          │              │
│  Range   │ ───▷ │ FM/PCM Converter and│ ───────▷ │  PDP 11/45   │ ───▷ 5 - 24-Hour Work Tapes
│  Tapes   │      │ Time Code Translator│          │              │
│          │      │      FR 2000A       │          │              │
└──────────┘      └─────────────────────┘          └──────┬───────┘
                                                          │
                                                          └──────────▷ PI Tapes
```
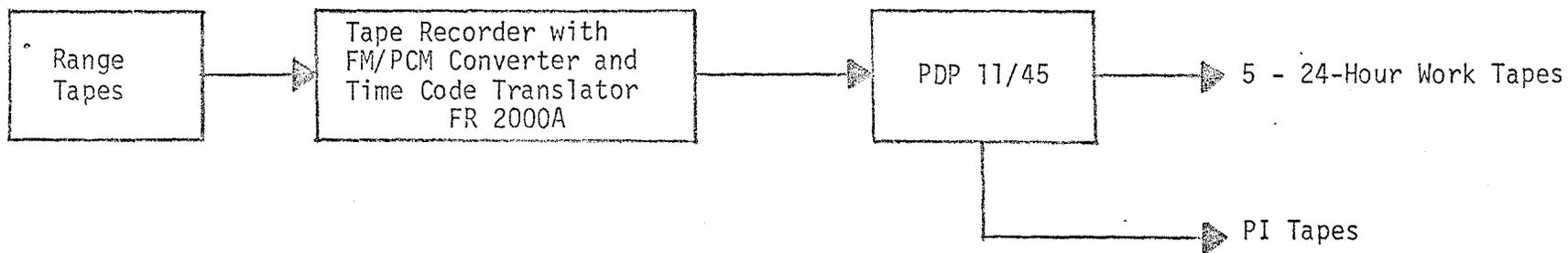
Figure B3: ALSEP data processing using a single unit for decommutation, time-code translation and
tape writing. One 24-hour work tape is generated for each ALSEP.

Notes on ALSEP Range Tape Processing at the

Geophysics Laboratory of the University of Texas at Galveston

1. Range tapes will be processed at speed up of 16:1. Assuming average

    of 7 range tapes per day, range tape processing will require 4-5 hrs.

    per day. Slower speed will 1) reduce maintenance cost and risk of

    damage to range tapes, and 2) eliminate need for purchase of high-

    speed digital tape drives.

2. The following products are planned:

First Pass

    (a) 7-track, digital work tape containing data from all 5 stations

        (on a single tape). Range tapes will be processed chronologically

        without merging. Each ALSEP frame (64 words) recorded on the

        work tape will include time and station identification. Work

        tapes will be delivered for archiving.

    (b) Compressed scale playout of seismic data from stations 12, 14

        (SPZ only), 15, and 16; and, possibly the gravimeter from sta-

        tion 17.

    (c) Experimenter tapes for

        i) LSM at station 16

        ii) LEAM at station 17

        Formats for these tapes to be arrived at by agreements with the

        Principal Investigators.

Second Pass - using digital work tape

    (a) PSE event tapes in present format for delivery to NSSDC

       and for use in further analysis by the P.I.

3. The Geophysics Laboratory will receive and log all incoming range tapes directly from their source; process and ship all range tapes, digital work tapes, PSE event tapes, and P.I. experiment tapes to their aqpropriate recipients.

4. No DSAD support required.

G. Latham
April 21, 1975

DATA FLOW

Decom rate 16:1

COMPUTER INTERFACE

FROM
GSFC/MARS
ANALOG
TAPE

| RECEIVER |

| ANALOG TAPE RECORDER |

| DECOM 5-6004 |

| 5-CHANNEL MULTIPLEXER ASSEMBLY |

| PDP 15/40 COMPUTER |

| VARIETEC PLOTTER |

| PSE-12 |
| PSE-14 |
| PSE-15 |
| PSE-16 |
| LSG-17 |

| TIME CODE TRANSLATOR |
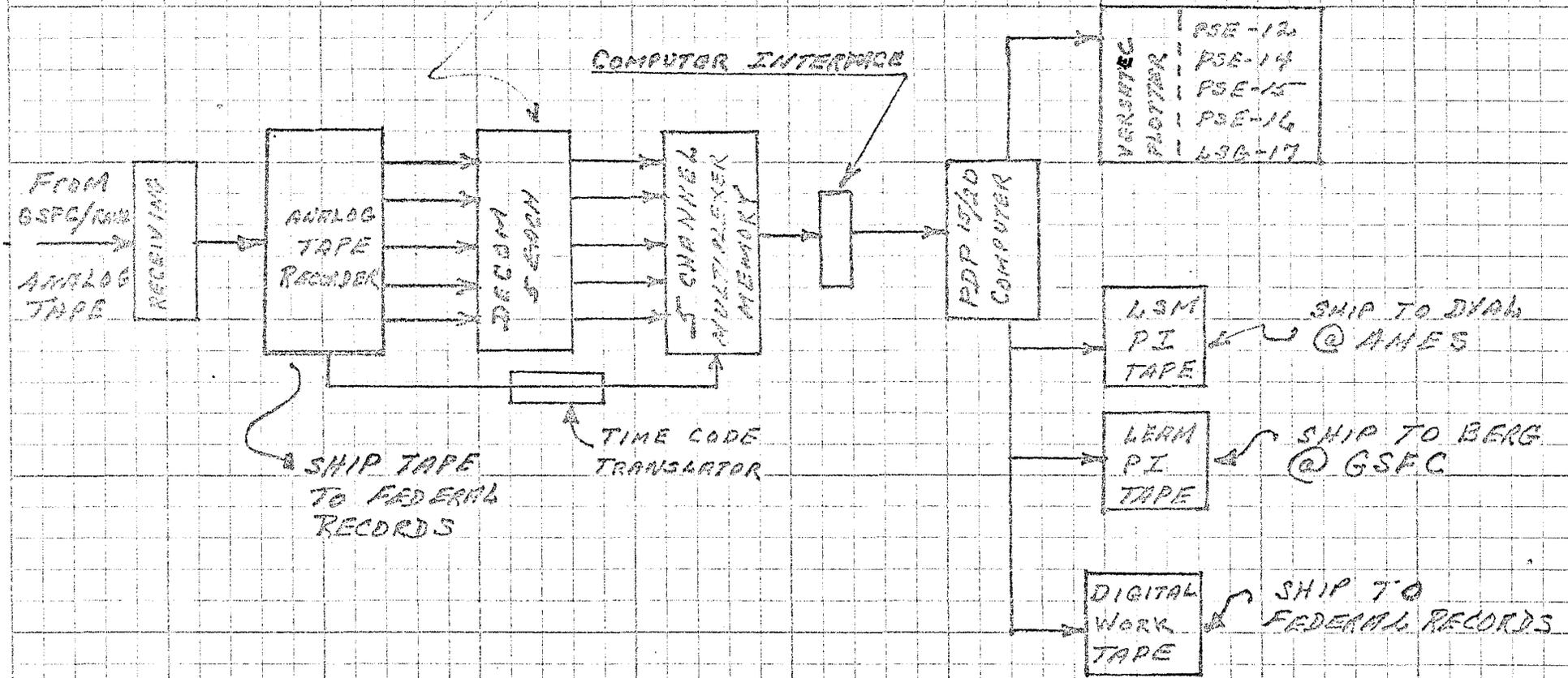
SHIP TAPE
TO FEDERAL
RECORDS

| LSM PI TAPE | SHIP TO DYAL @ AMES

| LEAM PI TAPE | SHIP TO BERG @ GSFC

| DIGITAL WORK TAPE | SHIP TO FEDERAL RECORDS