ATM-626

FEBRUARY ENGINEERING MODEL TEST PROGRESS REPORT

28 February 1967

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CONTENTS

ILLUSTRATIONS

TABLES

1.0 PROGRESS SUMMARY

This is the fourth monthly progress report on the ALSEP Engineering Model Systems Tests which covers the efforts during the time period 1 February through 28 February.

In general the EM System Tests are proceeding well and on the schedule established in ATM-604.

Category #2 and #3 tests are complete on all the Array "A" experiments provided (EM of SWE, LSM, and PSE Central Station Electronics, and a breadboard of the SIDE/CCGE). Category #4 tests are complete on LSM and partially complete on PSE and SIDE. In addition to these Array "A" experiment tests, limited Category #2 tests were performed on the CPLEE and ASE. STS #1 is commissioned on the EM and all functional operations resolved. The STS computer programs for the LSM, PSE, SIDE, and SWE are either complete, in last stages of checkout, or undergoing modification after initial system runs on Category #4 tests.

The Data Subsystem continues to operate well although the first faults in the digital portions of the subsystem occurred in this report period. The data processor has clocked 4.5 months of faultless operation. However, the analog multiplexer malfunctioned and was removed from the line for repairs for about one week during February. The command decoder developed an intermittent which was traceable to a broken wire in the unit. The performance of the command receiver was intermittent as reported in preceeding reports. The transmitter operated well through most of the period. However, during the later portion of the month, the transmitter on occasion drew excessive current and finally failed. Both EM transmitters were returned to the subcontractor for repair.

The operation of the PSE, SWE, EM models and SIDE breadboard was good during this report period. The major effort remaining for Array A tests with these experiments is to confirm that the STS software is correct. On the other hand, the LSM EM and its ETS contained a considerable number of functional discrepancies. These operational discrepancies were reported back to ARC for correction in succeeding models. The LSM STS software program operated well after simple modifications to improve the ease of interpretation of data.

The ASE and CPLEE Array B experiments underwent integration tests. An incompatibility with the ASE circuit protection circuits existed and these circuits were modified. The functional operation of ASE was correct. CPLEE operated in vacuum with the EM system for the first time during this period. When not bothered by an intermittent intercabling problem, the experiment operated well.

STS #1 was commissioned with the EM and the hardware operated well. The software for the LSM experiment was checked out completely and the PSE, SWE and

SIDE software ran with the system with varing degrees of success. This software is at present undergoing minor modifications.

A situation uncovered which may present problems on succeeding model tests is the time required to interpret the STS print-out data. It requires several tens of highly trained engineering man hours to interpret one hour of LSM print out. This has been discussed with the ALSEP test group.

An additional week of testing was added to March test schedule in order to perform confirming tests on ALSEP Array "A3". In this array the SIDE is replaced by CPLEE. On tests to date with EM, CPLEE replaced LSM. This addition will prolong the EM test period by one week.

2.0 MONTH's ACCOMPLISHMENTS

The significant accomplishments of this months EM tests are:

1. Completion of Category #2 tests on LSM EM.
2. Completion of Category #3 tests on Array "A" experiments consisting of PSE Central Station Electronics, SWE, LSM, and SIDE/CCGE breadboard.
3. Completion of Category #4 tests on LSM.
4. Partial checkout of Category #4 tests on PSE and SIDE.
5. Preliminary integration tests with ASE.
6. Preliminary integration tests with CPLEE.
7. Integration and checkout of STS with EM.
8. Confirmation of STS software programs for Data Subsystem checkout and LSM.
9. First prolonged operation using the RF up and down links.

3.0 TEST RESULTS

3.1 ENGINEERING MODEL TEST CONFIGURATION

The basic arrangement of the Engineering Model Tests is shown in Figure 3.1-1 of the January EM Progress Report, ATM-618. Figure 3.1-1 is a photograph of the EM test area. Table 3-1 indicates the status of all equipments on line during the month.

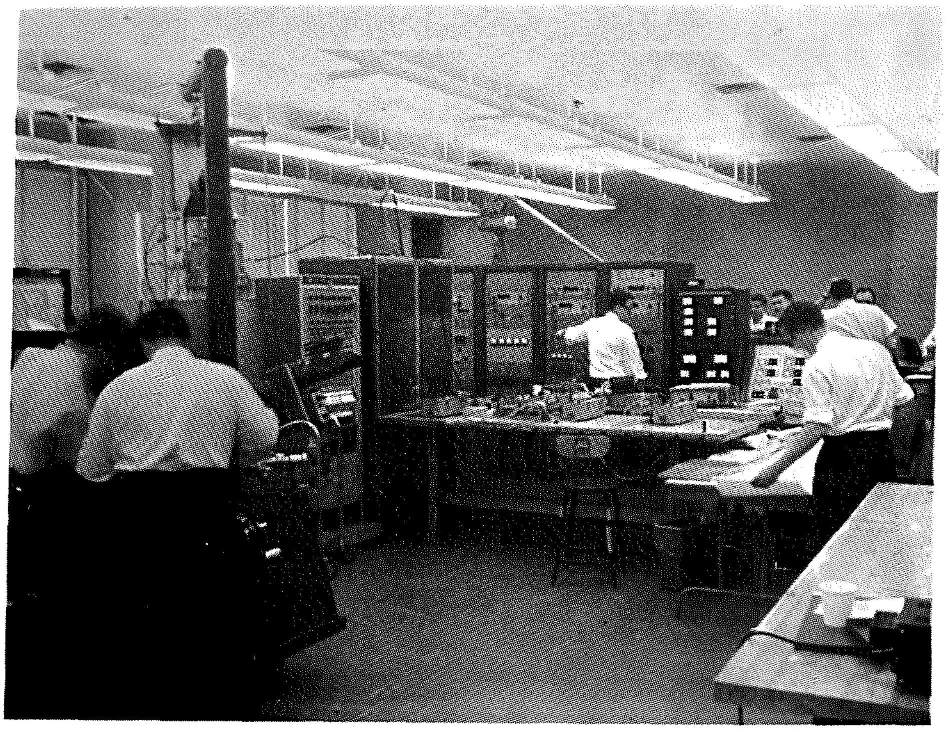


Figure 3.1-1 General View of Engineering Model Test Laboratory

TABLE 3-1

STATUS OF ENGINEERING MODEL HARDWARE ON LINE

Month Ending 28 February 1967

Prime Equipments

Subsystem/Component	Breadboard	Modified Brassboard	Engineering Model	Remarks & Status
Data Subsystem				
Data Processor		X		
Multiplexer - A/D Converter		X	X	Both malfunctioned and repaired.
Diplexer			X	
Diplexer Switch			X	
Transmitter "A"			X	Failed 2/24 } *
Transmitter 'B"		X		Undermodulated } *
Receiver		X		Intermittent Lo B
Command Decoder		X		
PDU			X	
Wire Harness			X	
Terminal Strip			X	
Power Subsystem				
RTG Simulator (BxA)			X	
RTG Generator (GE)				On line in January
PCU			X	
PDM			X	
Structural/Thermal				
Base Plate			X	
Dust Detector			X	
Experiments				
Passive Seismic			X	
Solar Wind			X	Turn off V trans dev.
Magnetometer			X	Many func. descrepancies
SIDE/CCIG		X		
CPLEE			X	{ Returned to BRLD
ASE			X	{ most of February.
Heat Flow				

*Both returned for repair.

STATUS OF ENGINEERING MODEL HARDWARE ON LINE

Month Ending 28 February 1967

GSE

Subsystem/Component	On Line	Operation: Satisfactory	Operation: Unsatisfactory	Remarks
Signal Breakout Boxes				
Passive Seismic #1	X	X		
#2				
Solar Wind	X	X		
Magnetometer	X	X		
SIDE/CCIG	X	X		
CPLEE	X	X		
ASE	X	X		
Heat Flow				
Data SS Test Set				
DDS 1000	X		X	Down for repairs for two weeks.
Uplink	X	X		Turned over to
Downlink	X	X		DSS for use in pro-
Experiment Simulators				totype checkout.
RF Test Set	X	X		
Experiment Test Sets				
Passive Seismic	X	X		
Solar Wind	X	X		
Magnetometer	X		X	
SIDE/CCIG	X	X		
CPLEE	X	X		
ASE	X	X		
Heat Flow				
STS #1				
Data Unit	X	X		Received on 2/13
Programmer Processor	X	X		

3.2 CENTRAL STATION STATUS

3.2.1 Data Subsystem

The digital circuits of the data processor continued to operate without fault during the period covered by this report.

One period of intermittent operation of the command decoder was encountered. This was associated with a broken wire in the harness of the decoder between the circuit boards and the central station connector.

The analog multiplexer malfunctioned and on investigation two of the FET transistors in the multiplexer were discovered to be short circuited. The reason for the failures is not fully established. It may be due to the overvoltage conditions which were caused by PCU defects, as described in Section 3.2.2 below.

Between 2/3/67 and 2/24/67 the RF data links were fully operational, using transmitter serial #2. Transmitter serial #1 could not be used with the downlink receiver. As previously reported its modulation index is too low to produce a satisfactory split phase data signal from the GSE receiver. During this period of operation, unexplained central station power fluctuations were observed, especially following initial turn on at the start of a new day's operation. The increase in power consumption was about 10W, and until 2/19/67 the high power consumption was only present for at the most a few seconds. The high power condition persisted for increasingly longer periods during the next week, and on the morning of 2/24/67 it was confirmed that the transmitter serial #2 was responsible.

During the afternoon of 2/24/67 following an overvoltage condition which reached about 35V on the 29V line for several seconds, the transmitter input current is believed to have increased to an abnormally high value, associated with a complete transmitter failure. The transmitter changeover circuit appears from the available records to have taken at least 5 seconds to react, possibly because the overload was sufficiently large to reduce the line voltage to about 10V. The station power was shut down, several attempts were made to reapply power for a few seconds during the next two minutes, and it appeared that the PCU oscillator would not restart, Finally, the PCU recovered after about 2-1/2 minutes from the initial overload, and it does not appear to have sustained any permanent damage.

3.2.2 Power Subsystem

Two PCU faults have occurred intermittently during February. The first was an occasional failure to respond to a PCU #2 to PCU #1 changeover command. No failure of the reverse transition was observed, and it appears that the PCU changeover relay has a tendency to hang up in the PCU #2 on position.

The second failure has been loss of regulation of PCU #1. On some occasions this fault would clear itself after a few seconds, at other times either turning power off and on again, or else changing over to PCU #2 and back again to PCU #1 restored voltage control. With a fully loaded central station the on set of the loss of regulation is difficult to detect as the rise in PCU output voltage is small; however, if some of the loads are then shut off the PCU output voltages rise, and this sequence of events occurred prior to the failure of transmitter serial #2.

Investigation has established that this is a failure within the PCU #1 regulator circuit and is not in any equipment external to the PCU. Further investigation has been hampered by the desire to maintain system operation to complete Category #3 and #4 tests, and by the intermittent nature of the fault condition.

3.3 CATEGORY #2 TESTS

3.3.1 Passive Seismic Experiment

Category #2 test for PSE were completed in January and the results were published in ATM 618. During the month, the turn-on power transient was verified and is shown in Figure 3.3.1-1. Transients as high as 400 ma were noted.

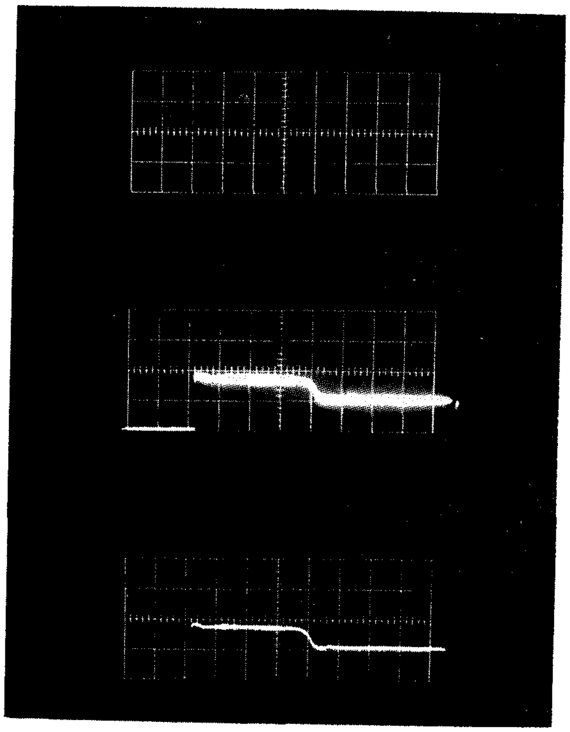
3.3.2 Solar Wind

Category #2 tests for SWS were completed in January and the results were reported in ATM 618. During Category #3 tests a change in the SWS turn-off voltage transient was recorded. Figure 3.3.2-1 shows the 200V peak-to-peak transient. Besides the increase in amplitude by a factor of 10, the frequency of oscillation shifted from approximately 15 to 133 KHz. This would correspond to a decrease in capacitance by two orders of magnitude if the interrupted circuit were a pure LC parallel resonant network.

3.3.3 Charged Particle Lunar Environments Experiment

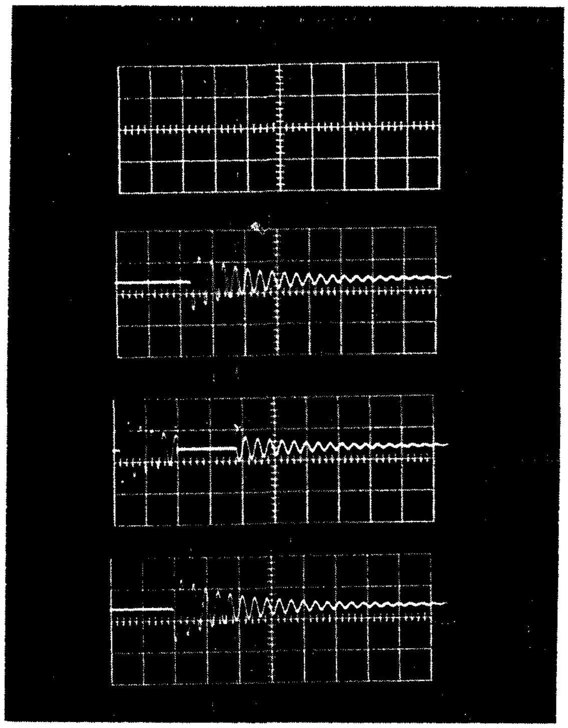
At the beginning of the reporting period Category #2 test on CPLEE were interrupted because of the nonavailability of a vacuum qualified connector. During the delay a decision was made to return the experiment to Bendix Research for modification.

At the end of the period, subsystem tests have again been completed and Category #2 tests in vacuum were initiated. A problem occurred with a subtle intermittent traceable to a low impedance path in the central station to CPLEE intercabling. From a preliminary review of the data, the experiment appears to be operating properly.



200 ma/cm
10 ms/cm

Figure 3.3.1-1 PSE Turn-On Transient



All
100V/cm
20 sec/cm

Figure 3.3.2-1 Solar Wind Turn-Off Voltage Transient

3.3.4 LSM Category #2 Tests

Category #2 tests on the LSM Engineering Model began on the afternoon of 14 February. Figures 3.3.4-1 and 3.3.4-2 show the LSM experiment and its associated flux tanks. Testing did not proceed smoothly and some of the major problems were not resolved until after initiation of Category #3 tests. The main problem was that the LSM EM's functional operation was incomplete and it had serious malfunctions. Also the ETS would not accept timing and control pulses from the LSM SBOB and the ETS status displays were not stable. The timing and control problem had also been encountered on the breadboard and was resolved by adjustment of the ETS Schmitt trigger levels. Jitter in the status displays was more difficult to find and was finally resolved on the 20th of February after more than three days of extensive trouble shooting. The problem was attributed to the lack of shield grounding in the ETS connection to the status lamps. Category #2 tests were essentially complete by the evening of the 15th. This included checking for power line noise, verifying command responses, and checking timing and control signals to determine differences between the breadboard and Engineering Model. The LSM power converter noise was lowest of any experiment examined to date. Figure 3.3.4-3 shows the high frequency noise is about 30 millivolts at a repetition rate of about 91 KHz.

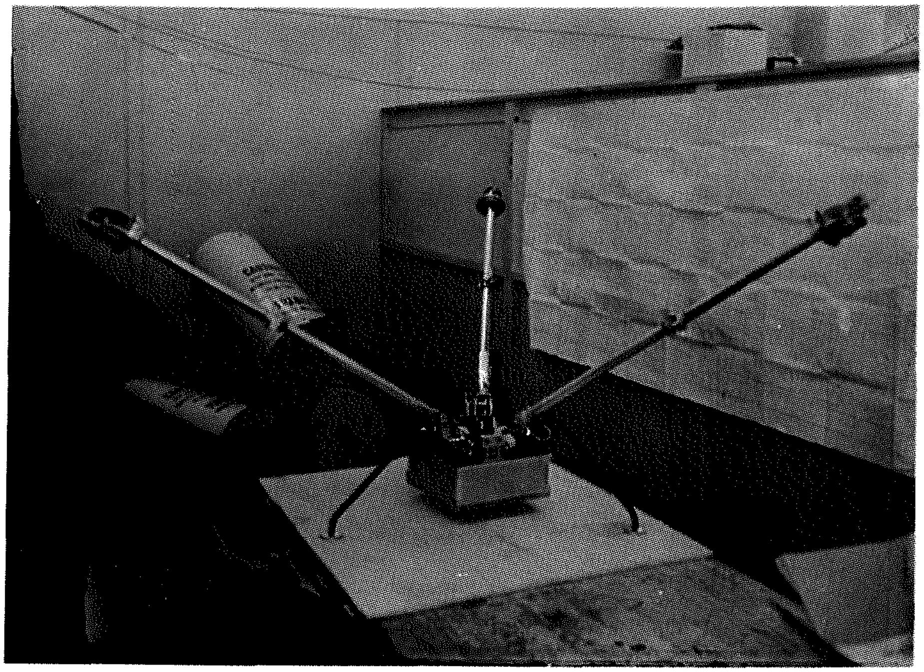
Table 3.3.4-1 is a table of discrepancies noted during the Category #2, #3, and #4 tests. Only those problems which are not resolved are shown. A brief summary of Category #2 tests is given below:

Power

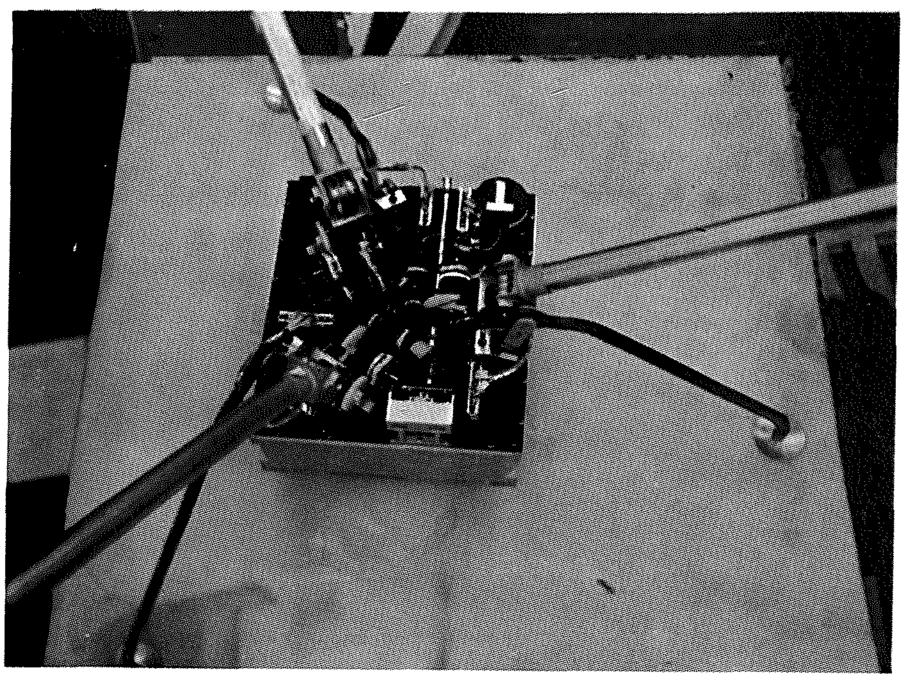
Power line noise feedback was very good as mentioned above. The turn-off voltage transient was also exceptional. Approximately 10V peak-to-peak was measured compared to 400V transient measured on the breadboard. A summary of power consumption is:

LSM Status	Current Ripple
1. Normal	165-210 ma
2. Flip-Cal	190-235 ma
a. With motor on*	475-520 ma
3. Initital Turn On	175-230 ma
4. Thermal Control	200-245 ma
5. Current Glitches	
a. Non-induced	70-90 ma

*Current level depended on individual motor and various levels were noted on each motor. High frequency spikes were not recorded.

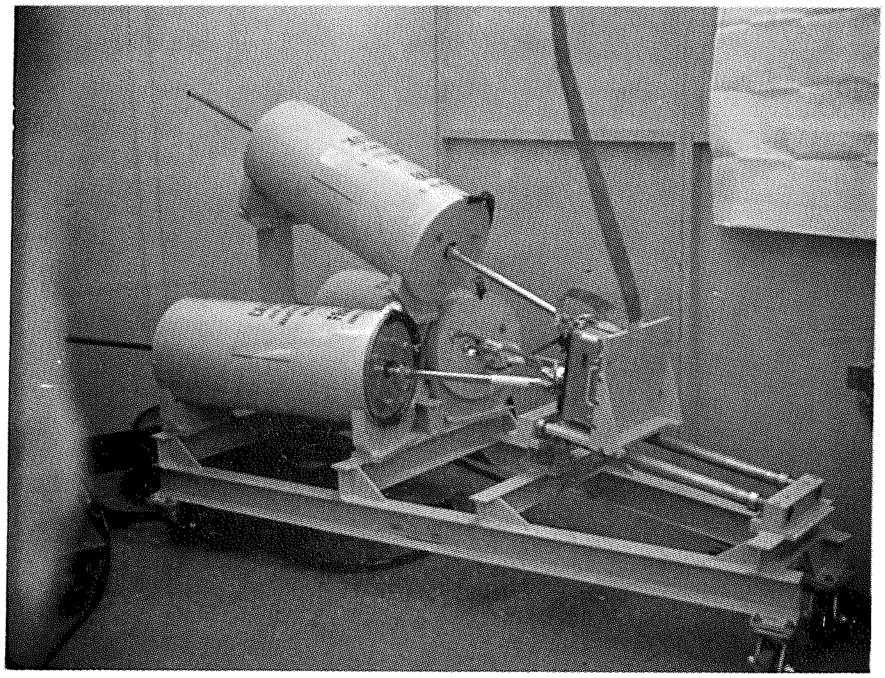


(a) Side View

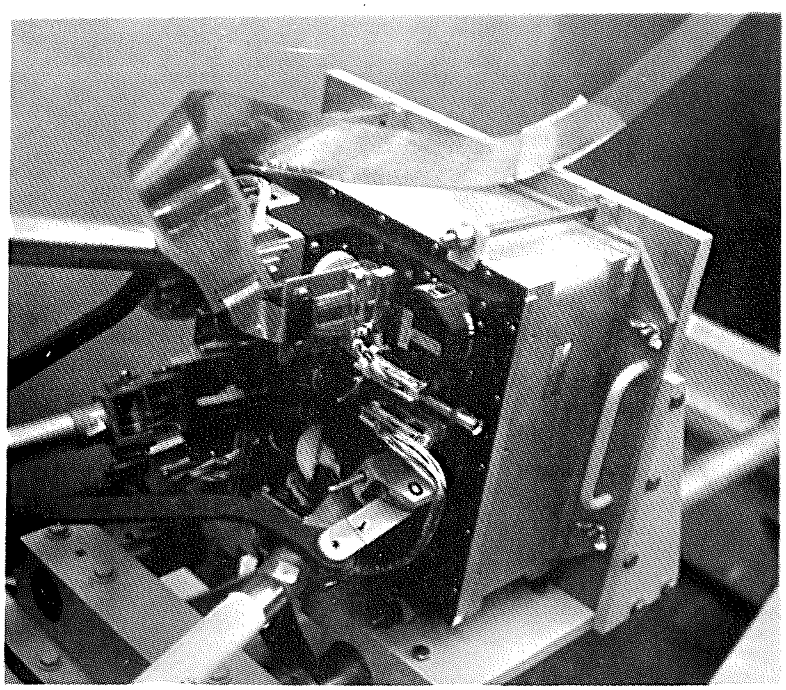


(b) Top View

Figure 3.3.4-1 LSM EM in Deployed Position

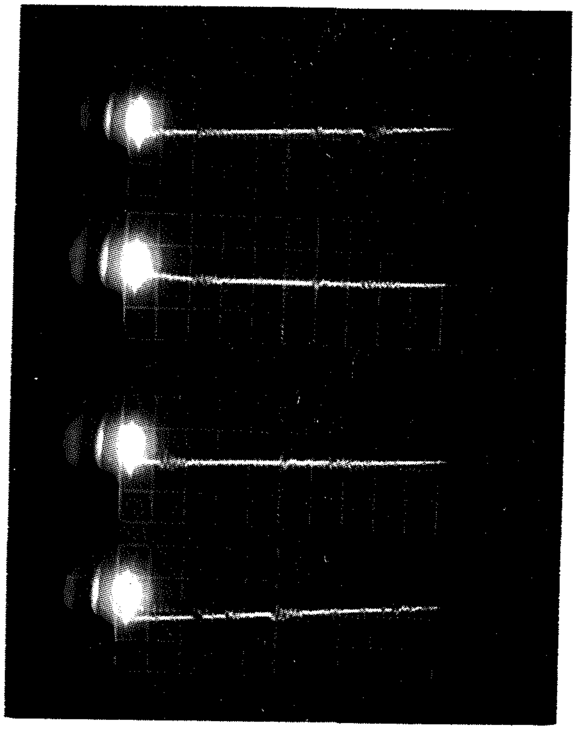


(a) In Test Position in Flux Tanks



(b) Close Up

Figure 3.3.4-2 LSM Engineering Model



50 mV/cm
2 μs/cm
Single Sweep

Figure 3.3.4-3 LSM 29V Noise

TABLE 3.3.4-1

LSM DISCREPANCIES NOTED IN EM TESTS

	Discrepancy	ICS Paragraph	ICS Value	Acceptable Value to Bendix	Remarks
1.	Turn-On Power Transient	3.2.3.1	3.5w		Not accurately measured. A 50 ohm power limiting resistor in +29V line was used to reduce surge to below 14W in both the breadboard and EM.
2.	Flip-Cal Power Transient	3.2.3	7.0w	7.0w	Total current during Flip-Cal with motors on, greater than 500 ma for both breadboard and EM.
3.	Operational Power	3.2.3.1	3.5w	3.5w	No significant change in power level noted between breadboard and EM. Normal current ripple from 165-210 ma. See discussion Category #2 test for further data.
4.	Test Set Display Jitter	3.2.6.3.1	NA	None	Schmitt trigger levels required adjustment in order to accept timing and control pulses from ALSEP for both breadboard and EM. Jitter re-appeared before completion of LSM EM tests. Cause unknown but appears due to EMI within the ETS.
5.	Improper Flip Calibrate	3.2.3.1	NA		Flip calibrate gave variable results. Power profile was unexplainable from information furnished to Bendix. Sequencing of power to motor phases was variable, Y motor power intermittent, Z motor power disabled.

TABLE 3.3.4-1 (CONT.)

	Discrepancy	ICS Paragraph	ICS Value	Acceptable Value to Bendix	Remarks
6.	Intermittent Z Offset Display	3.2.2.3.4	NA	NA	Improper response of Z offset noted in breadboard. The EM model indicated Z offset was intermittent between 0 and +50%.
7.	Transients in X, Y and Z Axis Data	NA	NA	NA	Occurred with and without digital filter in. Analog raster X axis from ETS indicates less noise with filter out.
8.	Z Offset Cycle Incorrect	NA	NA	NA	Z offset cycle in response to sequence of commands responds with +75, +25, 0, +75, +50, +25, and 0. X and Y axis respond +25, +50, +75, -75, -50, -25, and 0. Status bits for offsets are opposite value given in ICS Table IV.
9.	Data Level at 1.8V Between Demand Intervals	3.2.2.2	0-+0.4V	0-+0.4V	Problem corrected temporarily on EM by addition of 3.9K resistor between demand and signal ground on SBOB.
10.	LSM Not in Proper Preset Condition on Turn On	NA	NA	NA	CA/Inhibite not in.
11.	Calibrate Raster From Analog Output of ETS Garbled	NA	NA	NA	X-axis calibrate raster from ETS analog output was garbled with digital filter in. With filter out raster appeared better but was displaced due to permanent offset in the sensor or sensor electronics.

TABLE 3.3.4-1 (CONT.)

	Discrepancy	ICS Paragraph	ICS Value	Acceptable Value to Bendix	Remarks
12.	Permanent Offset Believed to be in Sensor Electronics Would Not Allow Flux Tanks to Zero Data Channel	NA	NA	NA	
13.	Power Ripple Inconsistent	NA	NA	NA	Power ripple unexplainably changes from its characteristic signal intermittently during normal operation of LSM.
14.	No Z Axis Flip Electronics	NA	NA	NA	Z axis flip electronics missing as reported to Bendix by Philco. X and Z axis science channels were connected together with opposite sign.
15.	Engineering Data for Words 4 and 12 Unstable	NA	NA	NA	Data in word 4 and 12 of LSM sequence shifted between 002 and 127 decimal. Unknown if active or dummy sensor used for Engineering status.
16.	Y Sensor Position in, not 0^{o}, 90^{o} or 180^{o} during Flip Cal	NA	NA	NA	Y Sensor Motor supposedly disabled although Y motor power appeared intermittent. Unknown which position sensor should be in although normal position is 0^{o}.
17.	X and Z Data Read Same Sign During Flip-Cal Cycle	NA	NA	NA	Z channel supposedly connected to X channel because of disabled Z motor. This resulted in normal reversal of sign, i.e., -X and +Z with same absolute magnitude. Both signs were positive during part of flip cal sequence.

TABLE 3.3.4-1 (CONT.)

	Discrepancy	ICS Paragraph	ICS Value	Acceptable Value to Bendix	Remarks
18.	Science Mode Status Indicated During Flip Motor On	NA	NA	NA	Status bits changed from cal to science mode during flip motor power on.
19.	X, Y, and Z Data Channels Saturated Inconsistently During Flip-Cal	NA	NA	NA	
20.	Data Levels Before and After Flip-Cal are Inconsistent	NA	NA	NA	
21.	Engineering Data 16 Frame Sub-Commutator Stops Intermittently, Skips and Jumps Forward	3.2.2.2	Table III	Table III	
22.	Logic and Power Switching Logic Apparently Unduly Sensitive to EMI	3.2.5		MIL-I-26600 Amended by MSL-ASPO-EMI-10A	Power glitches occurred intermittently and during switching of Sandborn recorder. Science data glitches accompanied the power glitches.

TABLE 3.3.4-1 (CONT.)

	Discrepancy	ICS Paragraph	ICS Value	Acceptable Value to Bendix	Remarks
23.	Channels 6 & 7 Engineering Data Change During Flip/Cal	NA	NA	NA	Channel 6 is normally @ 42 changes to 38. Channel 7 is normally @ 10 changes to 11. It is not known if real or dummy level sensors are used for EM.
24.	Z Offset Changes During Flip/Cal	NA	NA	NA	Z changes to +50% at beginning of flip cal, returns to 0 during flip.

b. Induced by Recorder — 100 ma, approx. 100 ms,

EMI (Two variations noted) — 80 ma, 1.2 sec.

6. Site Survey — Not Tested

Figure 3.3.4-4 is a Sandborn recording of the flip cal current level. Current noise spikes are present before and after the sequence. Figure 3.3.4-5 depicts a current glitch induced by switching speeds on the Sandborn recorder, a known source of EMI because of its ability to initiate SBOB command initiation lamps.

The turn on power surge was limited by a 50 ohm series resistance in or manner similar to that used for the breadboard. The PDU circuit breaker was adjusted from 450 ma to approximately 645 ma to keep the motor current transient from tripping the breaker. Flipping of the motor caused SIDE, and at times SWS, to ripple off.

Commands

Command response was normal with exception of the site survey command which was not attempted. Advance notice was given to BxA by ARC that the site survey mode of the LSM was inoperative.

Timing and Data Signal Waveforms

Two differences between the breadboard and Engineering Model were noted. First, the data bit reset on the trailing edge of the shift pulse for data from the X and Z axis, while the Y axis data reset on the trailing edge of the demand pulse. Figure 3.3.4-6 depicts this condition. Second, noise was observed on the data as shown in Figure 3.3.4-6. Both these differences apparently did not effect subsystem operation.

Flip Cal Raster

Pre flip cal raster and power profile changed from that seen on the breadboard. The Y and Z axis motors were supposed disabled. However, through the tests at Bendix, the Y axis motor power was intermittent. Turn on of the two phases of the motor appeared backward from that seen on the breadboard. The normal sequence appears to be turn on with both phases, then turn off the control phase. The usual mode for the Engineering Model appeared to be backwards, i.e., control phase only, followed by both, then off. On at least one occasion the sequence appeared correct.

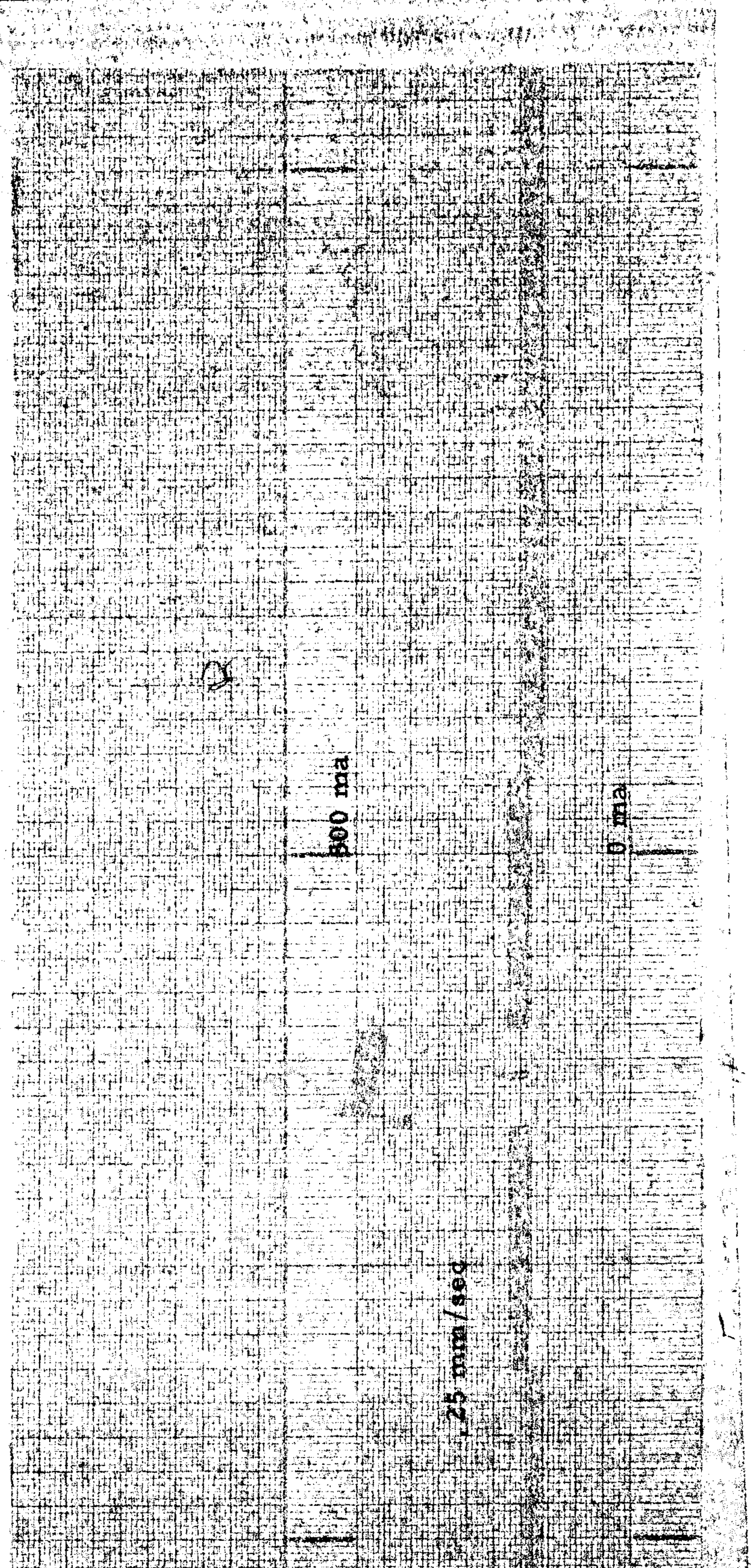


Figure 3.3.4-4 LSM Flip-Cal Current Profile with Noise Spikes

500 ma

0 ma

Figure 3.3.4-5 LSM Current Glitch From Recorder Speed Switch

5V/cm
2V/cm
1ms/cm

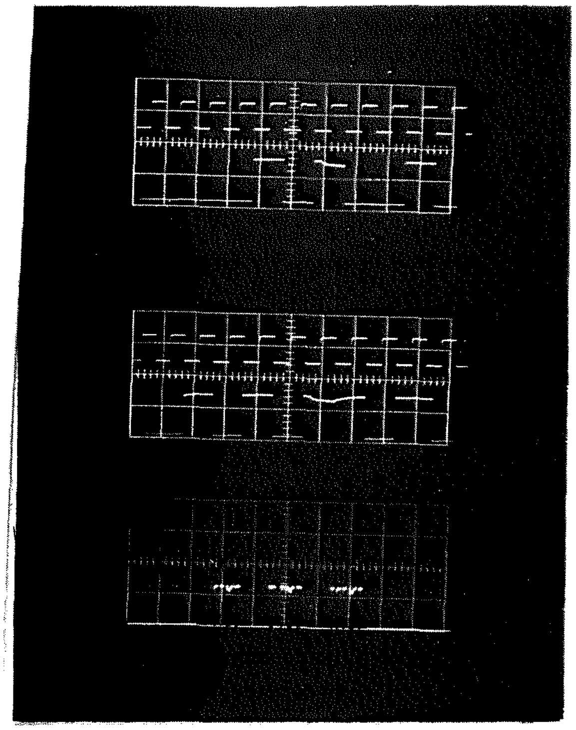
Shift Pulse
Word 5 Data

5V/cm
2V/cm
1ms/cm

Shift
Word 17 Data

2V/cm
10ms/cm

Words 17, 19, and 21



Shift and Demand Pulse
Word 21 Data

Data and
Shift 2V/cm
Demand 5V/cm
All 500 s/cm

Shift and Demand Pulse
Word 19 Data

Shift and Demand Pulse
Word 17 Data

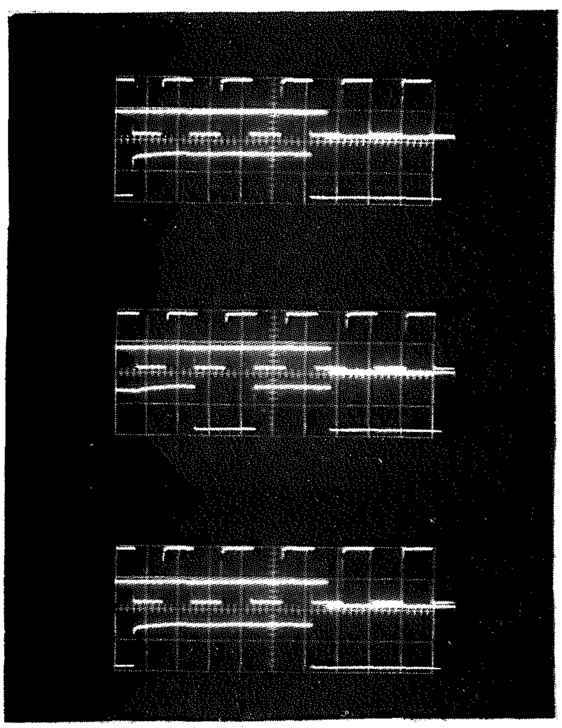


Figure 3.3.4-6 LSM Timing, Control and Data for Data Processor X

The cal raster was distorted. Figure 3.3.4-7 shows the cal raster from the X axis along with the power profile. With the digital filter in, the raster was quite confused. With the filter out the raster appeared better, however, a fixed offset which could not be nulled out, prevented obtaining a normal raster.

Downlink Performance

Downlink performance appeared normal but was difficult to determine because of jitter on the experiment status and problems in the DDS-1000 console. Therefore, confirmation of downlink performance was left to Category #4 tests.

3.3.5 Suprathermal Ion Detector - Category #2

Only Category #3 and #4 tests were performed on the SIDE/CCGE breadboard during this report period. The results of its Category #2 tests are reported in the January Progress Report, ATM-618.

3.3.6 Active Seismic Experiment Category #2

Only limited tests on the ASE were accomplished during this period due to difficulties with the experiment and the requirement to proceed with Category #3 and #4 testing on Array A.

Initially the experiment could not be turned on by the Central Station due to the design of the circuit protection circuits. The experiment circuit breakers on the +5V, +12V, -12V and +15V lines were tripping by the ASE turn-on transient. This fault was due to a logic design error which was not apparent on subsystem tests. A redesign was made in which the protection circuits are momentarily inhibited to tolerate a turn-on transient and are reset to provide circuit protection to the Central Station when the ASE turn on is complete.

The ASE was put in operation by inhibiting the protection circuits. The ASE's functional operation with the Central Station and Data Output Monitor Equipments appears good. The " time break" signal was received properly and the detonation time decoded. All timing and control signals appeared normal and were photographed. Further Category #2 tests on ASE will be conduced in mid March.

Subsystem tests of the ASE EM detected occasional false "time break" signals due to the inherent noise in the ASE receiver. A biasing circuit on the receiver output was incorporated in the EM and subsequent models to eliminate this fault.

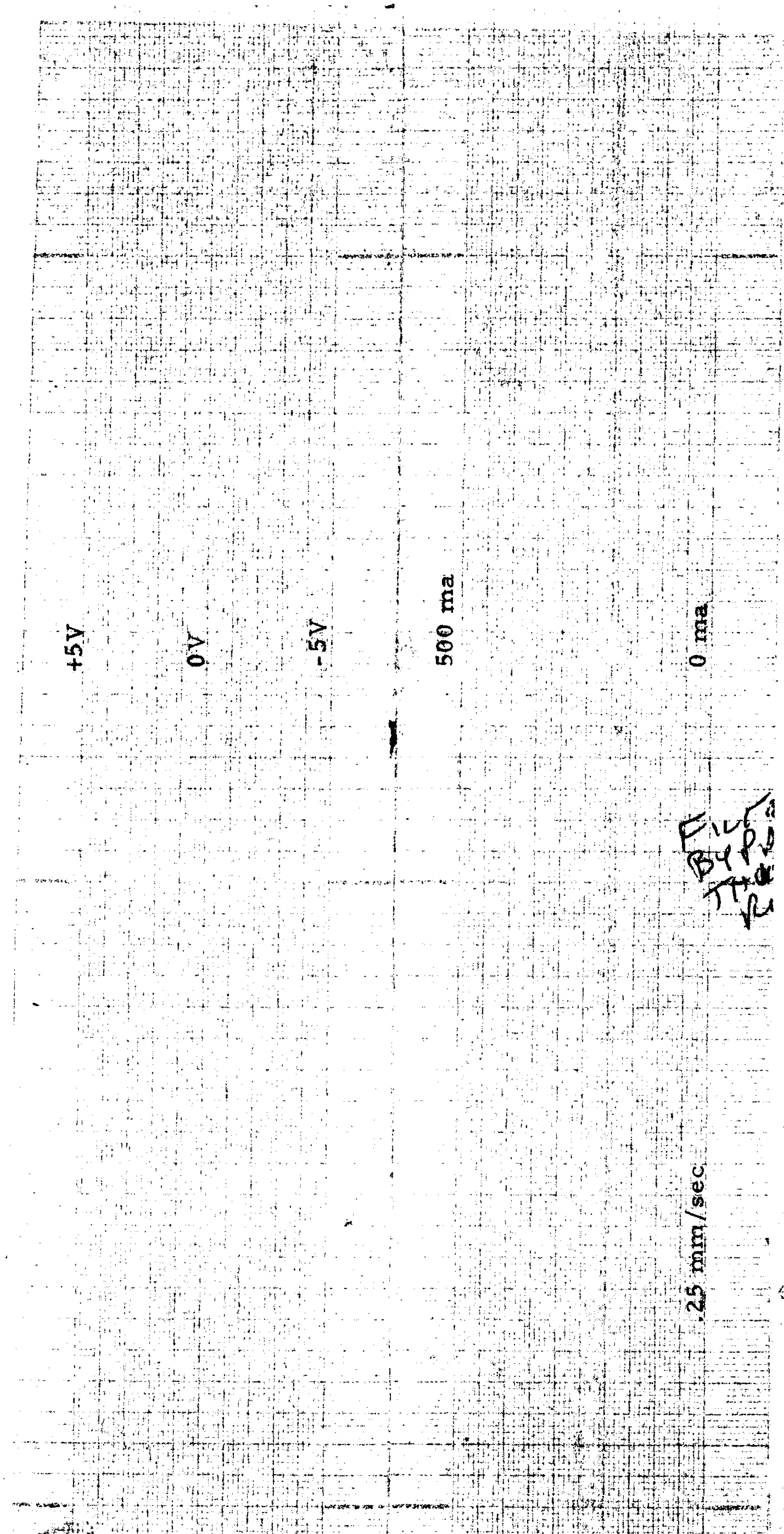


Figure 3.3.4-7 LSM Flip, Cal Current Profile and X Axis Analog Signal from ETS

3.3.7 Dust Detector

The EM model of the Dust Detector operated on the system for several days and checks of its output in word 33 were made. All interfaces appear normal.

The cause of the unpredictable variation in the output of the Dust Detector described in ATM-617 (3 February 1967) were isolated during February. The variations were proven to result from a DC offset at the input of the DD differential amplifier. This offset was due to a significant current flowing in a long ground return path. The design change between the EM and prototype eliminates this problem. These tests necessitated changing the gain of the amplifier from 50 to 31 to account for the increased signal amplitude upon elimination of the DC offset.

3.4 CATEGORY #3 TESTS

3.4.1 Scope of Tests

Category #3 tests of the Array "A" EM configuration commenced on 13 February 1967. The object of Category #3 tests is to confirm and demonstrate that no detrimental interactions arise from the normal operation of the Central Station Data and Power Subsystems and the four Array A experiments.

All the normal functions of the ALSEP system were checked, and the tests performed summarized as follows:

1. <u>Power Subsystem:</u>

   Power turn on, power line quality, experiment overload protection interactions, power relief sequencer interactions.

2. <u>Data Subsystem</u>

   Central Station experiment interface signals.

3. <u>Experiments</u>

   Central Station and experiment command response and interactions.

4. <u>PCU Changeovers</u>

   Interactions.

5. <u>Back-up Timer Sequence</u>

   One time only response, 12 hr repetitive sequence response.

6. Astronaut Control Switch

Experiments ON.

3.4.2 Power Subsystem

Power Turn On

The experiment turn on sequence for Array A, i.e., PSE, LSM, SWS, SIDE was followed. The only deviation from the planned sequence arose due to the necessity of using an external current limiting resistor with the EM LSM, which has to be manually removed following LSM turn on. No significant problems arose with this sequence even with the RTG simulator adjusted to the specification minimum of 56W. The system apparently recovered virtually instantaneously from the momentary power system overloads associated with SWS and SIDE turn-on transients. A check of the downlink data during these overload transients will be performed during Category #4 tests when the STS software is fully operational.

Experiment Overload Protection Interactions

No interactions were detected when individual experiments were tripped off by applying overloads to the +29V line downstream of the experiment circuit breakers. Examination of the downlink data during the overload transients will be performed in Category #4 tests.

Power Relief Sequencer Interactions

The power relief sequencer performance was checked both by applying preselected values of load to the PCU +29V output to sequence off one, two or three experiments, and also during the normal LSM sensor flip. If the EM LSM load during the sensor flip produces a power overload during or near the peak of the SWS power profile, the SIDE is rippled off by this peak load. Otherwise no interactions due to this circuit were observed. Again the examination of the data during relief sequencer operation is one of the Category #4 tests.

Power Line Noise

Photographs of the power line noise were taken for both voltage and current noise at each experiment's breakout box. The noise was essentially the same as that seen in Category #2 tests. Each experiment's contribution can be determined by simply noting its characteristic power converter repetition period.

Experiment	Repetition Period
1. PSE	19 μsec
2. SWS	230 μsec
3. LSM	10 μsec
4. SIDE/CCGE	96 μsec

A majority of the photographs were taken at fairly fast speeds in an effort to depict the power converter repetition rates. At lower sweep speeds, the PCU ripple is the dominating signal. Figure 3.4-1 is typical of the PCU noise at the Central Station and experiment SBOB with experiments off. At the faster sweep speeds Central Station high frequency noise can be seen, as shown in Figure 3.4-2. This noise shifts in frequency from 1.2 MHz to approximately 4.5 MHz. Its source has not been thoroughly investigated and it appears to maintain an amplitude of 20 mV and to shift from day to day. The noise appears to be associated with the shift pulse signal at times. Figures 3.4-3 to 3.4-14 shows the same noise characteristic at the PSE, LSM, SWS and SIDE SBOB's when all experiments are on.

Of all experiments, the PSE appears to be the largest contributor of noise. Its characteristic ringing is clearly depicted at all SBOBs. The second largest contributor is the SIDE breadboard. It's characteristic noise can usually be seen at all experiment SBOBs, mixed with the PSE noise. Photographs using random single sweep were made to avoid misleading results dependent on sync level. SWS is the next contributor to transient with LSM being the least. The SWS voltage noise is difficult to see with all experiments running because of its relatively long repetition period. Sweep speed of 50 to 100 μsec/cm are required to resolve this noise and the LSM noise photograph of Figure 3.4-6 shows the complexity of the signal at this speed.

3.4.3 Data Subsystem

The interface timing signals between the Central Station and experiments were examined for excess noise with all experiments operating. No unacceptable noise levels were observed.

3.4.4 Experiments

The system command response was checked with all Array A experiments operating, using command sequences for both central station control and for the individual experiments. During this test, the experiments which were

Internal Scope Sync

All traces 200 mV/cm

50 μs/cm

PCU +29V
SWS +29V at SBOB

200 μs/cm

PCU +29V
SWS +29V at SBOB

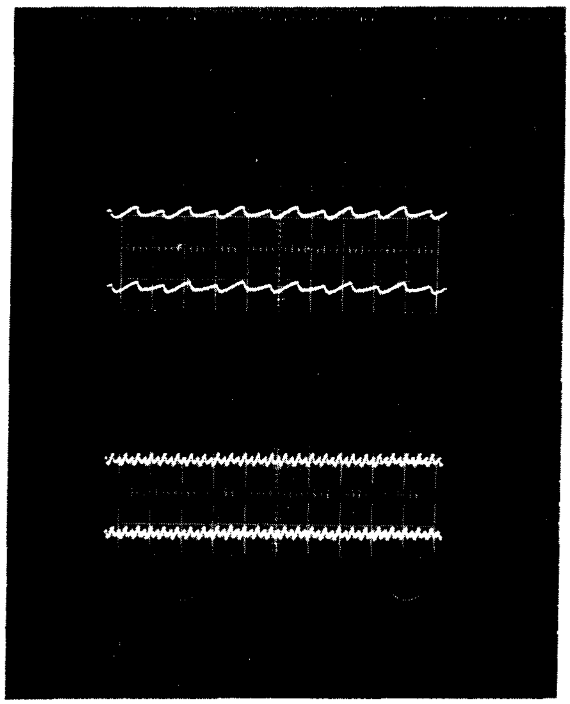


Figure 3.4-1 PCU +29V Voltage Noise at the Central Station, all Experiments off. SWS 100 ma Dummy Load on at SBOB.

Scope Sync to Shift Pulse

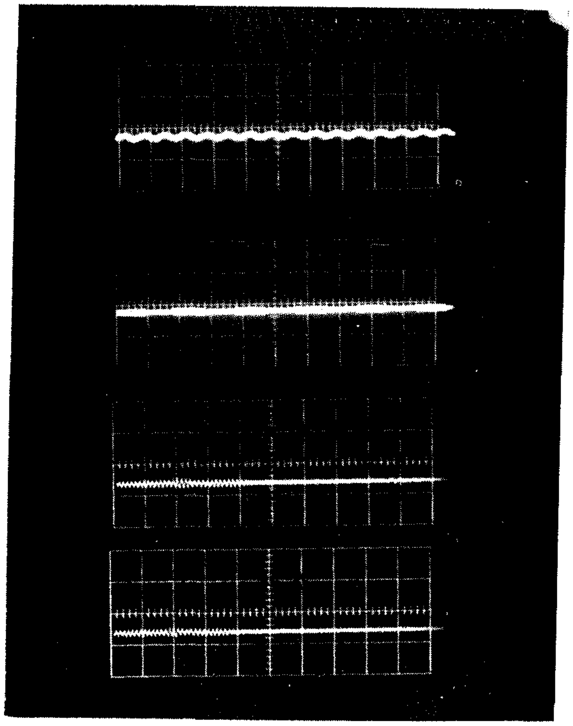
All Traces 50 mV/cm

1 µs/cm

500 µs/cm

5 µs/cm

5 µs/cm



Single Sweep

All Traces 50 mV/cm

1 µs/cm

1 µs/cm

2 µs/cm

2 µs/cm

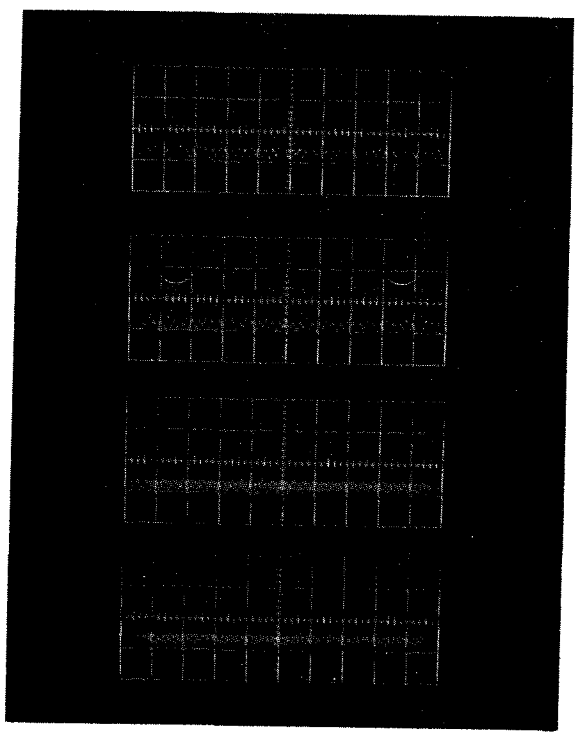
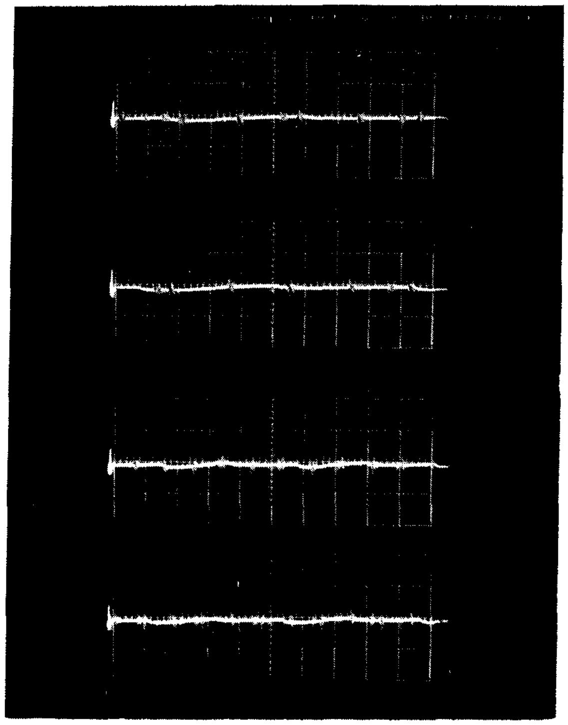


Figure 3.4-2 Central Station Noise, All Experiments Off, +29V Line



10 μs

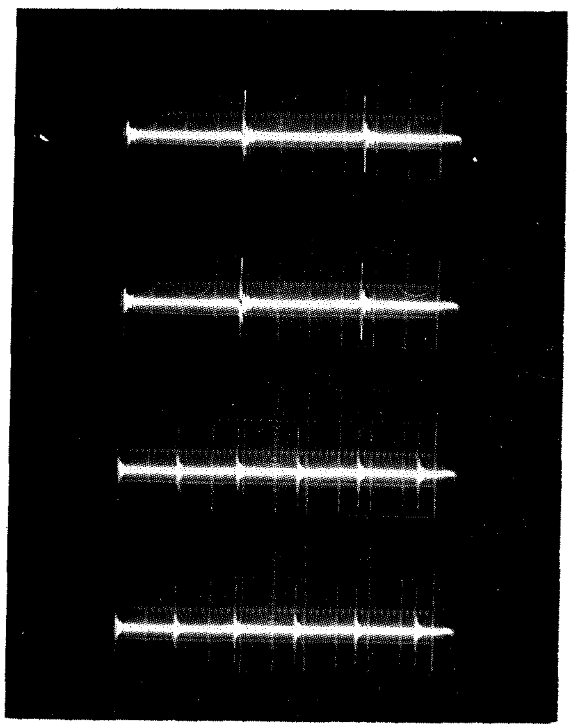
10 μs

20 μs

20 μs

Random Single Sweep

All Traces
500 mV/cm



5 μs/cm

5 μs/cm

10 μs/cm

10 μs/cm

Internal Scope Sync

All Traces
500 mV/cm

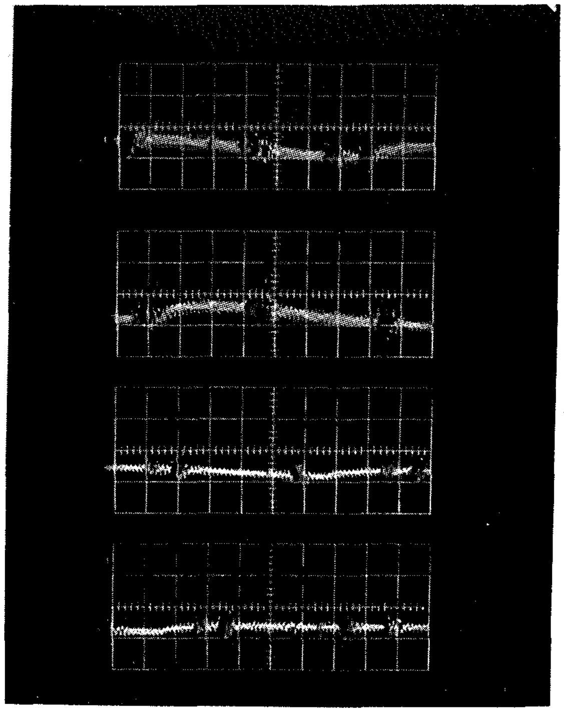
Figure 3 4-3 PSE +29V Voltage Noise,
All Experiments On

100 mV/cm

100 mV/cm

200 mV/cm

200 mV/cm



Random Single Sweep

All Traces
5μs/cm

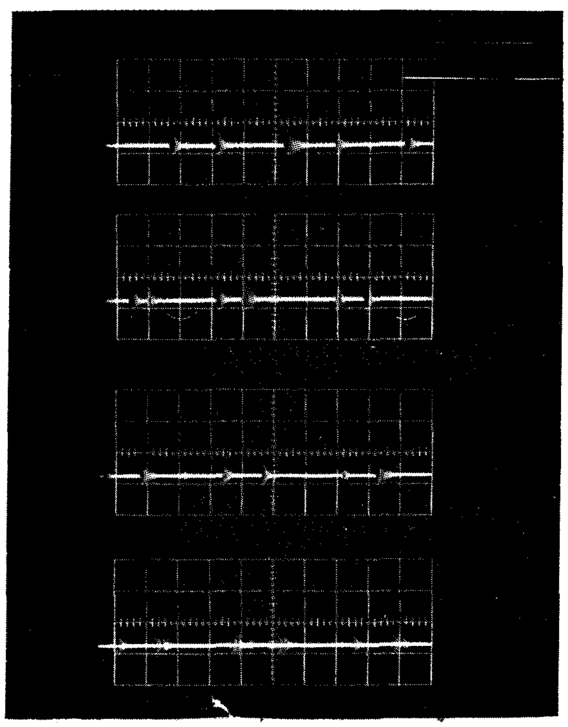
Figure 3.4-4 PSE +29V Voltage Noise,
All Experiments On

50 mA/cm

50 mA/cm

100 mA/cm

100 mA/cm



Internal Scope Sync

All Traces
5μs/cm

Figure 3.4-5 PSE +29V Current Noise,
All Experiments On

Random Single Sync

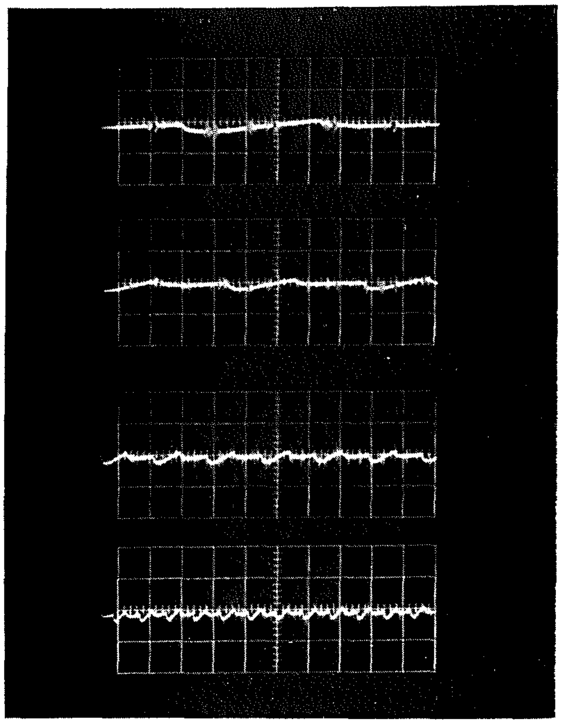
All Traces
200 mV/cm

10 μs/cm

20 μs/cm

50 μs/cm

100 μs/cm



Internal Scope Sync

10 μs — 200 mV/cm

20 μs — 200 mV/cm

50 μs — 200 mV/cm

100 μs — 100 mV/cm

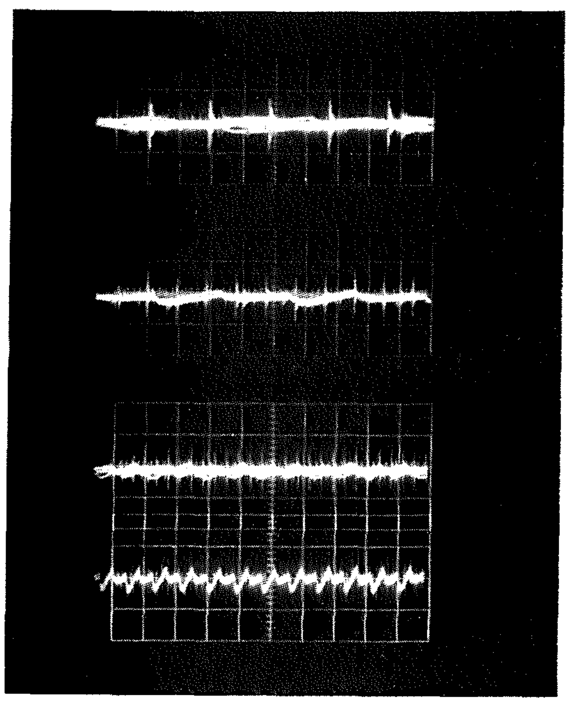


Figure 3.4-6 LSM + 29V Voltage Noise,
All Experiments On.

Random Single Sweep

All Traces
5 μs/cm

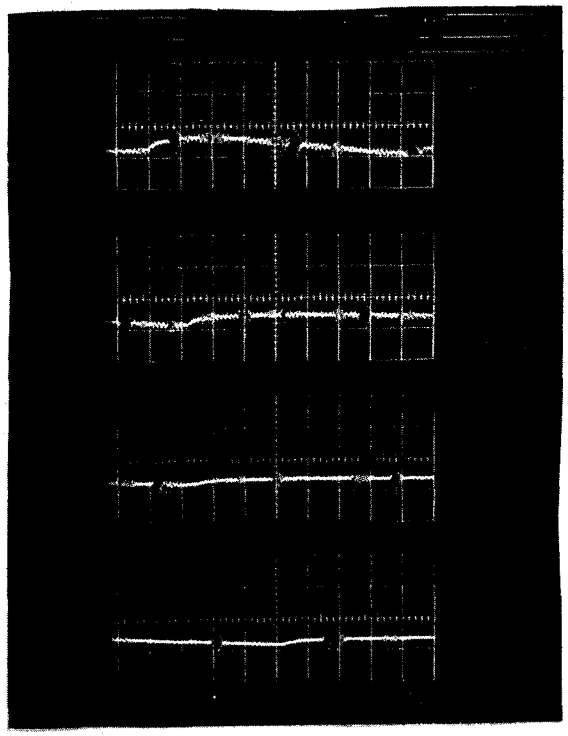


Figure 3.4-7 LSM +29V Voltage Noise, All Experiments On

Random Single Sweep

All Traces
50 mA /cm
5 μs/cm

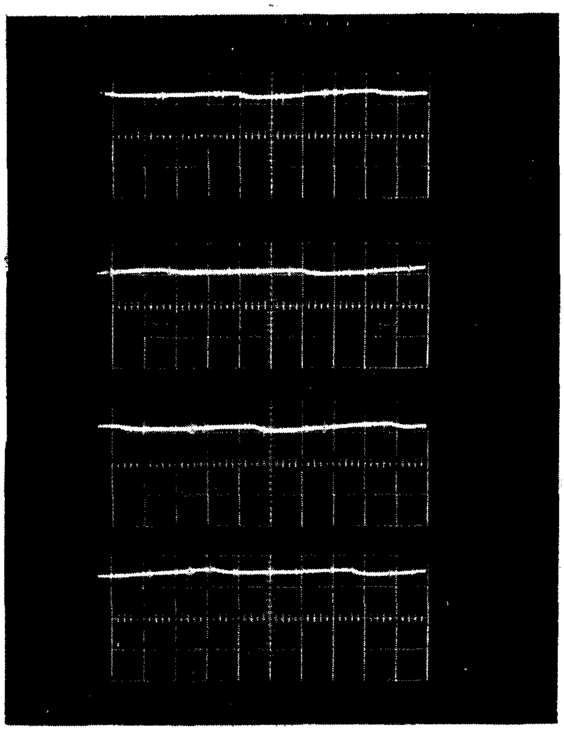


Figure 3.4-8 LSM +29V Current Noise, All Experiments On

Random Single Sweep

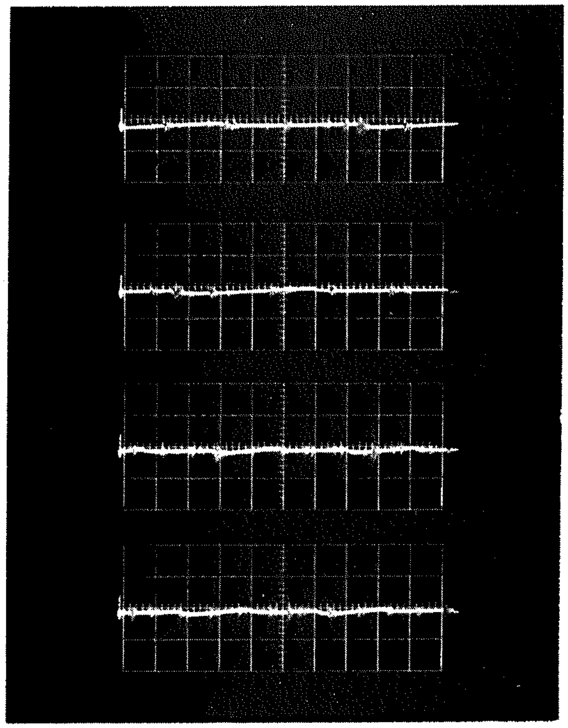
All Traces
500 mV/cm

10 μs/cm

10 μs/cm

20 μs/cm

20 μs/cm



Internal Scope Sync

All Traces
500 mV/cm

10 μs/cm

10 μs/cm

10 μs/cm

20 μs/cm

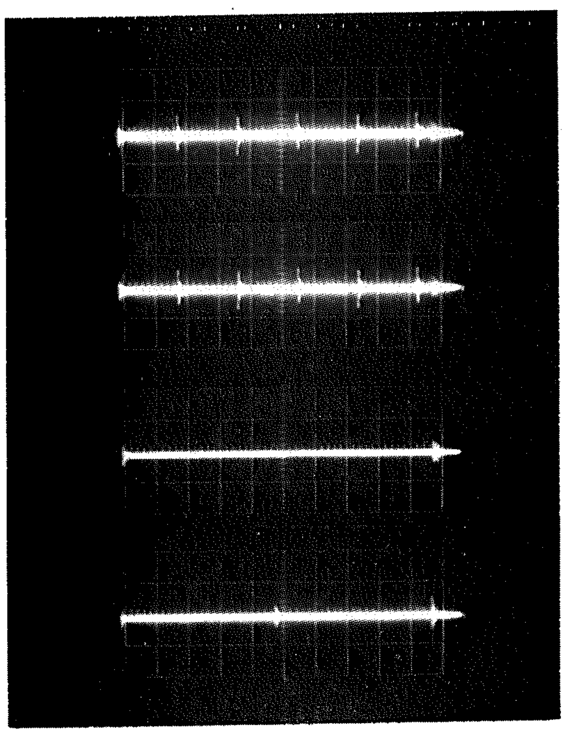


Figure 3.4-9 SWS +29V Voltage Noise,
All Experiments On

Random Single Sweep

All Traces
5μs/cm

100 mV/cm

100 mV/cm

200 mV/cm

200 mV/cm

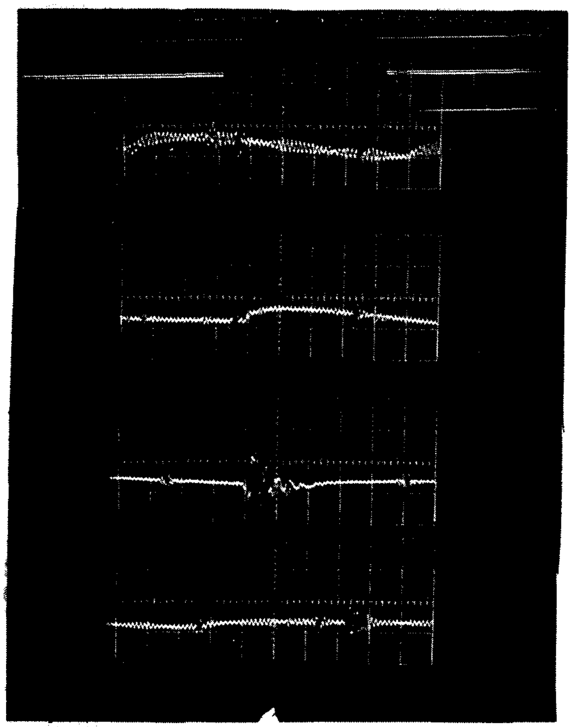


Figure 3.4-10 SWS +29V Voltage Noise, All Experiments On

Random Single Sweep

All Traces
100 mA/cm
10μs/cm

Zero at Bottom of Grid

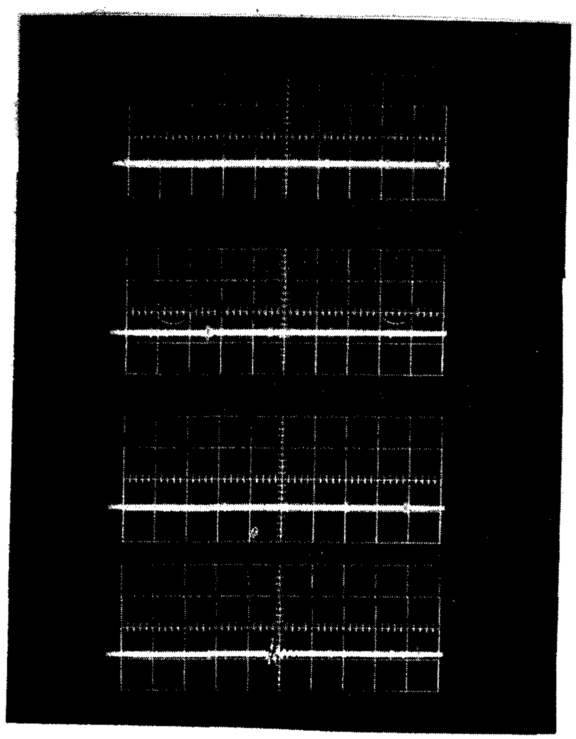


Figure 3.4-11 SWS +29V Current Noise, All Experiments On

Random Single Sweep

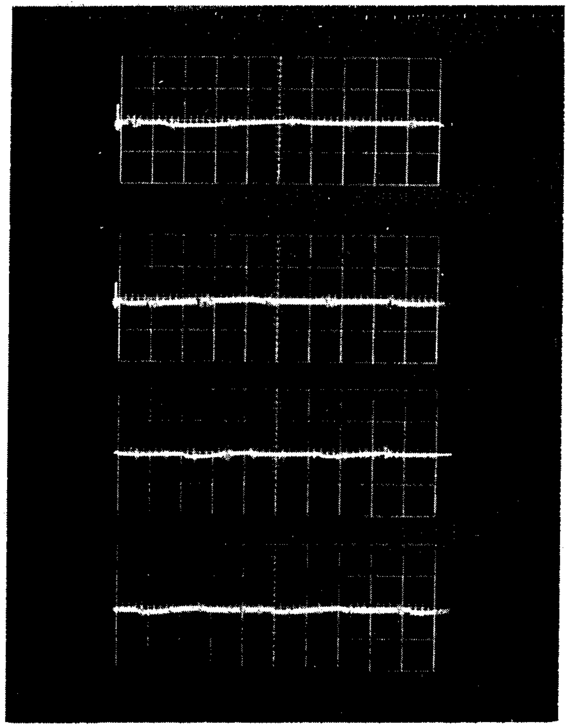
All Traces
500 mV/cm

10 μs/cm

10 μs/cm

20 ms/cm

20 μs/cm



Internal Scope Sync

All Traces
500 mV/cm

10 μs/cm

10 μs/cm

20 μs/cm

20 μs/cm

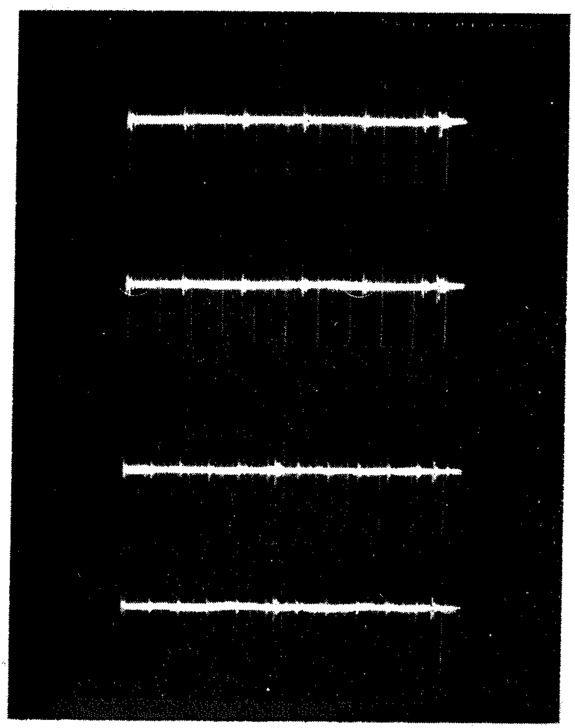


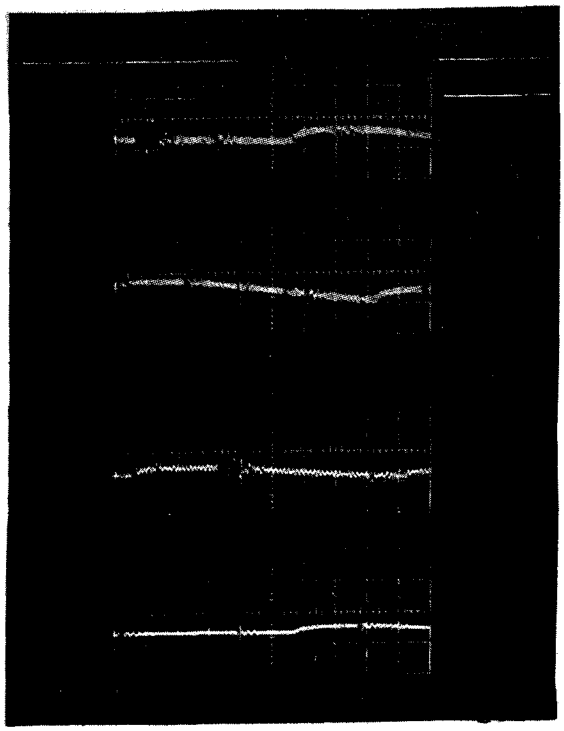
Figure 3.4-12 SIDE +29V Voltage Noise,
All Experiments On

100 mV/cm

100 mV/cm

200 mV/cm

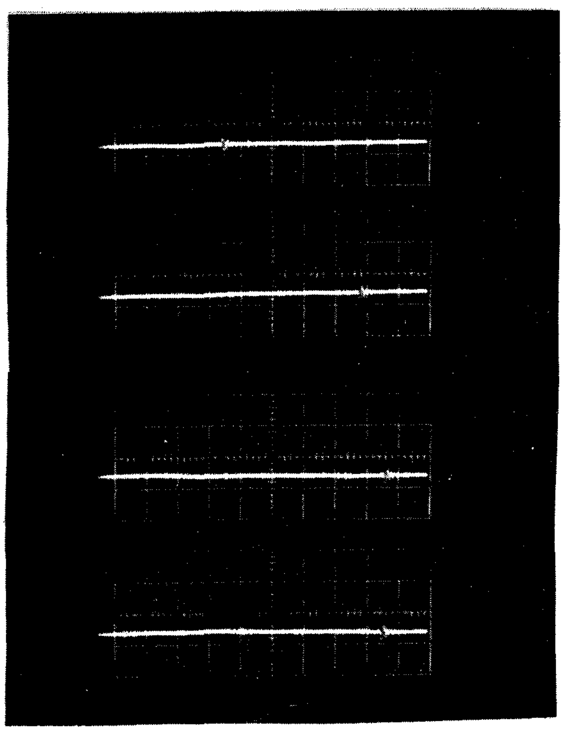
200 mV/cm



Random Single Sweep

All Traces
5μs/cm

Figure 3.4-13 SIDE +29V Voltage Noise, All Experiments On



Random Single Sweep

All Traces
10μs/cm
50 mA/cm

Figure 3.4-14 SIDE +29V Current Noise, All Experiments On not being directly addressed were set in their reset mode, and the operating mode status of the experiments was verified by the ETS's. This test proved that there are no major interactions which would permanently affect the operating mode of an experiment in its reset mode. More sophisticated tests in which:

1. The science data will be checked.

2. The experiments will be run in other major operating modes; will be performed using the STS in Category #4.

3.4.5 PCU Changeovers

PCU changeovers were performed with the entire system operating, including changeovers with the RTG simulator adjusted for 56W output. From the behavior of the power system observed during Category #1 tests, it was anticipated that SIDE would be rippled off during a PCU changeover. This occurred on commanding the changeover with the system operating. Records were taken showing the power system being driven out of regulation for 60 to 70 ms by the central station and experiment power convertor transients at changeover. This is followed by a smooth and rapid recover. No changes in experiment operating mode status, other than the SIDE ripple off, were observed on the ETS's displays. More detailed tests will be made using the STS in Category #4, checking both alternate experiment operating modes and the science data.

3.4.6 Astronaut Control Switch #3 (Experiments On)

The "Experiments On" Astronaut Control Switch was successfully operated and all experiments came on into normal operating modes. The PCU regulators went for a period of about 70 msec, then settled down smoothly. This test began with an unloaded regulator and the reserve was not quite totally consumed by the sum of all turn on transients.

3.4.7 Back-Up Time Command Sequence

Both the one time only and the repetitive back-up timer sequences were successfully tested by simulating 12 hr and 1 min. closures with push-buttons. The CCIG seal and SIDE and SWS dust cover blows were properly executed during the one-time sequence. The LSM on flip/cal and the SIDE on commands were properly executed during the repetitive sequence (every 12 hrs).

3.5 STS INTEGRATION TESTS

The integration of the STS, the Data Subsystem Checkout Program and EM Central Station occurred on 4, 6, and 7 February 1967. The purpose of the tests was to establish the hardware/software compatibility and to isolate any undetected problems. The STS hardware used in this test include the Data Units and the DPS 2000 Programmer - Processor. Figure 3.5-1 shows the STS in use with the EM.

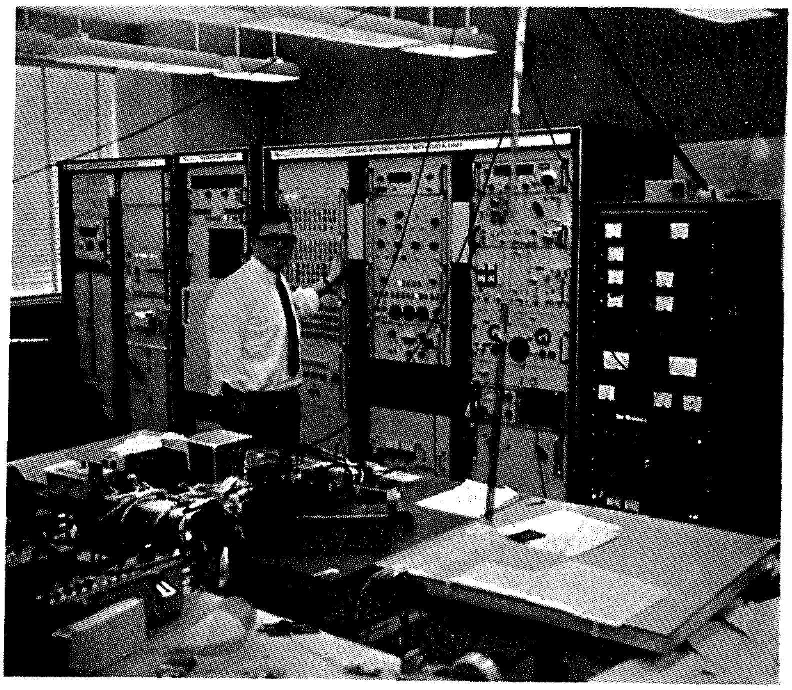


Figure 3.5-1 System Test Site In Use With Engineering Model

The tests were highly successful in that the experiment simulators and STS - Data Subsystem Checkout Program ran as anticipated with the EM Central Station. These tests include data transmission, command transmission (both manual and auto modes), printing of housekeeping data, output out-of tolerance and data change housekeeping words, mode identification, time identifications, and time markers, main frame subframe status syncronization of main frame and subframe, and resyncronization/reinitialization of program due to errors or bit stream drop out. Satisfactory RF operation was achieved throughout the tests. Only minor easily corrected or known hardware and software incompatibilities were encountered. Examples of items corrected are:

1. Excessive crosstalk in experiment simulator cabling because of sharp rise and fall times of experiment simulator output pulses.

2. Diagonal line print out by STS printer.

3. STS computer attempting two simultaneous operations gave a false indication that one (even frame mark error check) was in error.

4. Anticipated fault in 90th frame mark check which does exist in EM

3.6 CATEGORY #4 TESTING

Array "A" Category #4 testing began during this period. The primary purpose of this category is to integrate the Central Station and each experiment to its STS software, thus preparing the software for prototype testing. The STS software then allows long term observation of data and detection of errors in the Central Station and experiment's output data that would not be observed in preceeding tests. These malfunctions are caused by experiment faults or interactions between the various experiments. During this period, the software for each Array A experiment (PSE, LSM, SIDE, & SWS) was run with the experiment. In each case program bugs were discovered and efforts expended to correct them.

The early effort was concentrated on the LSM since this experiment was returned on 1 March. The intrepretation LSM program data outputs was improved as a result of actual experience and was completely debugged in preparation for prototype tests. The other software is partially debugged.

In addition, approximately 3 hours of Central Station output bit stream was recorded with Array A experiments operating. This is to be used later for a final check of Array A software on PSE, SWS, & SIDE since the LSM is no longer available.

3.6.1 LSM Category #4

Program modifications, improvements, and debugging were performed on the LSM software. An extended run was made using the operational program. This run revealed many experiment discrepancies previously undetected either because of poor operation of the LSM ETS or because the subtle nature of the discrepancy escaped manual means of detection. A detailed orderly record was obtained and is reported in the log of events for LSM of 2/28/67 which is given in Table 3.6-1-1.

Table 3.3.4-1 gives the discrepancies associated with LSM and its test set. Some of these (items 1 through 14) were first discovered during Category #2 and #3. The remainder (items 15 through 24) were discovered during Category #4.

3.6.2 PSE Category #4

The PSE software was tested with the experiment during this period. The outputs of this program are eight analog signals for the STS displayed on a photo process recorder. These channels represent X, Y, and Z long period; X, Y, and Z tidal; short period, and temperature. Sinusoidal and square wave signals were inserted into the sensor inputs of the PSE Central Station Electronics and were read out through the STS program and D/A onto the STS recorder. The digital data was also intercepted at the SBOB and converted by the test set to analog signals which were then recorded on the ETS strip chart.

The ETS data appeared normal but that from the STS was erratic and noncorrelated. Hardware problems in the D/A or STS strip chart recorder were suspected and debugging commenced on these items. The recorder was discovered to defective and is to be repaired by the manufacturer. A second recorder has been substituted and the program will be rechecked in the near future.

3.6.3 SIDE Category #4

The SIDE software was run with the experiment during this period. The software successfully decommutates, prints out, and performs limit checks on the data. However, it was discovered that the program parity checking portions were not performing correctly. The SIDE creates even parity on 51 bits rather than odd parity as called out in the ICS. The program runs also showed that the SIDE intermittently changed thesequence of velocity filter steps from SIDE frame 60 through 120. Debugging and change to even parity are continuing.

TABLE 3.6.1-1

LOG OF EVENTS DURING LSM CATEGORY #4 TESTS

Event or Command	Time	Response		Test Condition
Thermal Control Select	11:08:49	X - Heater Off		All experiments ON
Range Select	11:11:27	100		LSM Filter In
" "	11:11:49	200		
" "	11:12:06	400		
" "	11:12:22	100		
" "	11:12:35	Too Fast*		
" "	11:12:38	400		
Ratchet	11:12:48	X		
Offset	11:13:09	+25%	010	
"	11:13:20	+50	001	
"	11:13:36	+75	000	
"	11:13:51	-75	110	
"	11:14:17	-50	101	
"	11:15:03	-25	100	
"	11:15:48	0	011	
Ratchet	11:16:19	Y		
Offset	11:16:25	+25%	010	
"	11:17:35	+50	001	
"	11:18:15	+75	000	
"	11:18:40	-75	110	
"	11:19:17	-50	101	
"	11:19:50	-25	100	
"	11:20:15	0	011	
Ratchet	11:20:29	Z		
Offset	11:20:47	+75%	000	
"	11:21:07	+25%	010	
"	11:21:40	0%	011	
"	11:23:17	+75%	000	
"	11:23:52	+50%	001	
"	11:24:19	+25%	010	
"	11:24:48	0%	011	
Ratchet	11:25:23	Off		
Flip-Cal Inhibit	11:25:42	Inhibited		
Thermal Control Select	11:26:32	Y - Heat On		
" " "	11:27:09	X - Heat Off		
Eng. Channel #4 Error	11:28:52			
SIDE Standby	11:29:27	Too Fast		
SIDE Off	11:29:31	Experiment Off		
SWS Standby	11:29:32	Too Fast		
SWS Off	11:29:36	Experiment Off		
PDM #1 On	11:29:41	PDM #1 On		
PSE Standby	11:29:42	Too Fast		

*Too Fast. Subsequent command received before command confirmed.

Event or Command	Time	Response		Test Condition
PSE Off	11:29:44	Experiment Off		Other Experiments OFF
Range Select	11:30:16	100		
" "	11:30:27	200		LSM Filter In
" "	11:30:40	400		
Ratchet	11:30:43	X		
Offset	11:31:01	+25%	010	
"	11:31:12	+50%	001	
"	11:31:23	+75%	000	
"	11:31:34	-75%	110	
"	11:31:50	-50%	101	
"	11:32:03	-25%	100	
Eng. Channel #4 Error	11:32:06			
Offset	11:32:24	0%	011	
Ratchet	11:33:17	Y		
Offset	11:33:30	+25%	010	
Eng. Channel #4 Error	11:33:33			
Offset	11:33:41	+50	001	
"	11:33:51	+75	000	
"	11:34:03	-75	100	
"	11:34:15	-50	101	
"	11:34:25	-25	100	
"	11:34:40	0	011	
Ratchet	11:34:42	Z		
Offset	11:34:54	+75%	000	
"	11:35:06	+25	010	
"	11:35:24	0	011	
"	11:35:39	+75	000	
"	11:36:01	+50	001	
"	11:36:16	25	010	
"	11:36:29	0	011	
Eng. Channel #4 Error	11:36:35			
" " " "	11:36:55			
Ratchet	11:37:03	Off		
Filter In/Out	11:37:11	Out		
Thermal Control	11:37:18	Y - Heat on		
Eng. Channel #12 Error	11:37:23			
Eng. Channel #4 Error	11:37:28			
Thermal Control	11:37:35	X - Heat Off		
Flip-Cal. Inhibit	11:37:41	Not Inhibit		
Filter In/Out	11:37:44	In		
Eng. Channel #4 Error	11:38:12			
" " " "	11:38:22			
" " " "	11:38:32			
Eng. Channel #12 Error	11:38:57			
Eng. Channel #4 Error	11:40:03			
Eng. Channel #12 Error	11:40:08			
Eng. Channel #4 Error	11:40:13			
Eng. Channel #12 Error	11:41:25			

Event or Command	Time	Response	Test Condition
Eng. Channel #4 Error	11:41:40		
Eng. Channel #12 Error	11:41:45		
Eng. Channel #4 Error	11:41:50		
Eng. Channel #12 Error	11:41:55		
Eng. Channel #4 Error	11:42:00		
Eng. Channel #4 Error	11:42:10		Other Experiments Off
Flip-Cal Initiate	11:42:21		LSM Filter In
Y False (00 in Ch. #2)	11:42:23	Error	8 Bit Science Data
Channel #4 Error	11:42:25		Tolerance
Chan. #6 from 042 to 038	11:42:26		
Chan. #7 from 010 to 011	11:42:27		
Z Offset from 0 to +50%	11:42:28	Error	
Cal. Mode	11:42:29	Correct	
Eng. Channel #12 Error	11:42:38		
Eng. Channel #4 Error	11:42:44		
Eng. Channel #12 Error	11:42:58		
Eng. Channel #4 Error	11:43:03		
Eng. Channel #12 Error	11:43:08		
Eng. Channel #4 Error	11:43:13		
Eng. Channel #12 Error	11:43:28		
Eng. Channel #12 Error	11:43:48		
Eng. Channel #4 Error	11:44:12		
Eng. Channel #12 Error	11:44:47		
Eng. Channel #12 Error	11:44:57		
Eng. Channel #4 Error	11:45:02		
Eng. Channel #12 Error	11:45:07		
Eng. Channel #4 Error	11:45:22		
Eng. Channel #4 & 12 Errors	11:45:32		
to	11:45:52		
Z returns to 0% Offset	11:45:57	Correct	
Eng. Channel #12 Error	11:46:04		
Eng. Channel # 12 Error	11:46:14		
Eng. Channel #4 Error	11:46:19		
" " " "	11:46:29		
" " " "	11:46:39		
Eng. Channel #12 Error	11:46:44		
Eng. Channel #4 Error	11:46:59		
X Sensor turned by hand to 0°	11:47:10		
X & Z Data same sign	11:47:15	Error	
to	11:47:25		
Eng. Channel 12 & 4 Errors	11:47:16		
to	11:47:36		

Event or Command	Time	Response	Test Condition
Eng. Channel 4 & 12 errors	11:47:47		
to	11:50:09		
Calibration Over	11:48:27		
Sci. Mode Confirmed	11:48:28	Correct	
Ch. 6 from 38 to 42	11:48:29		
Ch. 7 from 11 to 10	11:48:29		
Y Position to 180°	11:48:31		Other Experiments Off
Flip Cal. Initiate	11:48:58		
Y Position False	11:49:00	Error	LSM Filter In
Ch. 6 from 42 to 38 Eng.	11:49:03		8 Bit Science Data
Ch. 7 from 10 to 11 Eng.	11:49:04		Tolerance
X & Z Data has same sign	11:49:04	Error	
to	11:49:13	LSM 9 to LSM 9	
Z to +50% Cal. Mode	11:49:05	Z error, Cal Correct	
Ch. #4 & 12 Eng. Errors	11:49:25		
to	11:49:55		
Ch #4 Eng. Errors	11:50:10		
Ch. #12 Eng. Errors	11:50:15		
Ch. #4 Eng. Errors	11:50:26		
Ch. #12 Eng. Errors	11:50:31		
Ch. #4 Eng. Errors	11:50:36		
Ch. #12 Eng. Errors	11:50:41		
Ch. #4 &12 Eng. Errors	11:50:51		
to	11:53:36		
Sci. Mode & Motor On	11:51:30	Science Error	
X to 180°	11:51:42	Correct	
X to 0°	11:52:02	Turned Back by Hand While X Motor Still ON	
X Motor Off	11:52:04		
Y Motor On	11:52:08		
Z to 0% Offset & Cal Mode	11:52:27	Correct	
Y Motor Off	11:52:36		
X & Z have same sign	11:52:34	Error	
to	11:52:44	LSM 9 to LSM 9	
X, Y, & Z Data Dropout	11:53:04	Error	
Ch. #4 & #12 in Error** to end of record	11:53:41		
X & Z Have Same Sign	11:53:51	Error	
to	11:54:01	LSM 9 to LSM 9	
Sci Mode	11:55:05	Correct	
Ch. #6 from 38 to 42	11:55:06		
Ch. #7 from 11 to 10			
Y to 180°	11:55:08		
Flip Cal. Initiate	11:55:33		Other Experiments Off
Y to False Position	11:55:36	Error	LSM Filter In
Ch. #6 to 38 & Ch. #7 to 11	11:55:38		8 Bit Science Data Tolerance

**Channel #4 & #12 Continually in Error to end of Record

Event or Command	Time	Response	Test Condition
X & Z Have Same Sign	11:55:39	(Runs LSM 10 to	
	11:55:49	LSM 10 Data -93)	
Z Offset to +50%	11:55:40	Error	
X Motor On	11:58:03		
Science Mode	11:58:05	Error	
X Motor Off	11:58:33		
Y Motor On	11:58:37		
X Flip Confirmed (180°)	11:58:17	Correct	
Z Offset to 0% &	11:59:03	Correct	
Y Motor Off			
Chan. #6 38 to 42 to 38	11:59:59		
X Position to 0°	12:00:15	Reset by Hand	
All Data Chan. Saturated	12:00:30	(Exactly 3 LSM Cycles)	
to	12:01:00		
Science Mode	12:01:39	Correct	
Ch. #6 to 42, Ch. #7 to 10	12:01:40		
Y Position to 180°	12:01:42		
Filter In/Out	12:01:56	Filter Out	
Flip Cal Initiate	12:02:25		
Z Offset to 50% Cal Mode	12:02:28	Z Offset Error	
Ch. #6 to 38, Ch.#7 to 11			
Ch. #6 38 to 42 to 38			
Y Position to False	12:02:31	Error	
X & Z Axis Data Same Sign	12:02:36	(2 cycles LSM 9 to	
to	12:02:56	LSM 9 value -5)	
X, Y, Z Axis Data Saturated	12:03:52	(3 cycles LSM 9	
to	12:04:22	to LSM 9)	
X Motor On	12:04:57		
Science Mode	12:04:59		
X Flipped	12:05:03		
X Motor Off	12:05:05		
X Confirmed to 180°	12:05:11	Correct	
Y Motor On	12:05:09		
Y Motor Off	12:05:35		
Z Offset to 0% & Cal Mode	12:05:37	Correct	
X Position to 0°	12:06:22	Reset by Hand	
X, Y, & Z Data Saturated	12:06:55	Error	
to	12:07:25	LSM 9 to 9 three cycles	
Calibration Ended	12:08:00		
Science Mode	12:08:06	Correct	
Ch. #6 to 42 & Ch. #7 to 10	12:18:07		
Y Position to 180°	12:08:08		
Change From 8 to 0 Tolerance on Science Data			
Flip Cal Initiate	12:08:47	Other Experiments Off	
Y to False Position	12:08:48	Error	Filter In
Ch. #6 to 38 & Ch. 7 to 11	12:08:51		Zero Science Data tolerance

Event or Command	Time	Response		Test Condition
X & Z Same Sign Sci. Data	12:08:52	Error		
to	12:09:12	(LSM 9 to 9 two cycles)		
Z Offset to +50%	12:08:54	Error		
All Science Data Saturates	12:10:04	LSM 9 to 9-3 cycles		
to	12:10:34			
X Motor On	12:11:15			
Science Mode	12:11:19	Error		
X Flip	12:11:21			
X to 180° Confirmed	12:11:31	Correct		
X Motor Off	12:11:45			
Y Motor On	12:11:49			
Y Motor Off	12:12:18			
Z Offset to 0% & Cal Mode	12:12:18	Correct		
X to 0° Position	12:14:36	Reset by Hand		
Cal Ends	12:14:42			
Science Mode	12:14:52	Correct		
Ch. 6 to Ch 7 to 42 & 10	12:14:53			
Y Position to 180°	12:14:55			
Tolerance to ± 8 from 0	12:15:23			
PSE On	12:15:54	PSE On		
PDM #1 Off	12:16:03	PDM #1 Off		
SWS On	12:16:05	SWS On		
SIDE On	12:16:08	SIDE On		
Range Select	12:16:21	100 Gamma		All Experiments On
" "	12:16:40	200 "		LSM Filter In
" "	12:16:54	400 "		8 Bit Science
Ratchet	12:16:58	X		Data Tolerance
Offset	12:17:01	+25%	010	
"	12:17:12	+50%	001	
"	12:17:36	+75%	000	
"	12:17:54	-75%	110	
"	12:18:20	-50%	101	
"	12:18:36	-25%	100	
"	12:18:51	0%	011	
Ratchet	12:18:52	Y		
Offset	12:19:09	+25%	010	
"	12:19:22	+50%	001	
"	12:19:41	+75%	000	
"	12:19:53	-75%	110	
"	12:20:04	-50%	101	
"	12:20:15	-25%	100	
"	12:20:26	0%	011	
Ratchet	12:20:29	Z		
Offset	12:20:38	+75%	000	
"	12:20:51	+25%	010	

Event or Command	Time	Response		Test Condition
Offset	12:21:02	0%	011	
"	12:21:14	+75%	000	
"	12:21:25	+50%	001	
"	12:21:38	+25%	010	
"	12:21:53	0	011	
Ratchet	12:21:56	Off		
Thermal Control Select	12:22:48	Y - ON		
" " "	12:23:00	X - OFF		
Filter In/Out	12:23:09	In		
" " "	12:23:15	Out		
F/C Inhibit	12:23:49	Inhibited		
" "	12:24:04	Inhibit Out		
Filter In/Out	12:24:06	In		All Experiments ON
F/C Initiate	12:24:46	Calibration		Filter In
Chan. 6 to 38, Chan. 7 to 11	12:24:47			
X, Y, & Z Data Saturated	12:24:49	LSM 09 to LSM 09		8 Bit Science
to	12:25:19	3 frames		Data Tolerance
Z to 50% Offset and Cal Confirmed	12:24:51	Z Offset Error		
Y Position to False	12:24:55	Error		
All Data Saturated	12:26:06	LSM 09 to LSM 09		
to	12:26:36	3 cycles		
X Motor ON	12:27:12			
X Flip	12:27:16			
Science Mode	12:27:16	Error		
X Position to 180°	12:27:28	Correct		
X Motor OFF	12:27:41			
Y Motor ON	12:27:45			
Z Offset to 0%	12:28:13	Correct		
X & Z Data Same Sign	12:28:31	LSM 10 to LSM 08		
to	12:28:40	1 cycle Error		
X Position to 0°	12:28:36			
Y Motor OFF	12:28:39			
X, Y & Z Data Saturated	12:29:38	LSM 09 to LSM 09		
to	12:30:08	3 cycles		
SIDE ON	12:30:04	Experiment ON		
End of Flip Cal Sequence	12:30:46			
Science Mode Confirmed	12:30:48	Correct		
Chan. 6 to 042 & Chan. 7 to 010	12:30:49			All Experiments ON
Filter Bypass Command	12:30:54	Filter Out		Filter Out
Flip Cal Initiate Command	12:30:59			8 Bit Science Data
Y Position to False	12:31:01	Error		Tolerance

Event or Command	Time	Response	Test Condition
Chan. 6 to 38, Chan. 7 to 11	12:31:04		
X & Z Data Have Same Sign	12:31:06	One cycle, LSM 9 to	
to	12:31:16	LSM 9. Data approx. -103	
Z Offset to +50%	12:31:18	Error	
Single Negative Z Read Out	12:31:17	In LSM 10	Error
X Motor ON	12:33:30		
Science Mode Confirmed	12:33:33	Error	
X Flipped	12:33:36		
Z to 0% Offset & Cal Mode	12:34:11	Correct	
X Motor OFF	12:34:07		
X Position to 0°	12:34:33	SIDE ON (rippled off during flip)	
SIDE ON Command	12:34:40		
X, Y, & Z Data Saturated	12:35:26	3 cycles, LSM 9	
to	12:35:56	to LSM 9	
Science Mode Confirmed	12:36:36	Correct	
Chan. 6 to 42, Chan. 7 to 10	12:36:37		
Y Position to 180°	12:36:39		
End of Flip Cal Sequence	12:36:39		
		Science Data Tolerance Charged to Zero Bits	
LSM Sequence Skips Position 4	12:36:50	Error	
i.e., from LSM 3 to 5 with			
Science Data Dropout Starts	12:36:50	Error	
LSM Sequence Skips 6	12:36:51	Error	
i.e., from LSM 8 to 10	12:36:52	Error	
End of Data Drop Out	12:36:52		
LSM Sequence Jumps to	12:36:53	Error	
Reset LSM 01 and Stops			All Experiments ON
Flip Cal Initiate Command	12:36:53	Not Confirmed,	Filter Out
		as LSM Sequence is	
		Stopped on LSM 01	
X Motor ON	12:39:25		Zero Science Data
X & Sensor Flip	12:39:30		Tolerance
X Motor OFF	12:39:53		
Y Motor ON	12:39:57		
Y Motor OFF	12:40:23		
LSM Sequence Stopped ON			
LSM ON Unitl	12:40:23		
Science Data Dropout	12:40:24	Error	
LSM Sequence Jumps to			
LSM 14 and Restarts	12:40:24		
LSM & STS Resync Correctly	12:40:26		
on Next LSM 01			
Z Position False	12:40:28	Error	
Chan. 6 to 39, Chan. 7 to 10	12:40:30		

Event of Command	Time	Response	Test Condition
Cal Mode Confirmed	12:40:33	Correct	
SWS ON Command	12:40:38	SWS ON (rippled off during flip)	
SIDE ON Command	12:40:41	SIDE ON (rippled off during flip)	
End of Flip Cal Sequence	12:42:56		
Science Mode Confirmed	12:42:59	Correct	
Chan. 6 to 42, Chan. 7 to 10	12:43:00		
Y Position to 180^{o}	12:53:02		

Program mode changed to PRINT ALL LSM data for one full LSM sequence plus.

4.0 STATUS AND SCHEDULE

At the end of the report period the EM tests are proceeding according to the schedule contained in the December Monthly Report, ATM-604. Array B testing is scheduled to start in mid March. The best estimates for the availability of EM experiments for test are:

ASE - 13 March

SIDE/CCGE - 15 March

Heat Flow - 8 April

The late delivery of the HFE may delay the commencement of full scale Category #3, Array "B" EM tests. Baring major problems on ASE and SIDE we would be prepared to start Category #2 tests on the HFE at least one week earlier than the above date.

APPENDIX A

ENGINEERING MODEL SYSTEMS INTEGRATION TESTS - BRIEF LOG

Date	
2/1	Active Seismic Experiment Category #2 tests. ASE turn-on problems encountered.
2/2	Active Seismic Experiment Category #2 tests. Preparation of monthly report.
2/3	Command decoder intermittent and most of day spent in determination and correction of problem.
2/4	Central Station operated with STS #1. Data Subsystem Program for STS checked out. Apparent fault in PCU corrected itself.
2/6	Continued Central Station - STS #1 integration tests.
2/7	STS #1 - Central Station integration tests. ASE on in PM with circuit protection inhibited. ASE would not turn off.
2/8	System shut down to replace ASE standby fuse. System on and ASE turn on and turn off transients measured.
2/9	SIDE breadboard arrived. Lab rearranged and ASE removed from test configuration.
2/10	SIDE breadboard put on line and precategory #3 tests performed on SIDE.
2/13	Initiation of Category #3 tests with PSE, SWE, and SIDE breadboard. DSSTS removed and STS #1 Data Unit commissioned with EM.
2/14	LSM EM Category #2 tests. LSM has many functional discrepancies. Category #3 tests commenced with all Array "A" experiments. Full day's operation with RF downlink.
2/15	Return to LSM Category #2 tests. LSM ETS unstable. Apparently instability is crosstalk within ETS. LSM power line noise is low. Apparent failure of FET in analog multiplexer. Brassboard multiplexer substituted for EM.

Date

2/16 Continued LSM ETS instability problem. Continued Category #3 tests neglecting glitches on LSM. PSE had unexplained high current consumption on 3 or 4 occassions. Transmitter serial #002 believed to be responsible for large (5w) momentary increases in Central Station power consumption. LSM appeared to hang up and LSM word #5 lost, cleaned by turning experiment off and on again. Command response of all experiments measured. LSM apparently executed commands without being commanded. No command execution indication on LSM SBOB.

2/17 Further efforts unsuccessful to correct LSM ETS instability problem. LSM appeared to hang up again. Corrected by turn off and on. Brass-board analog multiplexer failed. Returned to DSS for repair. No multiplexer on line.

2/20 Continued efforts on LSM ETS. Philco man into repair ETS.

2/21 Circuit breaker levels checked and LSM level reset. Category #3 tests continued. LSM ETS fault corrected. Glitches in LSM science data and power profiles noted. Many LSM functional discrepancies. STS operated with LSM checkout program. System checks indicated faults were in experiment and not Central Station.

2/22 LSM STS program modification initiated to read if change has occurred since last relevant value. Attempted to run SIDE STS program was unsuccessful. Noted a variation of transmitter serial #002 input current by up to 10 watts. Successful test of backup timer operations. Continued glitching on LSM data on ETS display, downlink data steady. LSM ETS printer disabled. Continued documentation of Category #3 tests.

2/23 Transmitter serial #002 drew excessive power for 3 minutes at turn on. Momentary fault in PCU caused voltages to rise above normal levels. Fault cleared by repeated switch overs from PCU #1 to PCU #2. PSE program for STS checked out. Problems encountered in driving the special PSE software believed to be correct. Start of Category #4 testing. Modified LSM software programs successfully ran.

2/24 Continued Category #4 tests. Analysis of LSM printouts and additional Category #4 LSM tests. Transmitter serial 002 drew excessive power and then failed. Returned to subcontractor for repair.

Date

2/25 GSE group performed a checkout of STS and refined their checkout procedure.

2/27 Category #4 tests with LSM software. Documented Category #3 interface signal with oscillograph photographs. CPLEE retuned to lab.

2/28 Checkout of LSM software and made mag. tape recording of about four hours of the Central Station wave train with all experiments on line for later analysis with STS software. LSM taken off line and returned to P. I. Detailed correlation of LSM errors. CPLEE pumped down and maintained vacuum.

3/1 PSE strip chart recorded checked-out. SIDE STS software ran successfully. CPLEE integrated with Central Station.

3/2 SIDE ran with STS software. A couple of simple modifications required to SIDE software. Attempted run of SWE software.