Bendix

Aerospace Systems Division

TRANSMITTER DESIGN ANALYSIS

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This ATM presents the results of analytical and experimental efforts, performed during the months of May and June 1970, to evaluate the performance of the ALSEP Data Transmitter, to incorporate design improvements and to document a description of critical circuit operation.

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TRANSMITTER DESIGN ANALYSIS

GLOSSARY OF ALL SYMBOLS USED

r_x	Input series resistance in hybrid π model
q_x	Input series conductance in hybrid π model
β	Small signal current gain of transistor in common emitter configuration.
g_m	Incremental transconductance of a junction transistor.
ω_T, f_T	Frequency where $\beta = 0$ (Extrapolated value).
g_π	Conductance in the hybrid π model
C_π	Capacitance in hybrid π model
s	Complex frequency variable.
h_{11}, h_{ie}	Short-circuit input impedance.
h_{12}, h_r	Open-circuit reverse voltage transfer ratio.
h_{21}, h_f	Short circuit forward current transfer ratio.
h_{22}, h_o	Open circuit output admittance.
h_{22r}	Real part of h_{22}
y_{11}	Short circuit input admittance.
y_{12}	Short-circuit reverse transfer admittance.
y_{21}	Short-circuit forward transfer admittance.
y_{22}	Short-circuit output admittance.
Z_s	Source impedance
R_s	Equivalent series resistance
R_P	Equivalent parallel resistance

GLOSSARY OF ALL SYMBOLS USED (CONT.)

C_{out}	Parallel output capacitance
X_s	Equivalent series reactance
$P_{o(o)}$	Power output at peak of Linvill graph
$P_{i(o)}$	Power input at $P_{o(o)}$
P_o	Power output
P_i	Power input
P_G	Power gain
G_r	Gradient of input-power plane in Linvill graph
V_{CC}	Collector supply voltage
β_o	Low frequency current gain of common emitter transistor

1. INTRODUCTION AND SUMMARY

Several problems were encountered during the build-up of the first flight type Bendix Data transmitters for the ALSEP system. These problems can be characterized principally as difficulties in tuning which resulted in significant delays in meeting schedules. A review of the design was made to determine the causes of the problems and to effect their solutions.

As a result of the review three circuit changes were made in the power amplifier sub-assembly. These changes were checked out on engineering model transmitters and then incorporated into the qualification and flight units. The general result has been very satisfactory and the tuning time during in-process testing has been significantly reduced. The review activity has continued so that a detailed analytical description of all of the critical circuits would be documented.

This report contains the results of the analytical effort. Section 2 is a general description of the transmitter and of the changes that were made in the power amplifier. Section 3 describes the characteristics of the problems and the approaches which were used in the review activities. Section 4 describes the three changes to the power amplifier in some detail. The last two sections present the circuit analyses, with Section 5 having the transistor circuit analyses and Section 6 devoted to the passive interstage networks. Section 7, the appendix, contains a sample power gain calculation and several calculations which were performed after the other calculations.

2. TRANSMITTER DESCRIPTION

2.1 GENERAL

The ALSEP Data Transmitter provides an output of one watt at a fixed frequency in the range of 2275 to 2280 megahertz (MHz). The output is split phase modulated as a result of the modulation input from the Data Processor at a rate which can vary from 265 Hz to 10.6 KHz. The output power is derived from a crystal oscillator operating at about 38 MHz. The oscillator output is multiplied, amplified and phase modulated in the primary transmitter circuitry. Figure 1 shows a block diagram of the functional parts of the transmitter.

Two complete circuit diagrams for the transmitter are also shown in this section. Figure 2 shows the circuitry prior to the changes which are discussed in this ATM, and Figure 3 shows the circuitry after the revisions were incorporated. These revisions consisted of three circuit changes accomplished in two drawing revision steps.

In the first change, which brought the circuit diagram from an E to an F, revision ferrite beads were added in the input circuits of three transistors in the power amplifier, and the power amplifier Q4 output stage parts were rearranged. In the second change (G revision) to the power amplifier, the interstage network between Q2 and Q3 was changed. Detailed descriptions of these changes are in Section 4.

2.2 DESCRIPTION

With reference to Figure 1, there are six main sub-assemblies in the transmitter, designated A1 through A6. The main interest in this report is in the power amplifier although the analyses of the pre-amplifier circuits are also included. Three sub-assemblies, A3, A4 and 5, which are printed circuit modules, are often referred to collectively as the exciter.

The crystal oscillator within the exciter module has its crystal frequency chosen to be one-sixtieth of the selected output frequency in the band 2275 to 2280 MHz. The oscillator output is amplified and drives a step recovery diode, CR3, to produce harmonics. The following tuned circuit is resonant at the fifth harmonic (190 MHz) and feeds a cascode amplifier which provides a signal level of 3.5 dBm into the modulator.

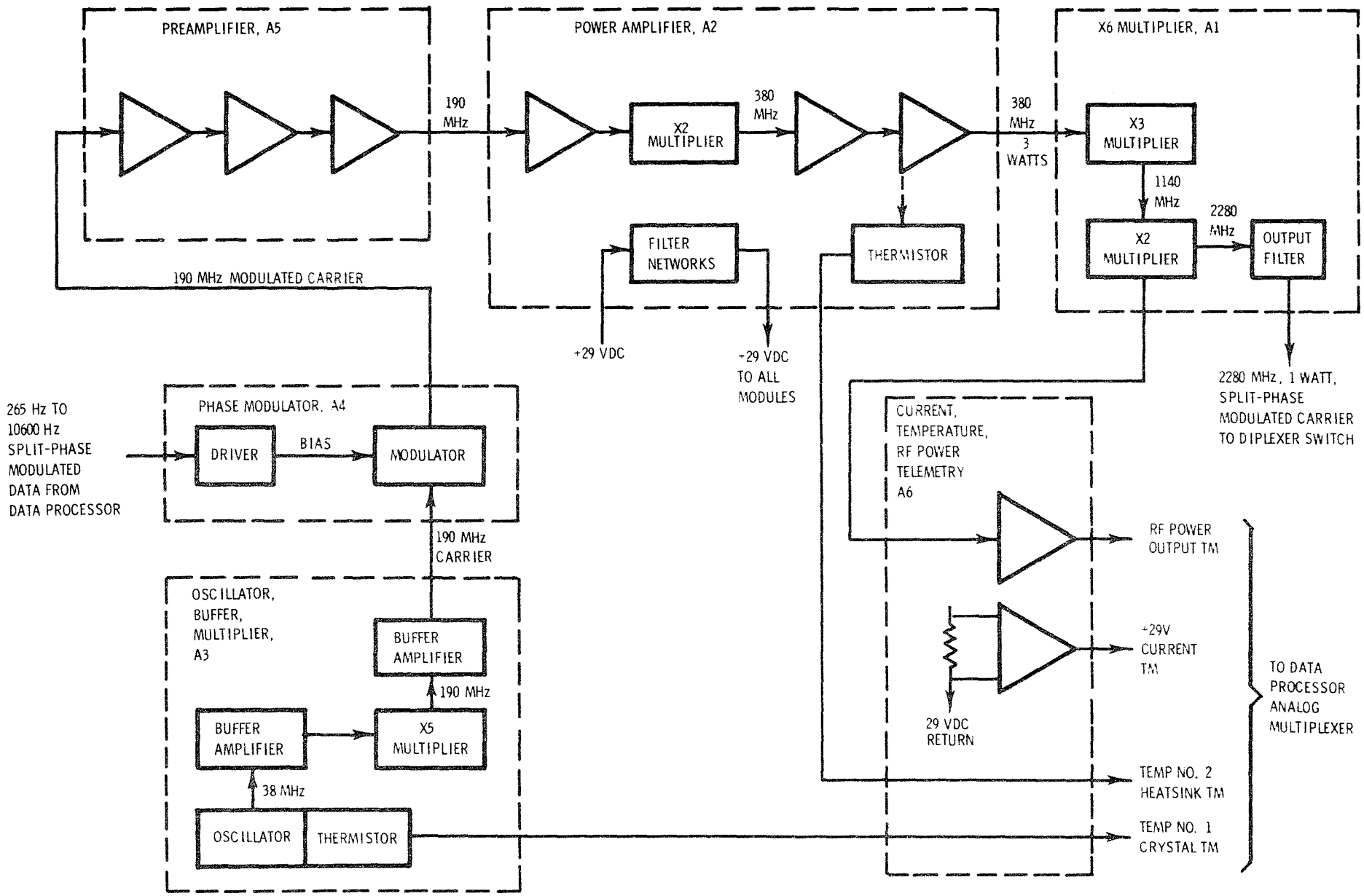


FIGURE 1. Transmitter Functional Block Diagram

The phase modulator consists of a series resistor and capacitance, with the capacitance being provided by two parallel varactor diodes. A driver circuit varies the reverse bias across the varactors to change the capacitance, and hence the phase of the carrier frequency. The input to the driver circuit is binary in nature and has a frequency of 265 Hz to 10.6 KHz.

The phase modulated carrier is then amplified in the pre-amplifier module, which is a three stage limiting amplifier. The input to the module is -7.5 dBm, and the output is saturated at 15 dBm.

This signal is fed into the power amplifier through a resistive-T attenuator network. The values of the components in this attenuator are selected to present the correct drive level to the power amplifier. This procedure allows for component variation within the preceding stages, and helps to keep the final output constant with varying temperature.

The power amplifier module uses four transistors to raise the power level to 35.2 dBm, and double the frequency to 380 MHz. The first stage works in Class A and feeds a Class C, common-base doubler circuit, followed by two Class C power amplifying stages. This module also contains the filtering networks for the 29 volt supply to the rest of the transmitter.

The 380 MHz output is fed into the X6 multiplier module, where a tuned cavity acts as a matching network into the first varactor. The cavity following the varactor is tuned to the third harmonic at 1140 MHz, and provides a matching network into the second varactor. This acts as a X2 multiplier, and produces an output at 2280 MHz, which is fed into two tuned cavities that match the signal into 50 ohms and filter out spurious harmonics.

The final module is the telemetry board, which delivers analog outputs corresponding to the RF power output, the supply current, and the temperatures of the oscillator crystal and the heatsink of Q4 in the power amplifier. The RF power is measured by sensing the voltage drop across a resistor in the bias network for the final varactor in the X6 multiplier. The supply current is determined by measuring the voltage drop across a 1 ohm resistor in the 29 VDC return. The two temperatures are measured using a simple voltage divider, with a thermistor in one of the branches.

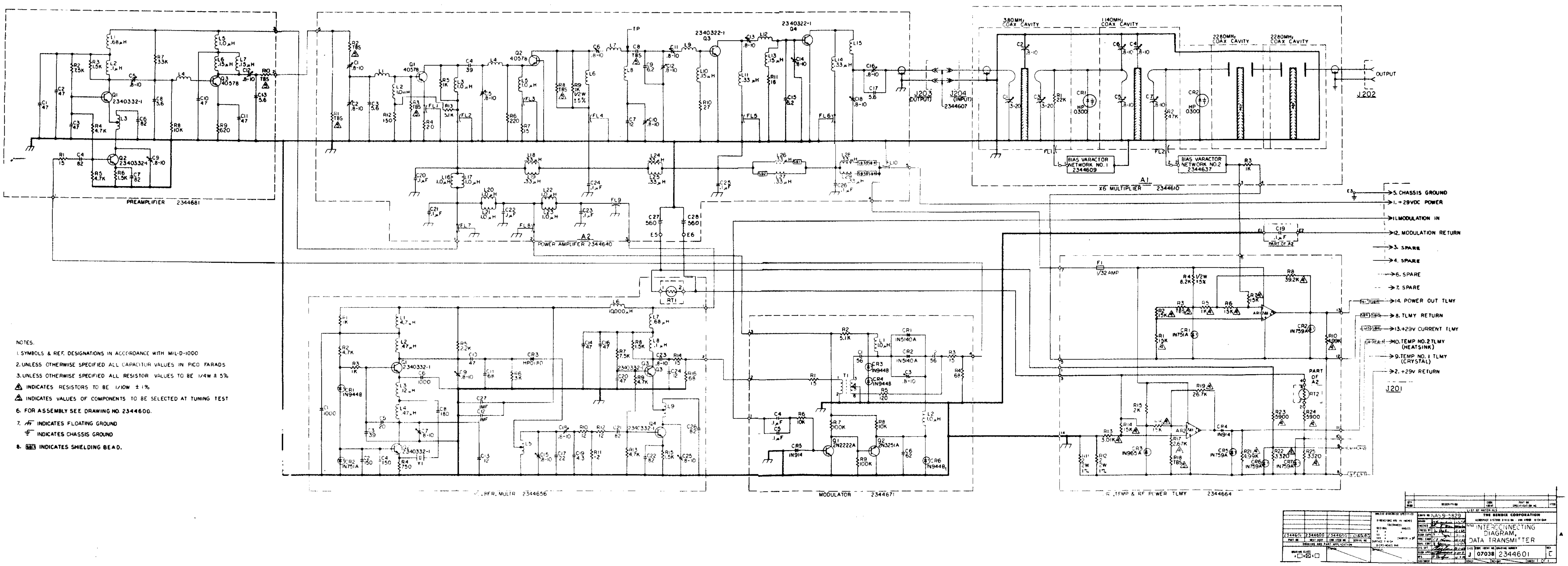


FIGURE 2. Circuit Diagram - "E" Revision

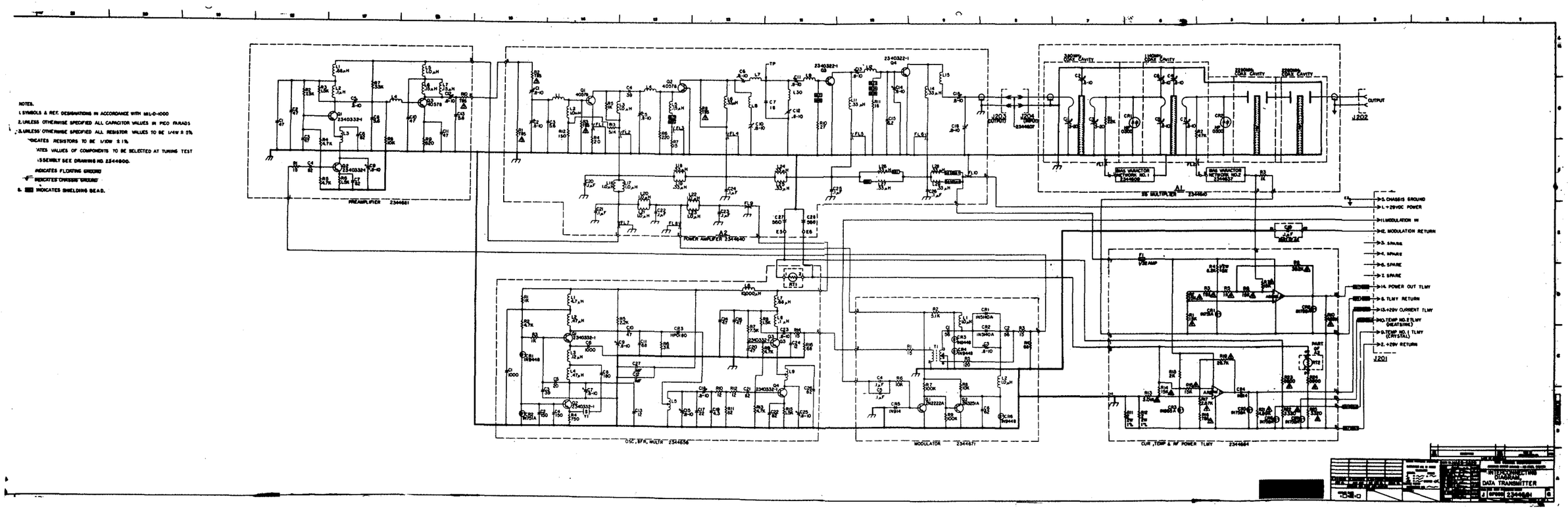


FIGURE 3. Circuit Diagram - "G" Revision

The physical construction is such that the power amplifier is built on an aluminum chassis, milled to provide five separate, screened compartments. The X6 multiplier is manufactured in a similar fashion and is fastened to the top surface of the power amplifier. The remaining modules are constructed on separate printed circuit boards, and all fit into screened compartments milled out of the power amplifer chassis. DC isolation from the station thermal plate is provided by a beryllium oxide plate, which fits between the power amplifier and the transmitter baseplate. The beryllium oxide provides a good thermal path for transmitter heat removal.

3. PROBLEMS AND APPROACHES

3.1 BACKGROUND

The developmental hardware for this transmitter design consisted of breadboard circuits and two engineering units which were very similar to the flight configuration. Significant time was spent in developing and tuning the engineering units and a certain amount of this design effort was empirical because of the difficulties of exact design at the frequencies involved. At these frequencies, hundreds of megahertz, small pieces of wire become primarily inductances and the location of parts affect the circuit capacitance. Another significant influence was the lack of transistor characteristics at the frequencies and signal levels being used. Some empirical design is therefore necessary in working with circuits operating at these frequences. The flight design was then based directly on the evolved engineering unit.

The first flight release was for five units, the first two designated for flight on the A-2 ALSEP, the third became the qualification unit and two were designated as spares. For reference purposes the serial numbers for these units are 21, 24, 23, 22 and 25 respectively.

Serial numbers 21 and 24 were built and tuned without great difficulty but S/N 23 was very difficult to tune. The difficulty was characterized by inability to control supply current, output power and frequency spectrum within specification requirements over a temperature range of $-30^{\circ}C$ to $+70^{\circ}C$. As the circuit diagrams indicate, there are ten variable capacitors in the power amplifier and seven in the X6 multiplier which provide a large number of interdependent tuning conditions. It was not obvious at this point in time whether the basic problem was a component deficiency or whether the proper tuning condition had not been reached.

At about the same time problems were being experienced in obtaining proper gold plating over the housings which were machined of magnesium, although the same vendor had provided good work for a number of years. As a result of the plating problems a decision was made to switch to an aluminum base metal, so that the plating quality would not be as critical as with magnesium. Plating quality was also corrected with a change in vendors.

Work was stopped on the S/N 22 and 25 transmitters and a new release was made for S/N 26 and 27 transmitters with aluminum housings. As these new units were being checked, during in-process testing, it became clear that the performance would be similar to S/N 23.

As a result of these tuning problems, several efforts were initiated:

1. An analysis of the critical circuits was begun,

2. Engineering hardware was modified to evaluate proposed changes,

3. The application group at RCA was contacted for suggestions,

4. A consultant from the Bendix Research Laboratories was assigned to help in the evaluation effort and

5. Transmitter tuning techniques were evaluated.

The general conclusion was reached that the power amplifier was marginally stable and that for some tuning and temperature conditions the amplifier stages would begin to oscillate. The oscillation energy mixed with the signal being amplified and the resultant spectrum caused the characteristic spectrum "break-up." In addition it was determined that there were difficulties in matching the impedance between Q2 and Q3 and between Q4 and the X6 multiplier. The tuning ranges were very limited and contributed to the difficulties in matching these networks.

Circuit changes were made to engineering units. These changes were then evaluated and improved upon. Analysis closely supported the re-design effort. After improved performance was verified on the engineering units, the changes were made to S/N 23 and then to S/N 26 and S/N 27 transmitters.

3.2 ANALYSIS

Due to the marginal stability and "out-of-spec." performance of S/N 23, followed by similar performance in S/N 26 and S/N 27, an analysis of the most critical circuits was begun. This analysis was conducted by evaluating each interstage network for range of impedance matching, using transistor data available. Each transistor was also considered separately for power gain and stability using Linvill techniques. The detailed results are presented in sections 5, 6 and 7.

Some difficulties were experienced in obtaining suitable transistor characteristics because the working frequencies of 190 and 380 MHz are close to the f_T of the transistors used (500 MHz for the 2N3375 type). The usual approximations and interpolations from manufacturers data are not valid close to the f_T frequency. In addition there are significant differences between small signal and large signal parameters. Small signal data has been available but large signal data has not been available for these high frequency transistor types.

3.3 CONSULTATION WITH RCA

One of the steps taken to solve the problems with the power amplifier was a consultation with the RCA Company, the vendor of the power transistors. Two Bendix engineers traveled to the RCA Electronic Components Division in New Jersey to discuss circuits and the proposed changes with the High Frequency Applications Group. RCA engineers agreed that proposed changes improved the circuits and suggested several other changes.

A previous RCA suggestion was that ferrite beads be substituted for some of the RF chokes in the power transistor bias circuits. This was recommended because the chokes used have self-resonant frequencies near the 380 MHz of the Power Amplifier power stages. The number of beads for each case is determined experimentally so that the stage is stable but losses are not excessive. These changes are discussed in more detail in Section 4.

Other circuit changes around Q4 of the Power Amplifier were also suggested, but were not evaluated since they required significant design changes in the chassis. It was suggested that Q3 was being run at too low a power level, and that a resistor-diode network might be required to ensure turn-on. This recommendation was not acted upon since no problems had been encountered with this transistor. A special RCA part was recommended for the grounding of Q3 and Q4 emitters. This part is more reliable and has lower inductance than the present method of shorting with a wire loop but circuit performance would be changed.

3.4 TUNING TECHNIQUES

In various following sections, analysis will be presented for interstage coupling networks, usually from the viewpoint of being capable of providing a conjugate match for maximum power transfer. In reality, a carefully tuned power amplifier will exhibit sufficient overall gain to provide excessive 380 MHz power output and a corresponding excessive current drain from the power supply. Levels close to +38 dBm output have been observed. There are several selectable resistors such as R1 and R2 in the input circuit, and R3 and R8 in the first two amplifier circuits which can be used to lower power output and overall current drain. In practice, it has proven more advantageous to use deliberate mis-match between one or more stages to control the power output level.

Excessive gain is traded for increased power amplifier bandwidth in this procedure. This feature has proved to be of importance in stabilizing output power against temperature variation. Although some variations in overall power gain are unavoidable, such as those due to changes in transistor current gain β with temperature, changes in input and output impedance typically produce less of an effect upon power for broadband tuning. Single frequency, non-swept tuning can produce rather narrowband, asymmetric, or hysteresis-prone behavior. Any thermally induced shift in center frequency could result in unacceptable power variation under these conditions. It also remains possible to so (mis-) tune an amplifier so that "breakup" will occur at frequencies not far removed from the desired output, a factor which can lead to breakup under variations in temperature.

The last two output stages of the power amplifier have traditionally been tuned using a swept Telonic generator. Sweep testing of the overall power amplifier evolved during May. At present, the sweep is manually performed by rocking the frequency knob of the HP608 VHF generator used as a 190 MHz source. At room temperature a properly tuned power amplifier will be essentially free of breakup or hysteresis for any input frequency. Response is typically somewhat asymmetric, with a 3 dB bandwidth at 380 MHz MHz of at least 4 MHz.

Part of the asymmetry present in a properly tuned design is a fairly rapid drop off in power with frequency on the low frequency side of the passband. Such response is not unusual for self-biased Class C operation such as that present in Q3 and Q4 of the power amplifier. This region is where hysteresis will appear for somewhat different tuning conditions, representing the transition between "on" and "off" in at least one of the self-biased stages. Although this effect may be minimized at room temperature the start of the region of rapid dropoff is normally kept at least 1 MHz below the desired 380 MHz center frequency, to be assured of cold turn-on. Hysteresis and hence turn-on is more of a problem at cold temperatures, due to in part to the reduced current gain of the transistors.

Although the power amplifier tuning procedure is empirical, it can now readily be accomplished, and performance verified over temperature, within the period of a day or two. Sweep testing is also employed when the amplifier is mated with the X6 multiplier, which has an inherent input bandwidth moderately broader than that of the amplifier. There is some equivalent bandwidth narrowing due to the addition of the X6 multiplier, but the greatest effect is the introduction of a sharper skirt response outside the passband of the design. The 3 dB bandwidth of the output of the X6 multiplier at 2280 MHz is typically in the order of 18 MHz.

4. POWER AMPLIFIER DESIGN CHANGES

4.1 RF CHOKES

An experimental investigation of the "breakup" problem was made by probing a flight model power amplifier, stage by stage, with the aid of a semi-rigid coaxitube probe described in more detail in the next section. The probe was inserted into the chassis holes through which the series Johanson interstage capacitors are tuned. Very light capacitive pickup was used so as not to disturb circuit performance. A spectrum analyzer was used to view the signals. Breakup could be caused by deliberately detuning the input signal, one of the earliest overall swept tests performed, or by reducing the operating temperature. In either case, the undesired signals appeared in the vicinity of the 380 MHz signal, the 190 MHz circuitry remaining stable. Breakup due to cooling was traced to later stages in the 380 MHz circuitry.

Some instances of breakup due to off-frequency operation are believed to be caused by frequency sensitivity in the action of the series resonant trap used to short out the 190 MHz signal in the output interstage of the multiplier. This was remedied by moving the shunt trap directly to the collector of Q2, from its previous location after the first series branch of the output matching network. (Serious mistuning of the trap can still cause some breakup despite its new location).

It was suggested by RCA applications engineers that oscillations in the amplifiers might be due to spurious resonances with the Nytronics RF chokes used in the circuitry. RCA favors the use of high impedance, low Q, ferrite loaded chokes. The manufacturer of the Nytronic chokes list resonance frequencies which were above the operating frequencies of interest, except for L5 which had a resonant frequency of 240 MHz. Since this is in the input of the multiplier it was operating above resonance to the extent that 380 MHz signal appears at the emitter. Since the resonance involved is a parallel resonance, an effective open circuit in the biasing lead, nothing deleterious is particularly expected to happen at or near resonance. It is an incidental resonance with some of the impedances present in the interstages which would be expected to cause trouble. Such resonances can be destroyed by reducing the "Q" of the RF choke.

Ferroxcube 3B ferrite beads, used to decouple the D. C. power circuitry, were available for this purpose. The value of L5 was reduced to .15μH and two such Ferroxcube 3B beads were mounted on the leads. In addition, the base return choke L10 of Q3 was replaced by a wire with two beads, and the base return choke L13 of Q4 was replaced by three beads. Measurements of the beads on a Hewlett Packard network analyzer indicate that slipping one bead onto a wire at 380 MHz increases the apparent series resistance in the line by 30 ohms, without modifying the basic inductance contributed by the wire itself. Thus, L5 has about 60 ohms resistance in series with its .15μH basic inductance. The two bead replacement for L10 has 60 ohms resistance and roughly similar inductive component due to the lengths of wire present in the circuit. The replacement for L13 presents similarly a reactance of about 90 + j90 ohms.

The above modifications essentially eliminated the breakup problem. It might be argued that the reasonably low real impedance presented by the beads may have squelched some other spurious resonance within the interstage which was not related to the original RF choke. In any event, the solution has remained valid in all five units modified to date. The addition of the beads did cause a noticable loss in RF power, but one that was easily overcome. The resistive loading presented is not unlike the selectable resistors in the 190 MHz circuitry used to adjust drive power.

4.2 Q2 - Q3 INTERSTAGE

The 190 MHz input supplied to the power amplifier is doubled to 380 MHz within Q2, an RCA 2N3866 overlay transistor. Doubling is provided principally by varactor multiplication within the voltage variable collector-to-base capacitance of the transistor. In an ordinary Class-C doubler, collector current flow is suppressed at the fundamental, while in the present common-base multiplier, the collector is deliberately shunted with a series resonant trap at 190 MHz to aid pumping of the collector-to-base capacity. The second harmonic so produced is routed to the input of Q3. The real impedance loading presented by Q3 to the doubler output at 380 MHz is transferred by the varactor multiplier to a real collector load at 190 MHz. The transistor thus provides power gain at 190 MHz much as in a normal common-base amplifier. The gain of the amplifier at 190 MHz minus the loss of the multiplication process still leaves a net overall stage gain of about 6 dB.

A description of the theoretical performance of this type of amplifier/multiplier may be found in the article "Generation of Microwave Power by Parametric Frequency Multiplication in a Single Transistor", by M. Caulton, H. Sobol, and R. L. Ernst, RCA Review, June, 1965, pp. 286-311. The treatment given is of the small signal variety, Class-C amplification requiring experimental input and output matching procedures as discussed more recently in "RCA Silicon Power Circuits Manual", published by RCA Electronic Components Division, Harrison, New Jersey, 1969.

Q2 output impedance determinations were made using engineering unit #3. A set of covers was constructed which permitted the output of Q2 to be routed through an OSM connector to a power meter. The output matching circuit included the L8/C10 190 MHz trap, the series L7/C6 branch, and an external shunt C across the output connector. The chassis was driven with the normal +13 dBm input to Q1, and was tuned to provide maximum power transfer into the 50Ω power meter load, with a measured output of +24.5 dBm at 380 MHz. The covers were arranged such that the lead from the collector of Q2 could be unsoldered from the output matching network and be replaced by an OSM connector whose center pin had essentially the same length as the transistor lead. Since maximum power transfer had been arranged, the impedance seen looking from the transistor into the network terminated with 50 ohms will be the complex conjugate of the output impedance of the transistor. A Hewlett Packard 8410A network analyzer with a .1 to 2 GHz reflection test box was used for measuring the network through the substituted connector. At 380 MHz, the output impedance of the multiplier was determined to be $Z = 12 + j\,60$. The impedance measured at 190 MHz had an unmeasurably low real part, and an imaginary part of + j18 ohms, which is low enough to cause appreciable current to flow at 190 MHz in the transistor.

Earlier circuitry used in the transmitter had the trap separated from the transistor by the series L7/C6 network. This location caused an interdependence between trap adjustment and impedance transformation, and resulted in breakup if the input frequency was detuned. The present trap, connected from the collector to the ground, utilized a higher impedance coil L8, whose inductance is in the order of 100 nH. The capacitor C10 is adjusted at 190 MHz to produce series resonance. There is approximately 1/2" of lead between the collector terminal and the trap, which contributes to the majority of the j18 ohms measured at 190 MHz at the collector output. The impedance of the shunt trap at 380 MHz is about j200 ohms,

which is quite high in comparison to the Q2 output or Q3 input impedance levels. The trap has accordingly a small effect on impedance transformations at 380 MHz.

In effect, the principal 380 MHz interstage matching network consists of the series arm L7/C6, a shunt branch consisting of an 18 pF capacitor C7 shunted by a series tank L30/C12, and the final series arm L9/C11 leading to the base of Q3. Although the shunt branch is shown grounded on the "G revision" diagram, the Johanson variable C12 is mounted on a plastic insulator, the "ground" leads of the capacitor and the C18 glass encapsulated capacitor running over to the emitter pin of Q3. The latter pin is then grounded with a wire running down the side of the Q3 TO-60 transistor can. Earlier development work indicated that the above grounding scheme produced a higher net gain than any other. Recent measurements have indicated that there exists sufficient series inductance in the grounding lead to permit a noticable voltage drop between the emitter and true ground.

The latter potential gives rise to degeneration which makes the measurement of Class-C input impedance of Q3 difficult by the conjugate impedance method, since both the base and the emitter impedances are attached to different points in the matching network. The physical location of the transistor at the bottom of the case also makes connection of a bridge difficult, even at the end of a coaxial cable. The effect of the series emitter inductance is such that a nominally tuned power amplifier will lose from 3 to 12 db in gain if the emitter pin is more securely grounded with an additional grounding path. Both input and output impedances of Q3 appear to be affected by this change. Careful retuning of input and output networks with a somewhat more secure ground present, restored all but about one dB of circuit gain in a recent test on an engineering unit.

It is believed that a form of Q3 "emitter tuning" is accomplished by the interstage network. The shunt branch, in particular, provides fairly heavy current into the emitter terminal. The lead inductance of the 18 pF glass capacitor, C7, is great enough so that at 380 MHz the capacitor is very close to series resonance. Although testing with individual components indicated that fairly low loss parallel resonances could be generated between the two almost series-resonant shunt branches, tests of the circuitry mounted in the amplifier indicate that adjustment of C12

produces a measured net shunt branch impedance which varies from about +j13 to about +j20 ohm inductive, with some loss. The exact behavior depends on correction for the inductance of a short lead running to the impedance analyzer connector. As adjusted for maximum power transfer the corrected value of net shunt impedance might be in the order of 1 + j8 ohms.

In view of the difficulties in measuring Q3 input impedance under operating conditions, a signal probing technique was devised to further investigate interstage tuning. A spectrum analyzer was used to view the output of a probe which was held in close proximity to the component whose potential level was being tested. The probe was constructed out of 50 ohm, .086" O. D. semi-rigid coaxitube whose Teflon insulation and center conductor extended about 1/8" past the outer shield. Fairly small circuit disturbance was created with this probe. In contrast, a Hewlett-Packard vector voltmeter with "high impedance" probes provides 2pF capacity to ground, which rather seriously detunes all but low impedance points within the circuit. Further tests may be run with the vector voltmeter probe capacity tuned out as part of the matching procedure.

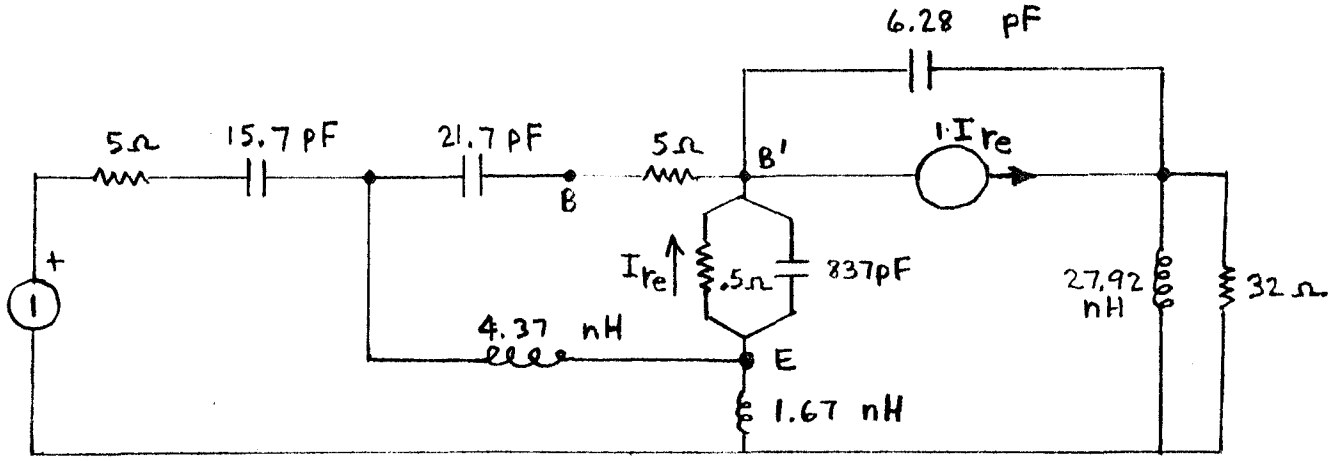
Use of the low capacity probe indicates that the shunt interstage point is indeed at a low impedance with respect to ground. With typical tuning, the voltage at the top of the shunt interstage is about 15dB below the output voltage at the Q2 collector. The level at the "grounded" emitter pin on Q3 is only a few dB lower than the potential at the top of the shunt tank. In contrast the voltage at the base of Q3 is only about 2 to 5 dB below the collector potential, much above the shunt branch potential. This implies that the series branch L9/C11 leading to the base exhibits an imaginary part which is substantially the conjugate of the base input impedance of the 2N3375 for Q3.

A simplified analysis was performed to demonstrate that routing signals into both the base and emitter terminals as outlined can supply power gain which is higher than achievable from a normal input stage. The calculations use a high frequency "T" model for Q3, based on an assumed 50 mA collector current and an f_α which is quite close to the operating frequency, 380 MHz. Under these conditions $C_{b'e}$ = 837 pF and r_e = 0.5 ohms. The "T" model was chosen for convenience, since the current-controlled current source present in the model may be directly analyzed by an ECAP computer program.

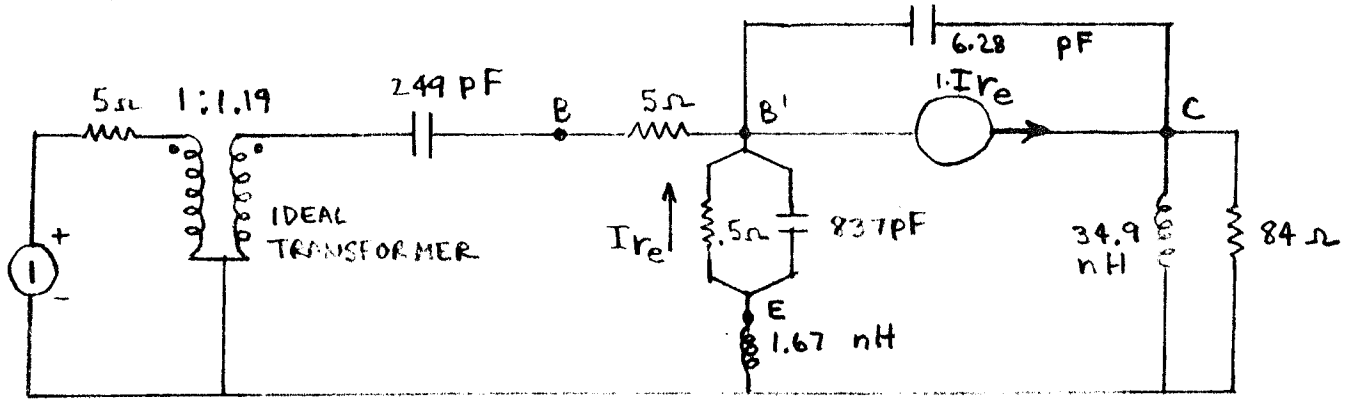
The low frequency current gain α_o is assumed to be equal to one, the controlling parameter for this source being the current flow through r_e. The remaining parameters of the model were chosen as $r_{bb'}$ = 5 ohms and $C_{b'e}$ = 6.28 pF. A 1.67 nH inductance is assumed to be present in the emitter lead, external to the transistor proper.

The above transistor model is inserted into a network whose parameters reasonably characterize the Q2 - Q3 interstage. The shunt branch was assumed to exhibit a loss free j10 ohms, based on the previously described measurements. The two series branches were evaluated by calculations based on the variable capacitor settings used for maximum power transfer, identical values of -j10 ohms being achieved for the net impedance of each branch. For convenience, the fairly small transformations due to line length, the shunt trap, and the input series branch have been lumped together, the output of Q2 being represented by a voltage source, and 5-j50 ohm series impedance at the point of attachment to the shunt interstage. The lower real impedance chosen here was influenced in part by later output impedance data obtained from additional tests of a 2N3866 multiplier.

Earlier analyses of more conventional amplifiers using similar transistor parameters exhibited parallel output resistances in the order of 50 to 70 ohms. A 62.5 ohm output load has been chosen for the present example. This is shunted by an inductance, used to tune out the imaginary part of the output impedance. The inductive reactance is chosen to be the conjugate of the collector-to-base feedback capacitor reactance, which provides first-order output tuning according to the earlier analyses. The analysis of the overall circuit as outlined provided voltage gain but no power gain, a not unexpected result in view of the approximate knowledge of the interstage values. As a result, an optimization procedure was instituted to "tune" the interstage and transistor loading to optimize power gain. The final values arrived at are shown below:



In this circuit, the output is almost exactly conjugately matched. The input match has not been fully maximized for reasons of computational economy, the residual mismatch being less than about .25 dB in power gain. As the circuit stands, the transistor power gain, based on the 5 ohm source, is 5.88 dB. The significance of this value can really only be demonstrated by providing a conventional amplifier analysis using the same assumed transistor parameters. The resulting optimized design is shown below:



Both the input and output circuits are very close to conjugate match, the overall tranducer gain from the 5 ohm source being 4.30 dB, which, because of the matched conditions, is also the power gain P_{in}/P_{out}. This is 1.58 dB below the gain achieved by the previous base/emitter feed circuitry. In effect, the gain loss which results from the 1.67 nH inductance in the emitter has been reduced by the current flow from the 4.37 nH "shunt" interstage branch.

Since Q3 actually operates as a class - C amplifier, the values assumed for the transistor model are only approximate. The effect of lead inductance within the transistor proper should be included.

The foregoing models are presented only to demonstrate that there is a basis for claiming that the equivalent to "emitter tuning" can be achieved with the interstage component topology as outlined, rather than being intended as accurate predictors of achievable gain, etc.

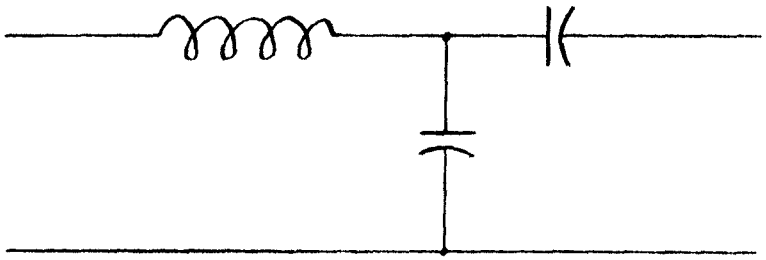
"Emitter-tuning" ordinarily uses an external capacitance in series with the emitter to tune out the effect of lead inductance. A recent communication between Bendix engineers and H. C. Lee of the RCA transistor applications group indicated that, alternately, a short lead capacitor connected between the base and emitter of a common emitter VHF

amplifier would improve efficiency and power output. The capacitance required is to be determined by trial and error. A comparison between this approach and the base emitter feeding technique would be interesting, since a several dB gain improvement can be achieved experimentally from either technique.

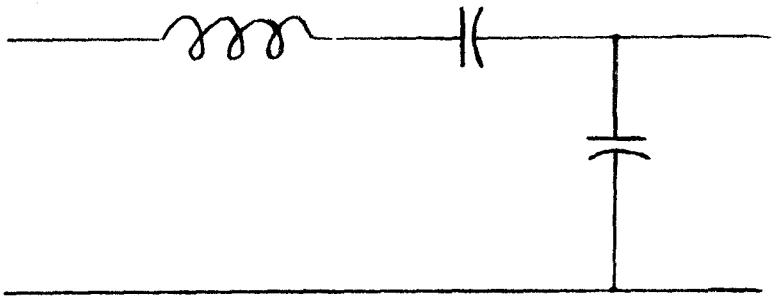
The original interstage network, and F "Revision" modifications, were laid out in such a manner that lead length had too large an effect on the tuning achieved. Series or shunt tuners would accordingly bottom out in this interstage without reaching optimum tuning. The use of the 18 pF capacitor mounted directly from the series interstage to the emitter "ground" has proved much more satisfactory. Despite some obvious small differences in length in the leads of this capacitor, all five separate units modified to date have tuned up without bottoming any tuners in this stage.

4.3 OUTPUT NETWORK

The network was changed from:



to a network of the following form:



The main advantages of this change were ease of tuning, a higher Q, and a greater ability to match into variations of the 50 ohm load. While the Q of the old circuit could have been raised, impracticable component values soon occurred. A higher Q resonant circuit enables the class-C output stage to produce an output with a less distorted waveform, and increase its efficiency. The ability to accommodate varying loads is shown on the two graphs, Figures 4 and 5. These show the variations required in the network component values to match into loads, from 40 to 60 ohms, at various Q's. The lower slope of the component values, as shown on the graph for the new circuit, indicate less of a mismatch for load variations. It can be seen that the new circuit is better in this respect.

Calculations show that for the output impedance of Q4 obtained from the data sheets of 28 - j67 ohms, and a load of 50 ohms, the new circuit has a Q of 4.7, compared to the Q of 1.6 of the old circuit. The impedance charts shown in section 6.2.4 on Q4 output show the range of output impedances that can be matched for both networks.

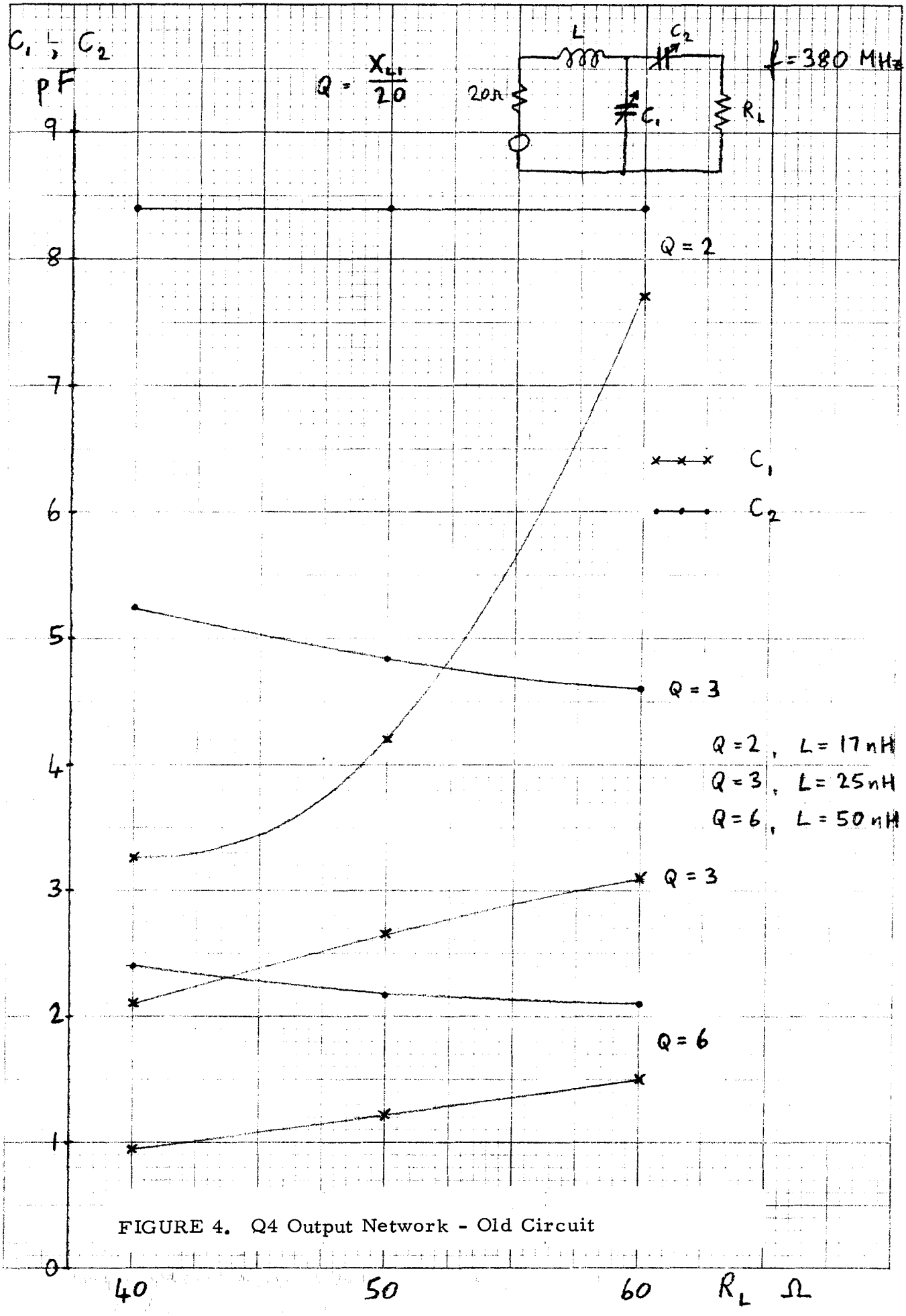


FIGURE 4. Q4 Output Network - Old Circuit

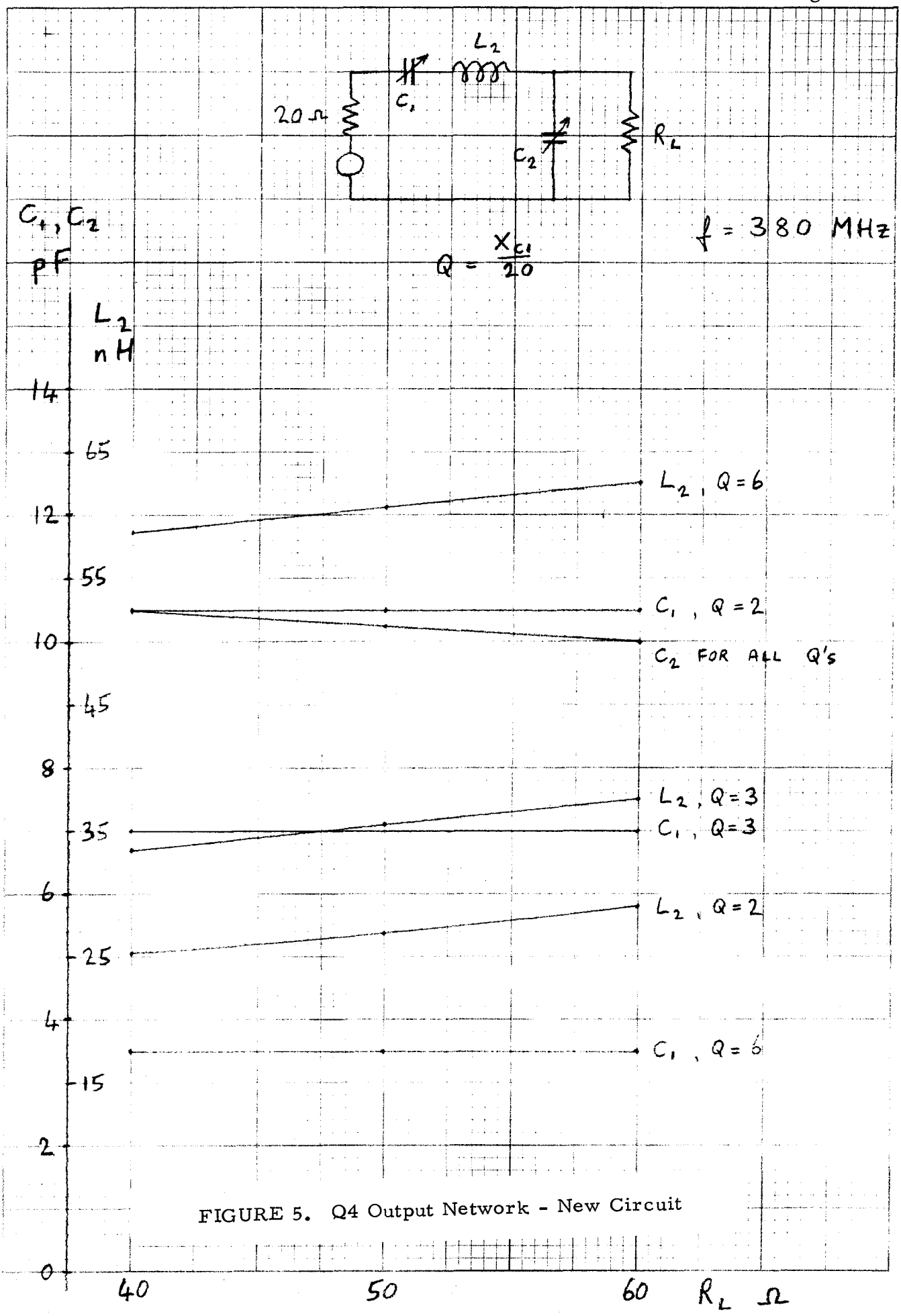


FIGURE 5. Q4 Output Network - New Circuit

5. TRANSISTOR CIRCUIT ANALYSIS

5.1 GENERAL

The following analysis is an attempt to establish the power gain and efficiency of the transmitter power amplifier stages. There is no over-all feedback so the amplifier is considered as a series of cascaded power stages, with matching elements between successive stages. Each stage is considered separately, and analyzed according to the Linvill Method, to establish how close the amplifier is to its optimum operation point, and how stable it is under expected operating conditions.

5.2 THE LINVILL METHOD

This method provides a graphical solution to power optimization, and provides a graphical three dimensional model to completely define the transistor under all load terminations, but only at the given frequency. The transistor, however, is part of a tuned circuit so only resonant frequencies need be considered[1].

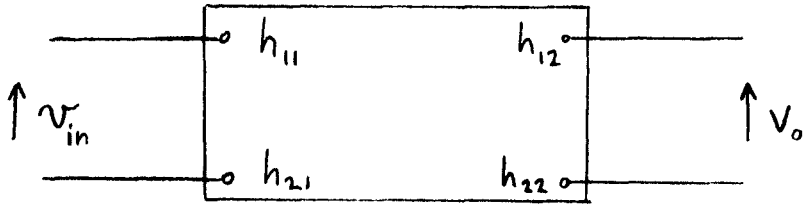
The solution is an admittance - impedance chart or Smith chart which represents all possible terminating impedances. If the transistor is potentially unstable, part of the chart will be defined as an unstable region and the rest as a stable region. The likely range of terminating impedance must be within the stable area if instability is not to occur. Estimates of power gain are readily made for every position on the chart.

To establish a particular chart all that are necessary are the "h" parameters for the device. These, however, need to be very carefully estimated if no facilities exist for direct measurement. Transistor data is required for each transistor stage in its particular configuration, where the configuration range through common emitter, common base, Class A, and Class C. Also data is required for small signal and large signal operation.

---

[1] Linvill, J. G. and J. F. Gibbons: Transistors and Active Circuits. McGraw-Hill Book Company, 1961, p. 241.

5.2.1 Estimation of 'h' parameters. (Small Signal)



The transistor 'h' parameters are defined by the following expressions:

$$E_1 = h_{11} I_1 + h_{12} E_2$$

$$I_2 = h_{21} I_1 + h_{22} E_2$$

$$\begin{bmatrix} E_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ E_2 \end{bmatrix}$$

h_{11} is readily obtained from the data sheets but h_{12}, h_{21}, and h_{22} are more difficult to obtain.

5.2.2 Calculation of h_{21}

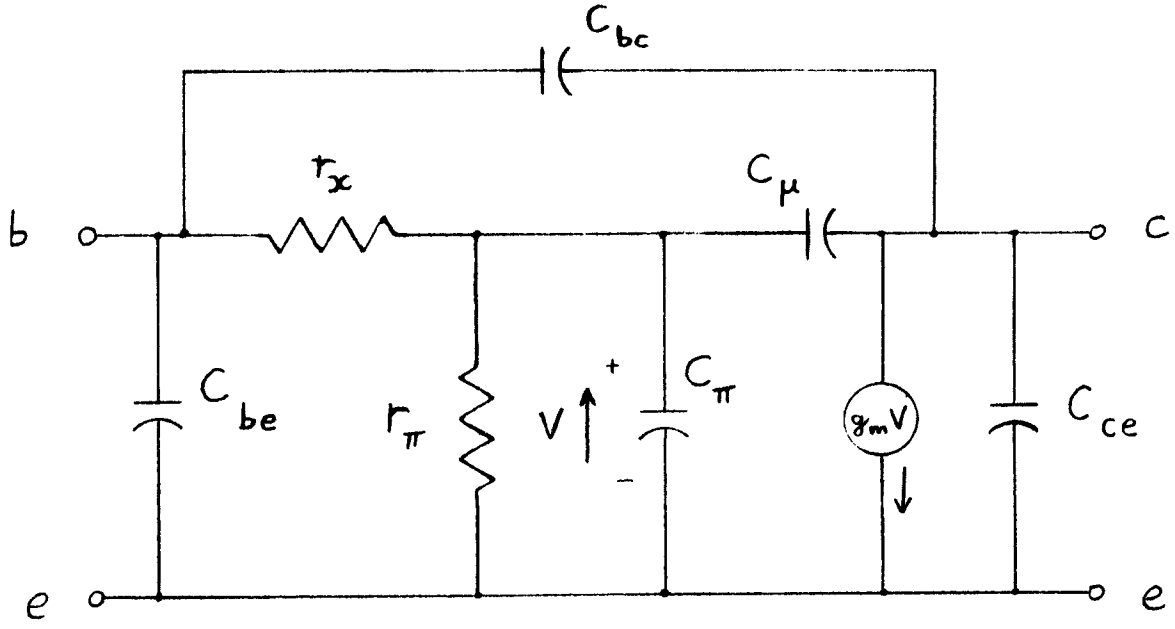
At the frequencies of interest h_{21} has as slope of - 6 db/octave. Therefore, since the 2N3866 has an f_T of 800 MHz, the gain at 400 MHz is 2, and the gain at 200 MHz is 4.

The phase of h_{21}[1] is 90° lagging at $f = f_T$. For frequencies lower than $f = f_T$ an estimation of phase for small signals was made according to the following:[2]

---

[1] Semiconductor Electronics Education Committee: Elementary Circuit Properties of Transistors, Volume 3, John Wiley & Sons, 1964, p. 262.

[2] Semiconductor Electronics Education Committee: loc. sit., p. 103-105.



$$h_{21} = h_{fe} = \beta = \frac{g_m}{g_\pi + s\,(C_\pi + C_\mu).} \qquad \text{(s = frequency of input signal)}$$

and

$$\omega_T = \frac{g_m}{C_\pi + C_\mu}.$$

$$h_{21} = \frac{\omega_T}{(g_\pi/g_m)\,\omega_T + s}$$

But $g_\pi/g_m = 1/\beta_o$ where β_o is the low frequency value of β,

therefore,

$$h_{21} = \frac{\omega_T}{\frac{\omega_T}{\beta_o} + s} \approx \frac{\omega_T}{s}$$

For a sine wave input $h_{21} \approx \frac{\omega_T}{j\omega} = -j\frac{\omega_T}{\omega}$ (1)

i.e., the phase angle is close to -90° for one octave either side of f_T.

Also, by definition ω_β occurs at $0.7\beta_o$ at which arg. $h_{21} = -45°$.

Therefore since $h_{21} << 0.7\beta_o$, it is reasonable to assume that for all transistors under consideration the phase of h_{21} is close to -90°.

However, as a limiting case, all Linvill charts are drawn for $< h_{21} = -45°$. It is interesting to note the effect of this change of phase, which is that the power gain is not very different from the case where $< h_{21} = -90°$, since the geometry of the transistor power model is not altered greatly.

5.2.3 Calculation of h_{12}

h_{12} is defined as the open-circuit reverse voltage transfer ratio, or voltage developed at the open circuited input terminals per unit voltage applied at the output terminals.

This amounts to $h_{12} = \frac{h_{11}}{h_{11} + Z_f} \approx \frac{h_{11}}{Z_f}$ (2)

Where Z_f = feedback impedance from output to input. The transistor model used to derive this is shown on page 30.

It can be seen that $h_{12} = h_{11} \left(\frac{C_\mu g_x}{(C_\pi + C_\mu)}\right) + j\omega C_{bc}$

Neglecting the first term in comparison to the second,

$$h_{12} = h_{11}\, j\omega\, C_{bc} = \frac{h_{11}}{Z_f}.$$

h_{12} becomes a very critical factor in the analysis since it is this term which represents the feedback within the transistor and causes:

a. The transistor to be potentially unstable,

b. The output load reflected at the input to the transistor, and

c. The driving source impedance to be reflected at the output of the transistor.

It becomes necessary to consider the stability of each transistor in each configuration carefully.

5.2.4 Calculation of h_{22}

h_{22} is defined as the open-circuit-output admittance, and differs from the parameter y_{22} given in the R.C.A. data sheets. "y_{22}" is defined as the short-circuit output admittance, and is measured with the input short circuited, whereas h_{22} is measured with input open-circuited.

The relationship connecting h_{22}, y_{22} is[1]

$$h_{22} = \frac{y_{11}\, y_{22} - y_{12}\, y_{21}}{y_{11}}$$

5.3 INTERPRETATION OF LARGE SIGNAL PARAMETERS

The Linvill Method of analysis is applicable to any two-port device operating in a linear fashion. Unfortunately not all the transistors in the transmitter are used in a class-A mode. It is possible to generate large signal parameters from large signal data if such data is available. Since no such data is available on the transistor data sheets, R.C.A. has been asked to measure the large signal parameters directly.

Several attempts were made to devise a means of interpolating large signal data from small signal information. The following table shows the lack of correlation between small signal and large signal data. Both the large and the small signal data came from the relevant data sheets[2]:

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1. Ref. Motorola "Integrated Circuit Data Book." Appendix 1.
2. R.C.A. Data Sheets "2N5916" and "2N5919".

Transistor	Frequency (MHz)	Z_{in} Small Signal (ohms)	Z_{in} Large Signal (ohms)
2N5916	800	9 + j 7.5	4 + j4
2N5916	400	7.5 + j 2.5	5 + j 0
2N5919	800	2 + j2	4 + j 55
2N5919	400	2 - j 2.5	1.5 + j 1.8

To interpret large signal 'h' parameters from large signal data is a very inaccurate process, especially as all relevant formulae involve sum and difference procedures in which any errors can become severely magnified.

The relevant formulae are:

$$Z_{in} = h_{11} - \frac{h_{12}\,h_{21}}{Y_L + h_{22}} \quad \text{ohms} \quad \text{where } h_{12} = F(h_{11})$$

$$Y_o = h_{22} - \frac{h_{12}\,h_{21}}{h_{11} + Z_s} \quad \text{ohms} \quad \text{where } h_{12} = F(h_{11})$$

5.4 ANALYSES

5.4.1 Linvill Graphs for 2N3866 (Small Signal Class A).

Three 2N3866 transistors are used in the amplifying stages, one in the pre-amp and two in the power-amp. The following analysis applies to the pre-amp transistor and to the first stage of the power amplifier, both of which are working in Class A.

Data is available for this configuration by direct interpretation of the RCA data sheets. h_{11}, is stated directly on the data sheets and h_{12}, h_{21}, and h_{22} calculated as described previously.

All values are taken for f = 190 MHz

$$I_c = 25mA$$

From equations (1) and (2) and the data sheets:

$h_{11} = 24 - j\,2.5$

$h_{22} = (14.5 + j\,7.5)\,10^{-3}$

$h_{12} = (7.8 + j\,75)\,10^{-3}$

$h_{21} = (0.7 - j\,3.9)$ or $(2.83 - j\,2.83)$

The two alternatives listed for h_{21} correspond to the most likely value of phase h_{21} of -85°, and secondly the maximum possible deviation of phase from this value. No measured values of phase are available, but, as will be seen, no serious discrepancy in result is likely to occur by taking the phase of h_{21} to be -85°.

For typical Linvill analysis calculations see Appendix (Section 7.1). The results of these calculations are as follows and may be interpreted on Figure 6. The power output function is a paraboloid with its apex at L = 1, M = 0, at which point

$$\text{output power} = P_{0(o)} = \frac{|h_{21}|^2}{4h_{22r}} = 275$$

The Linvill method of analysis proposes an input current of 1 + j0, so current and power units are arbitrary since ultimately only power gain is of interest

The power input function is a plane of slope,

$$G_r = \frac{|h_{12}\,h_{21}|}{2h_{22r}} = 10$$

The gradient of input power makes an angle 0 with M 0 where 0 = -arg $(-h_{12}\,h_{21})$ 176°.

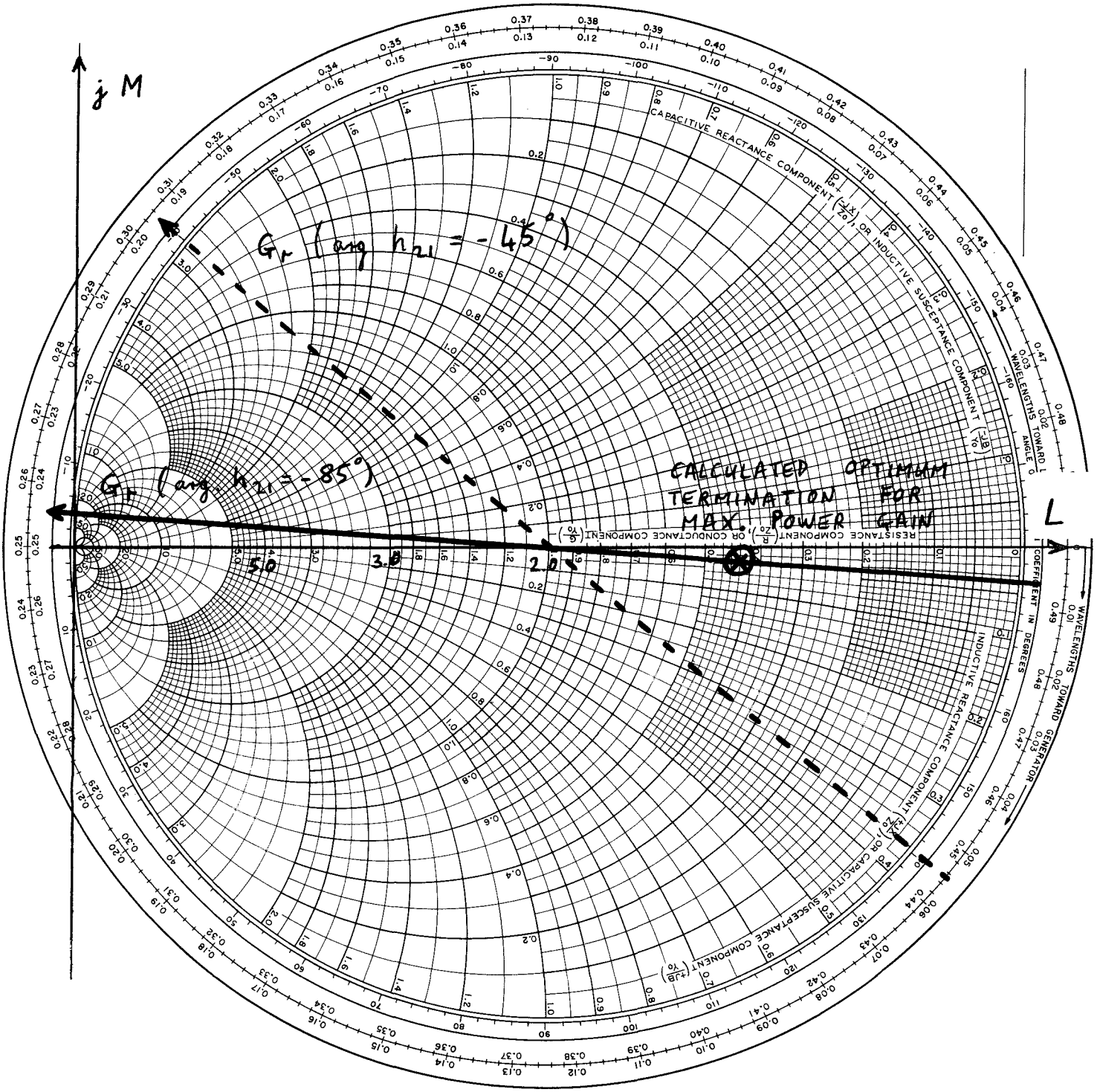


FIGURE 6. Smith-Linvill Chart for 2N3866 Common-Emitter

The value of input power at L = 1, M = 0 is

$$P_{i(o)} = 2h_{11r}h_{22r} - \mathrm{Re}\,(h_{12}h_{21})\ 1/h_{22r} = 13.8$$

These values are for $< h_{21} = -85°$ and are shown on the graph as a full line.

The dotted line is for a transistor of $< h_{21} = -45°$ in which case $\theta = 141°$, $G_r = 10$, $P_{o(o)} = 275$ and $P_{i(o)} = 16$.

It can be seen from the Linvill Chart (Figure 6) that for both arg. $h_{21} = -85°$ and arg. $h_{21} = -45°$ that the transistor is unconditionally stable.

The model used in the following analysis is for the case where $< h_{21} = -85°$. As an estimation of accuracy obtained with using the Linvill method of analysis, some of the analysis is repeated for the limiting case of $< h_{21} = -45°$. Using $< h_{21} = -85°$ the Linvill model for the transistor is a power output parabaloid with a peak power out of 275. Cutting the parabaloid is the power-input plane which has a gradient of $|10|$ at an angle of 176° with the real L axis. The power input plane has a value of 13.8 when the power-output function is at its peak of 275 (at L = 1, M = 0), which gives power gain = 20.

According to Linvill (Ref. 1) the optimum point of operation of the transistor is not at the peak of the parabaloid but at a distance 'd' from the apex along the gradient of input power. 'd' is given by

$$d = \frac{1 - \sqrt{1-C^2}}{C} \quad \text{where } C = \frac{2P_{o(o)}}{P_{i(o)}} \left| \frac{h_{12}}{h_{21}} \right| = 0.76.$$

This gives 'd' = 0.46, at which point power gain = 24. This optimum termination point is marked on the Linvill graph (Figure 6) for the 2N3866 at a distance 'd' from the L = 1, M = 0.

1. Linvill, J. G.; loc. sit

5.4.2 Power Amplifier

The power amplifier is split up into a number of cascaded power-amplifier stages separated by matching networks. There are four stages based on each of the four transistors Q1 - Q4. Included in Section 6 are the analyses of all the matching networks, the results, in terms of the load and source impedances seen by each transistor stage, are used in this section. The results used are those for the average settings of variable capacitors found from experimental results of tuning the transmitter.

5.4.2.1 First Stage

Load impedance = 95 + j68 ohms

$\therefore Y_L = (7-j5)\ 10^{-3}$ mhos

$Y_L + h_{22} = 21.5 + j2.5 \quad (1.5 + j\ 17)\ h_{22r}$

It is now possible to plot the load termination directly on the Smith Chart for the 2N3866 in terms of G + jB, where $Y_L + h_{22} = G + jB$. Having defined the point of operation it is possible to directly interpret power out, power in, and hence power gain, as well as the effective input impedance of the circuit. It can be seen that the point of operation of Q1 is very close to the predicted optimum termination, and gives max gain. (i.e., operation on power-output paraboloid at 80% of peak power).

From Figure 7 , $P_o = 0.8\ P_{o(e)}$

$$P_i = P_{i(o)} - |G_r|\ x = 13.8 - (.4)\ (10)$$

$\therefore$ Power gain in transistor $= \frac{P_o}{P_i} \quad \frac{0.8\ (275)}{13.8-(.4)10} = 23 = 13.6$ dB

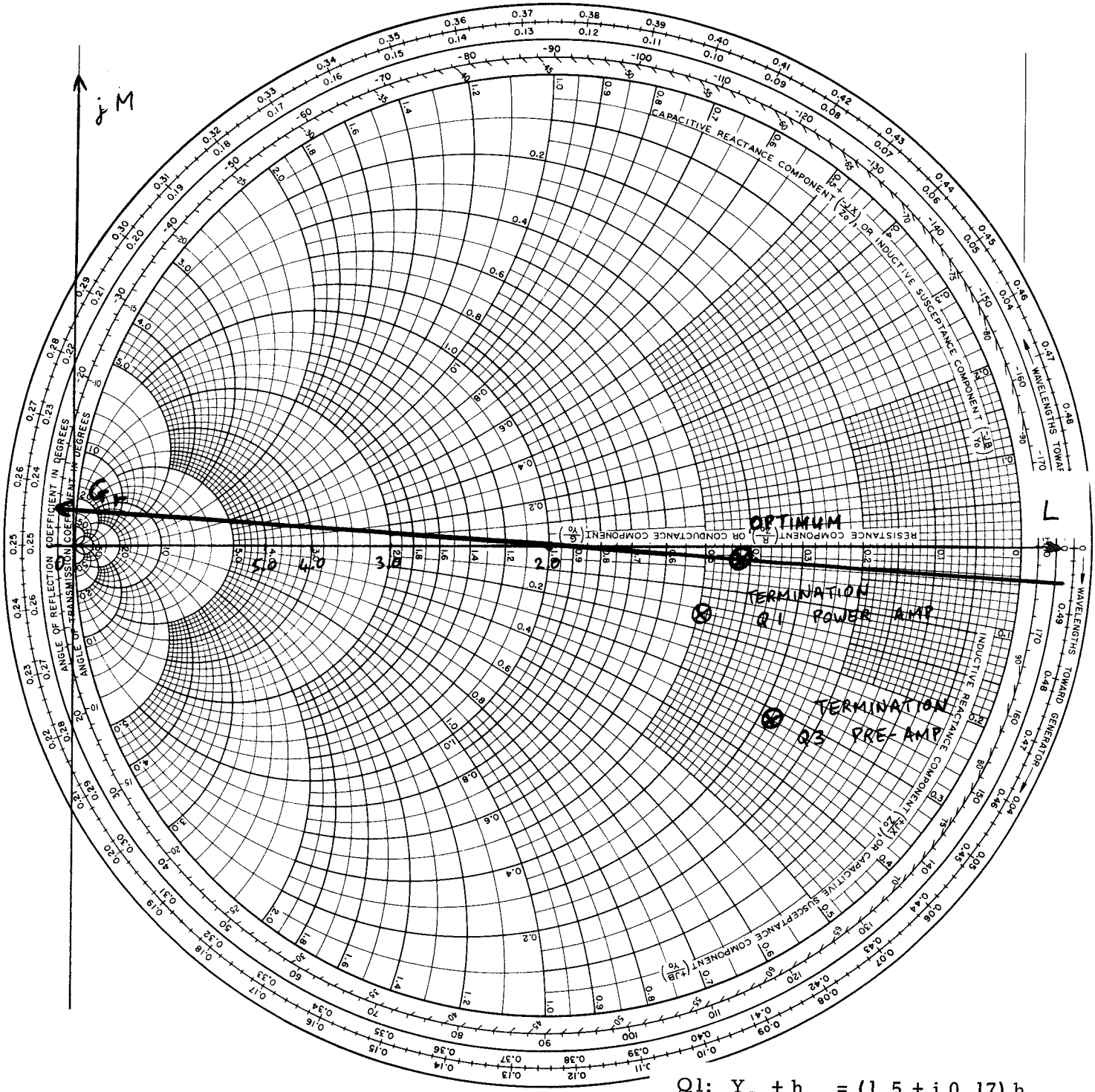
Also input impedance $= h_{11} + R + j\ X_1$ ohms

where from the chart $R = -1.37\ |G_r| = 13.7$

$$j\ X_1 = j0$$

results in $Z_{in} = 10.3 - j\ 2.5$

These figures were obtained using arg. $h_{21} = -85°$.



Q1: $Y_L + h_{22} = (1.5 + j\,0.17)\, h_{22r}$

Q3: $Y_L + h_{22} = (1.28 + j\,0.32)\, h_{22r}$

FIGURE 7. Smith-Linvill Chart for Q1 Power Amplifier & Q3 Pre-Amplifier

Should the limiting case of -45° be used; the results give P_G = 14.6 dB. and stable operation. Q1 should therefore give at least 13.6 dB gain or 14.6 dB at very maximum.

It should be noted here that the source impedance for Q1, assuming a 50Ω source to the power amplifier complete, is calculated to be 5 + j 2.5 (Section 6.2.1). This means that there is a resistive mismatch which is equivalent to a 1.6 dB power loss.

5.4.3 Pre-Amplifier

The pre-amplifier circuit is split up, as is the power amplifier, into discrete power stages. All the transistors Q1 - Q3 are susceptible to the Linvill method of analysis, and the resulting plots are shown in Figures 7 to 9 for Q3 (2N3866) and Q1, Q2 (2N918).

5.4.3.1 Third Stage (Q3)

It becomes more practical to consider the latter stages first as it is necessary to know the load admittance presented to each gain stage.

Stage 3 is a common emitter stage with a poorly grounded emitter. The emitter impedance at 190 MHz is - j 20 ohms and must be allowed for in the calculations of power gain and stability.

The load admittance is (4 - j 2.9) mmhos, assuming an average value of C12 of 9 pF.

The relevant Smith Chart for the transistor is shown in Figure 7 and is equivalent to the one for the first stage of the Power Amplifier.

For this termination the following values of power gain and input impedance are apparent.

$$Y_L + h_{22} \quad (1.28 + j.32)\, h_{22r}$$

$$P_o = 0.65\, P_{o(o)} = 180$$

$$P_i = 13.8 - .55\,(G_r) = 8.3$$

$$\frac{P_o}{P_i} = 21.5 = \underline{13.5\ dB}$$

The input impedance = $h_{11} + R + jX$.

of the transistor

where $R = -4|G_r| = -14$

$jX = j.3|G_r| = j3.3$

$Z_{in} = 10 + j0.5$

Including

-j20 Ω emitter impedance

Z_{in} Total = $\underline{10 - j19.5\Omega}$

This stage is working very efficiently, close to maximum gain. Both 2N3866 stages appear to be well designed and operate close to optimum power gain.

5.4.3.2 Second Stage (Q1)

This particular transistor is in a common base configuration for which no transistor parameters are directly available. It is possible to calculate common base parameters from common emitter parameters, which in this case are only available for a 'y' parameter model. It is also possible to convert between 'h' parameters and 'y' parameters so that, given common emitter 'y' parameters, it is possible to generate common base 'h' parameters. This was tried with little success since the computation for calculating h_{22} is as follows:

$$h_{22} = \frac{y_{11}\, y_{22} - y_{12}\, y_{21}}{y_{11}}$$

This expression results in a small negative value for h_{22} which is difficult to interpret physically and indicates the limited power of such conversions. It appears that any calculations of transistor behavior at the frequencies of interest must be based on relevant data for the particular configuration in question. Ordinary methods of interpretation of one set of parameters from another set are inaccurate at these frequencies. All that are available in data on the 2N918 are 'y' parameters so it would seem logical to use 'y' parameters directly in the Linvill Analysis. This is possible and all the relevant Linvill parameters are readily calculated in terms of 'y' parameters.[1] All that is necessary is a conversion between common emitter and common-base configuration, which is reasonably accurate.

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1. Laucher, J. and M. Silverstein: "Design High-Frequency Amplifiers Graphically," Electronic Design, 12 April 1966.

The transistor Q1 is not strictly in a grounded base configuration since there is a capacitor on the base which goes to ground having a reactance of -j 20 ohms at the frequency of interest.

Common Base Configuration

$$Y_{11(b)} = (51.7 - j\,42.5)\,10^{-3}$$

$$Y_{12(b)} = -(0.2 + j\,1)\,10^{-3}$$

$$Y_{21(b)} = -(45.2 - j\,4.8)\,10^{-3}$$

$$Y_{22(b)} = (0.2 + j\,2.1)\,10^{-3}$$

$\therefore$ Max power out $= P_{o(o)} = \dfrac{Y_{21}}{4\,\mathrm{Re}\,Y_{22}} = \underline{5.5}$ watts

$$\text{Power in} = P_{i(o)} = \mathrm{Re}Y_{11} - \frac{\mathrm{Re}\,(Y_{12}\,Y_{21})}{2\,\mathrm{Re}\,Y_{22}} = \underline{0.088}\ \text{watts}$$

The gradient of input power $= G_r = \dfrac{(Y_{12}\,Y_{21})}{2\,\mathrm{Re}\,Y_{22}}\ e^{j\theta} = \underline{0.14}\ e^{j\theta}$

$$\text{Where } \theta = \tan^{-1}\frac{\mathrm{Im}\,(Y_{12}\,Y_{21})}{-\mathrm{Re}\,(Y_{12}\,Y_{21})} = 148^{\circ}$$

Therefore the transistor has a large area of instability over the shaded area shown.

The terminating impedance for this stage is 15 + j 182 ohms which is equivalent to $Y_L = (0.4 - j\,5.4)$ mmhos.

$$Y_L + Y_{22} = 0.4 - j\,5.4 + 0.2 + j\,2.1$$

$$= 0.6 - j\,3.3 \text{ mmhos}$$

$$Y_L + Y_{22} = (3 - j\,16)\,h_{22} = G + jB$$

This is plotted directly on the Smith Chart, Figure 8, and represents the point of operation of the transistor. It can be seen from the Linvill graph for the common base 2N918 that the transistor is operating very close to the boundary of the chart, where the power output function goes rapidly to zero. Very little gain can be expected here and any estimate of power gain using the Linvill method of analysis will be of limited accuracy, due to the difficulty of reading values in this region. However it can be clearly seen that the transistor is very stable and gives approximately 9 dB of gain.

From the Smith Chart,

Power Out $P_o \quad \frac{0.55}{0.3} P_{o(o)}$

Power In $P_{in} = \frac{1.125}{3.6} G_r = -4$

$\therefore \frac{P_o}{P_1} \quad 7.5 \quad 9 \text{ dB}$

The input impedance Z_{in} of Q3 is given by

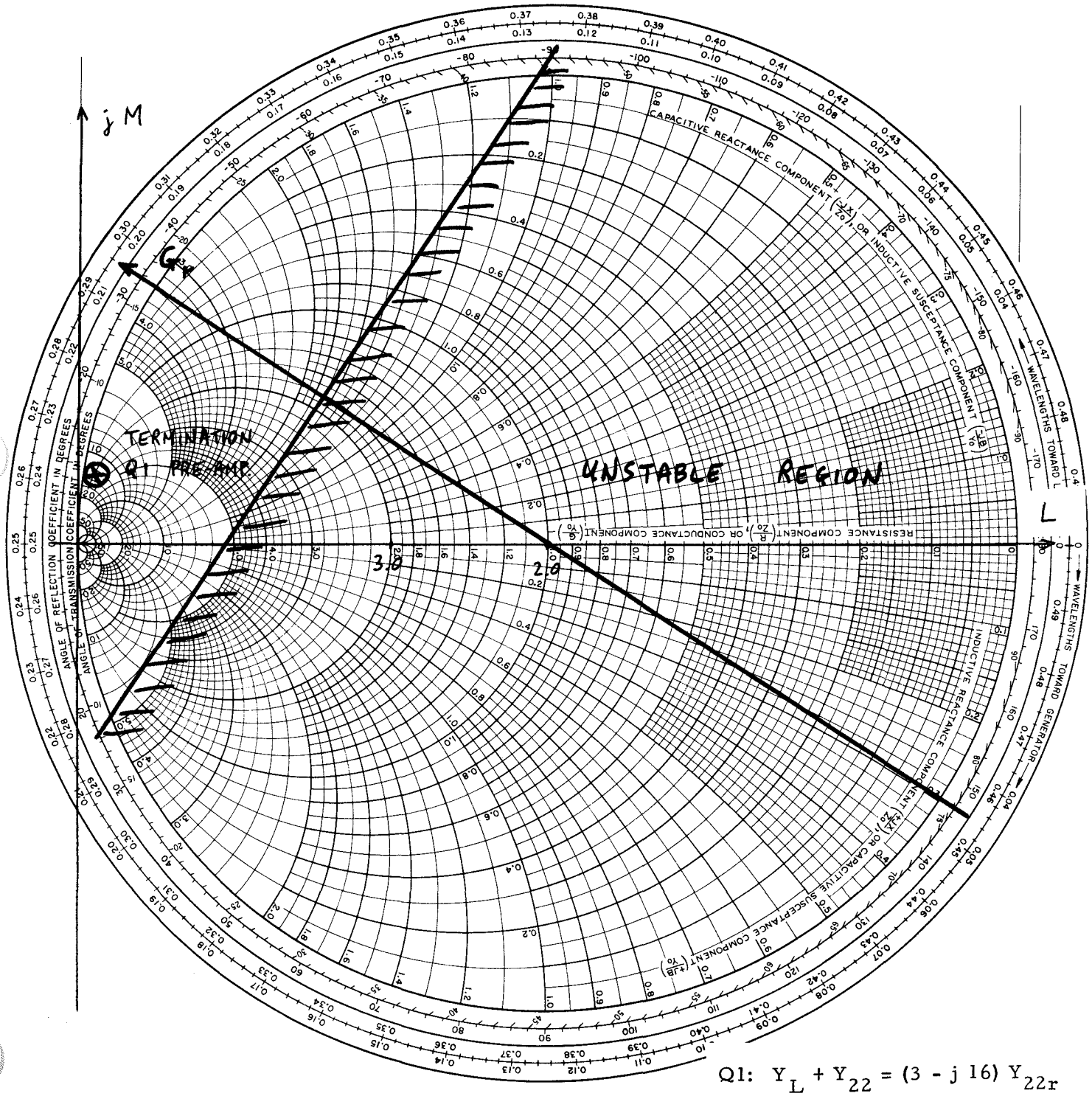
$$\frac{1}{Z_{in}} = Y_{in} = Y_{11} - \frac{Y_{12}\,Y_{21}}{Y_{22} + Y_L}$$

Which gives $Z_{in} = 14 + j\,14$ ohms

5.4.3.3 First Stage (Q2)

This transistor is in common-emitter configuration.

The 'y' parameters governing its behavior are directly determined from the data sheets as follows:



Q1: $Y_L + Y_{22} = (3 - j\,16)\,Y_{22r}$

FIGURE 8. Smith-Linvill Chart for Q1 Pre-Amplifier, Common Base 2N918

$$y_{11} = 6.5\ (1 + j)\ 10^{-3}$$

$$y_{12} = (-j\ 1.1)\ 10^{-3}$$

$$y_{21} = (45 - j\ 50)\ 10^{-3}$$

$$y_{22} = (0.2 + j\ 2.1)\ 10^{-3}$$

The Linvill Chart, Figure 9, is characterized as follows:

$$\text{Max Power Out} = P_{o(o)} = \frac{Y_{21}^{\ 2}}{4\ \text{Re}\ Y_{22}} = 5.5$$

$$\text{Max Power In} = P_{i(o)} = \text{Re}\ Y_{11} - \frac{\text{Re}\ (Y_{12}\ Y_{21})}{2\ \text{Re}\ Y_{22}}$$

$$= 0.146$$

$$\text{Angle of input power gradient} = \arg.(Y_{12}\ Y_{21}) = -45^{o}$$

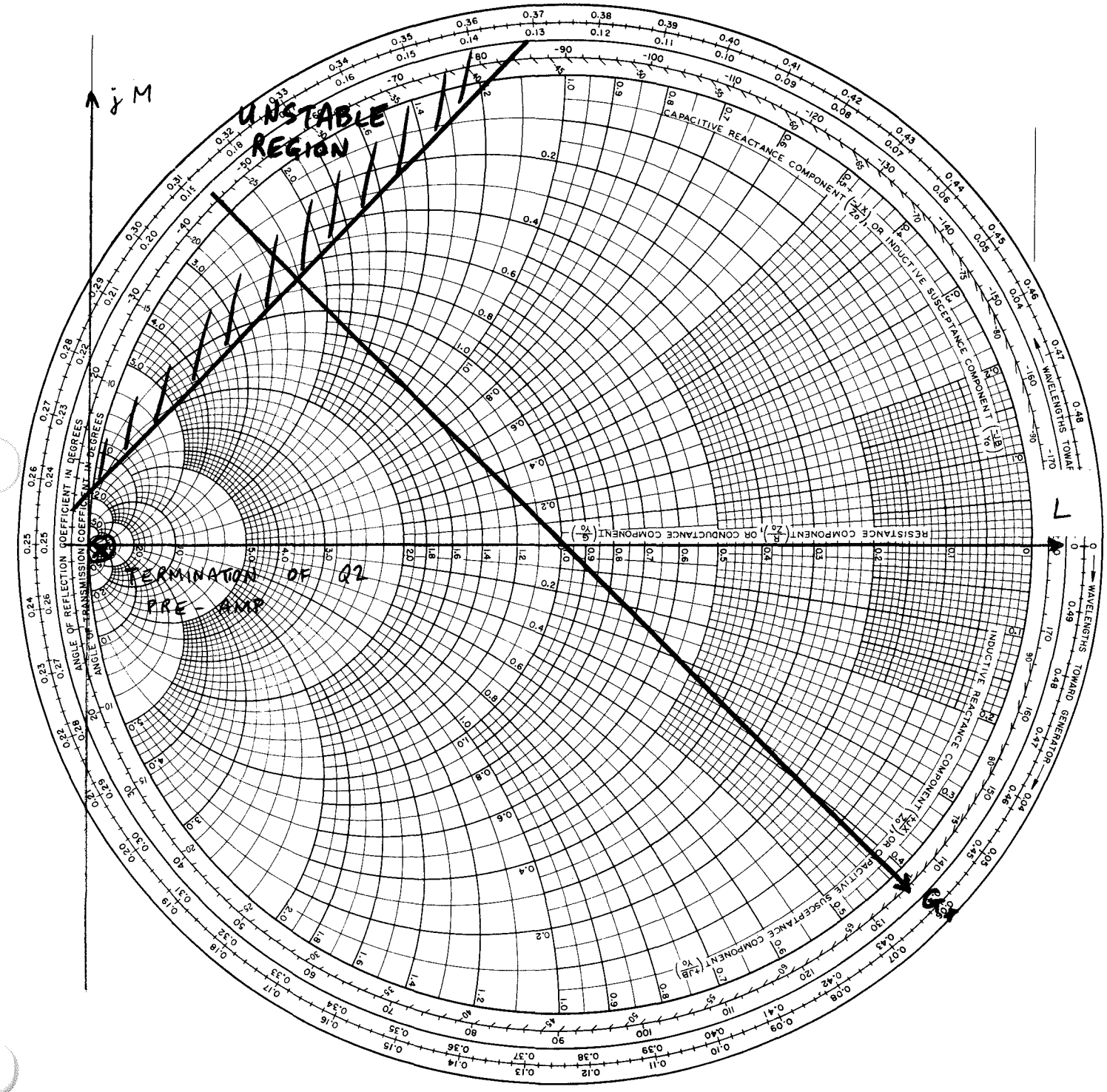
$$\text{Input power gradient} = G_r = \frac{Y_{12}\ Y_{21}}{2\ \text{Re}\ Y_{22}} = 0.180$$

The load presented to the transistor (Section 6) includes the emitter impedance and is calculated to be (16.4 + j 2.4) mmhos. This value of termination is plotted on the Smith Linvill Chart shown in Figure 9. It can be seen that for this value, the transistor is once again stable but is operating at fairly modest gain.

Therefore from the Smith Linvill Chart

$$\text{Power out at } (Y_L = 16.4 + j\ 2.4) = \frac{(P_{o(o)})}{3 \times 10} = .18$$

$$\text{Power in} = \frac{5}{8}\ \frac{1}{3.6}\ (G_r) = .03$$



Q2: $Y_L + Y_{22} = (83 + j\ 22)\ Y_{22r}$

FIGURE 9. Smith-Linvill Chart for Q2 Pre-Amplifier Common Emitter 2N918

Power Gain = P_G - 6 8 dB

The input admittance of Q_2 = $Y_{11} - \frac{Y_{12} Y_{21}}{Y_{22} + Y_L}$

Y_{in} = (8.5 + j 10.6) mmhos.

∴ For the whole preamplifier the input impedance presented to the modulator is 62 - j 80 ohms.

The total gain of the preamplifier for small signals, before any saturation occurs, is (9 + 8 + 14) dB 31 dB.

There is no chance of instability occurring with matching networks as they are. This is evidently so by examination of the three Linvill charts, which show that the terminating admittances are well away from the unstable areas.

Considerably more gain could be achieved in the first two stages with better matching networks, by moving the terminating admittances on the Linvill chart. All terminations occur in areas of the Linvill Charts where the Power Gain is rapidly changing.

The advantage of operating close to the boundary of the Linvill Chart is that changes of output impedance have less effect on gain and input impedance than the case where the transistor is operated closer to the unstable region or power-output apex. This is especially important where the transistor is only conditionally stable. Maximum attention has thus been paid to stability in the first two stages with the resultant modest gains.

The last stage of the preamplifier is unconditionally stable, so less attention is paid to stability and the stage is tuned up for near-to-maximum power gain.

5.4.4 Power Amplifier - Stages 2, 3 and 4.

The last three stages of the power amplifier are not so easily analyzed as the previous stages since small signal parameters no longer apply. As previously explained under Section 5.2, "Interpretation of Large Signal Parameters", it is not possible to extrapolate or interpolate existing small-signal data to cover large-signal parameters, nor is it easy to accurately interpret large signal 'h' parameters from large signal input/output impedance data. There appears to be little point in even making an estimate of these variables as the Linvill analysis requires reasonably accurate values of 'h' parameters.

Having obtained values of 'h' or 'y' parameters it would be possible to use the full Linvill analysis as before, and determine the stability and power gain of these stages.

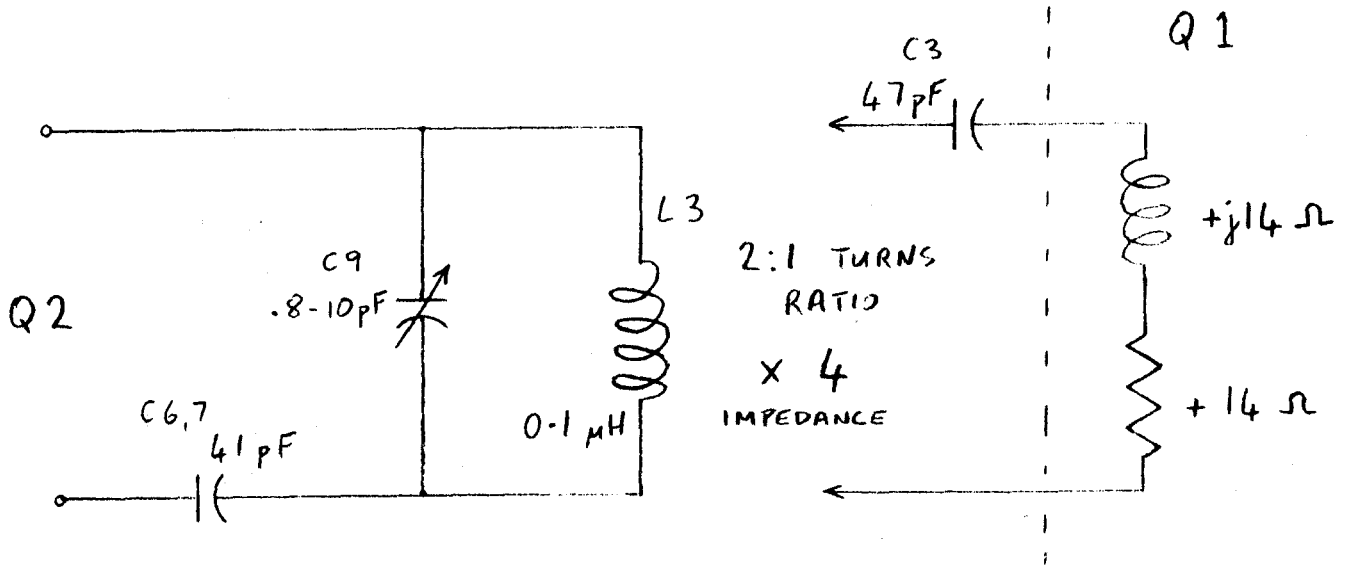
It must be emphasized that, at these frequencies and power levels, nothing short of direct parameter measurements at the collector current, input power and frequency used, will suffice. Using any other data, it is possible to prove almost anything with a suitable collection of numbers and equations. It was for this reason that RCA has been asked to measure the relevant parameters at the correct operating conditions, however this data has not yet been obtained.

6. INTERSTAGE NETWORKS

6.1 PRE-AMPLIFIER

6.1.1 Q2 - Q1 Interstage

This network matches Q2 output to Q1 input in the cascode pair Q1, Q2. The network has the following form:



From the previous stability considerations the input impedance of Q1 was found to be 14 + j 14 ohms. An impedance/admittance chart is shown in Figure 10 giving the range of Q2 output impedance that can be matched. Using a typical capacitor setting for C9 of 1.5 pF the output impedance of Q2 that can be matched is shown to be 60 + j 9 ohms.

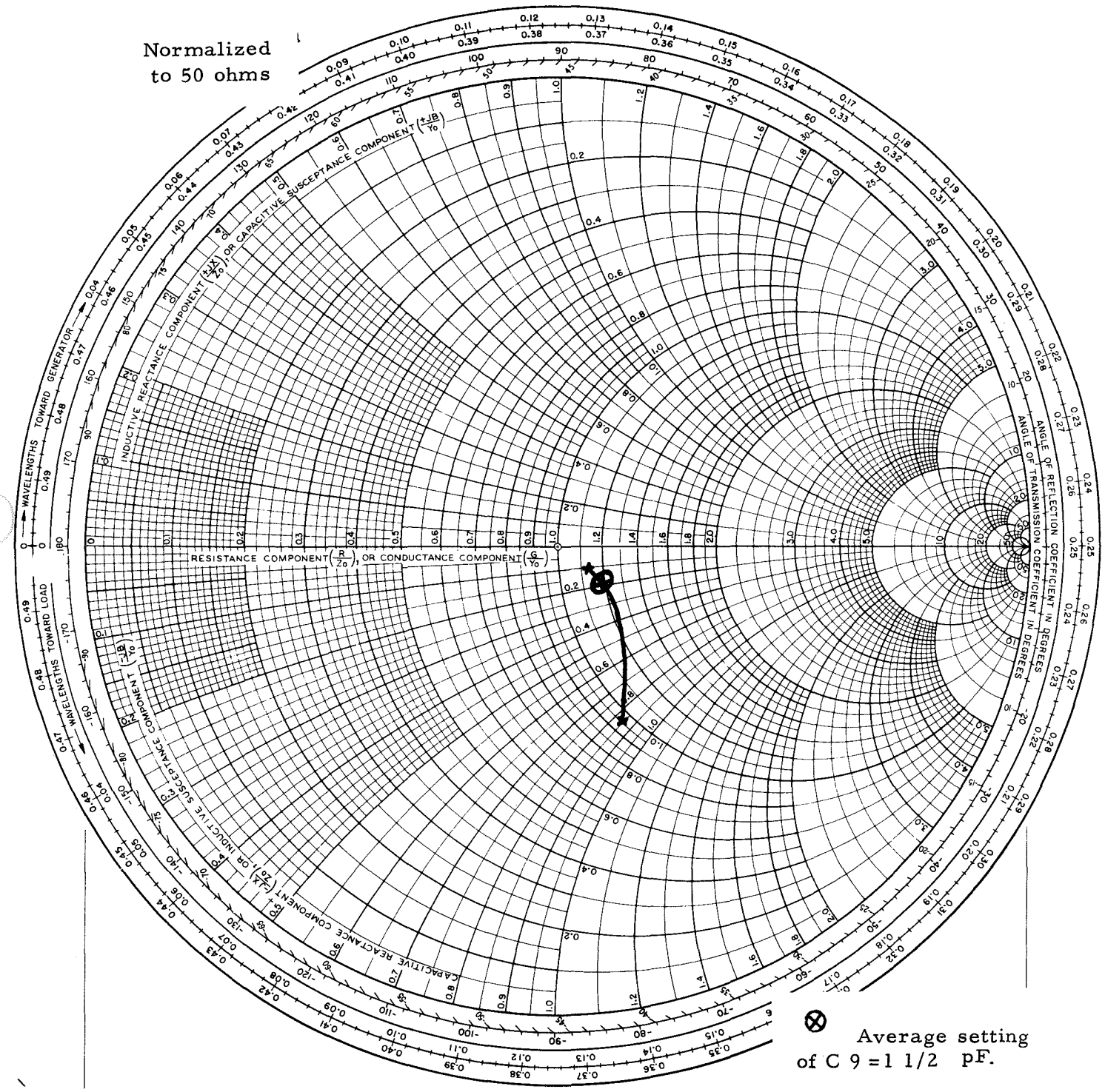
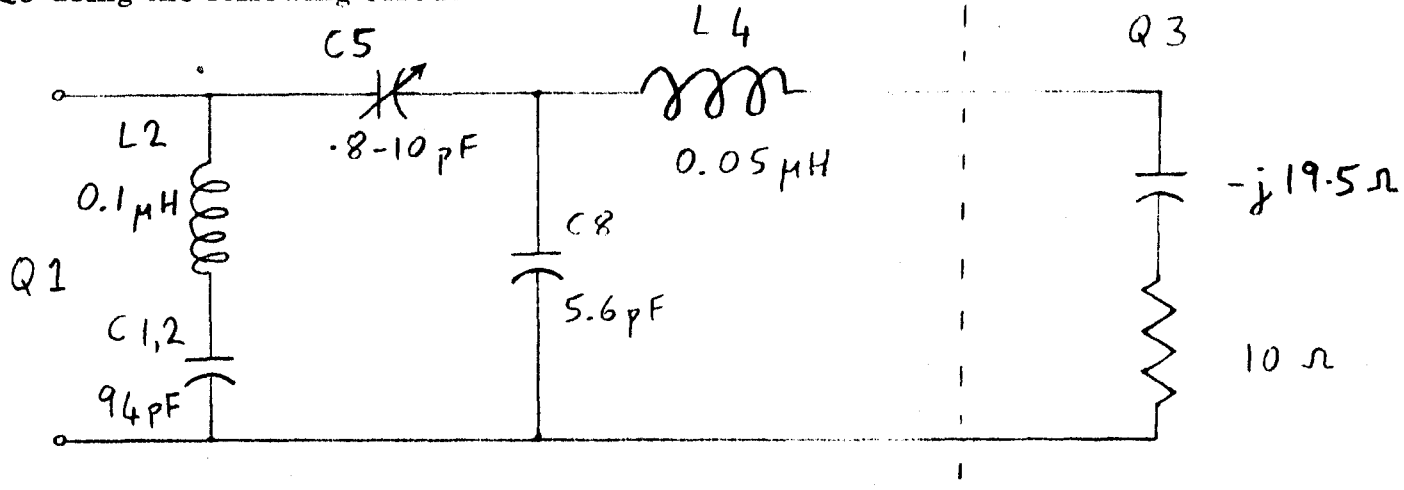


FIGURE I0. Impedance Chart for Q 2 - Q I Interstage of Pre-Amplifier.

6.1.2 Q1 - Q3 Interstage Network

This network matches the output of Q1 to the input impedance of Q3 using the following circuit:



The input impedance of Q3 was obtained from a Linvill Chart for that transistor[1]. From this value, an impedance chart Figure 11 was plotted showing the variation of matched impedance with varying values of C5. Using an average setting of 2.5 pF for the value of C5, a load impedance of 15 + j 182 ohms, was obtained for the network. The output impedance of Q1 is the conjugate of this, i.e., 15 - j 182 ohms.

6.1.3 Q3 Output Network

This circuit matches the output impedance of Q3 into the 50 ohm attenuation pad feeding the power amplifier. The equivalent circuit of the network is:

---

[1] Section 5.4.3.1

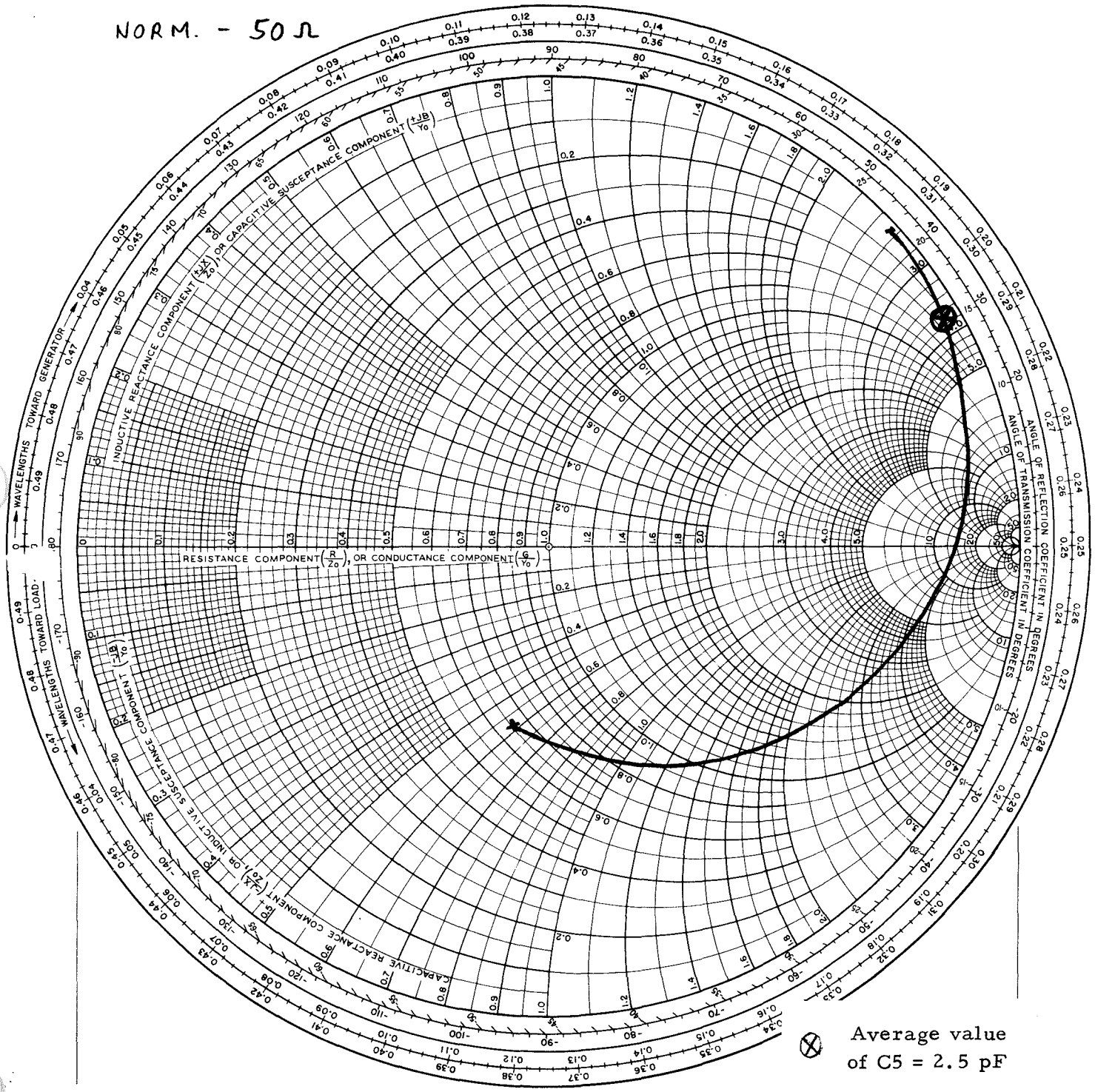
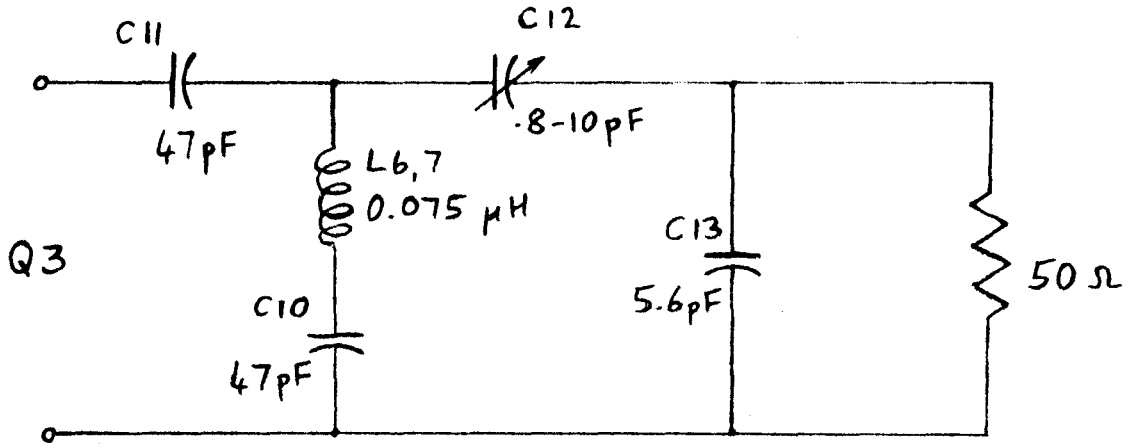


FIGURE 11. Impedance Chart for Q1-Q3 Interstage of Pre-Amplifier.

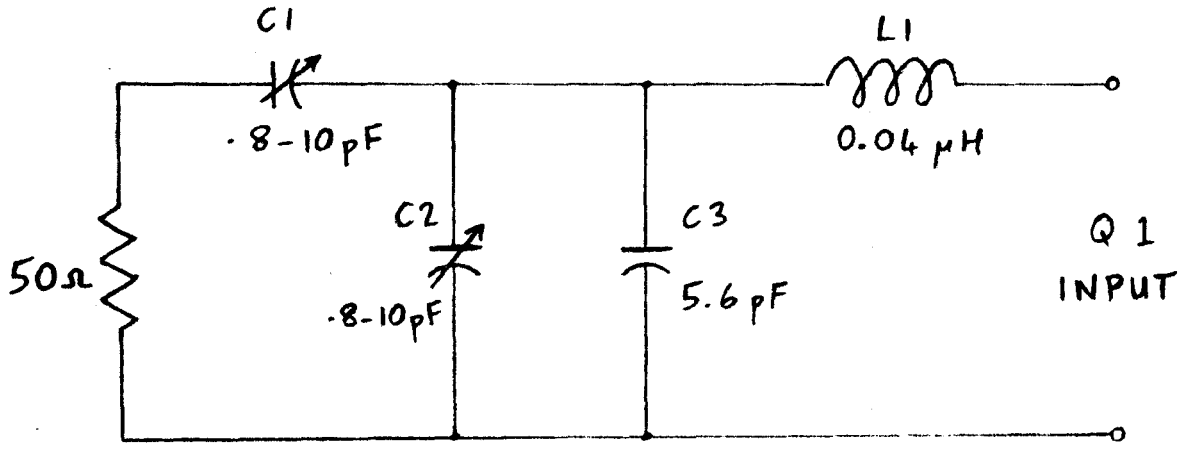


The variation in load impedance of the network is shown plotted on an impedance chart, Figure 12. This chart also shows a value of 165 + j 120 ohms for the load impedance with C12 set at its average value of 9.0 pF. The conjugate output impedance of Q3 is therefore 165 - j 120 ohms.

6.2 POWER AMPLIFIER

6.2.1 Q1 Input Network

This network matches from the 50 ohms, 3 dB resistive pad at the output of the preamplifier, into the power amplifier. The circuit is as follows:



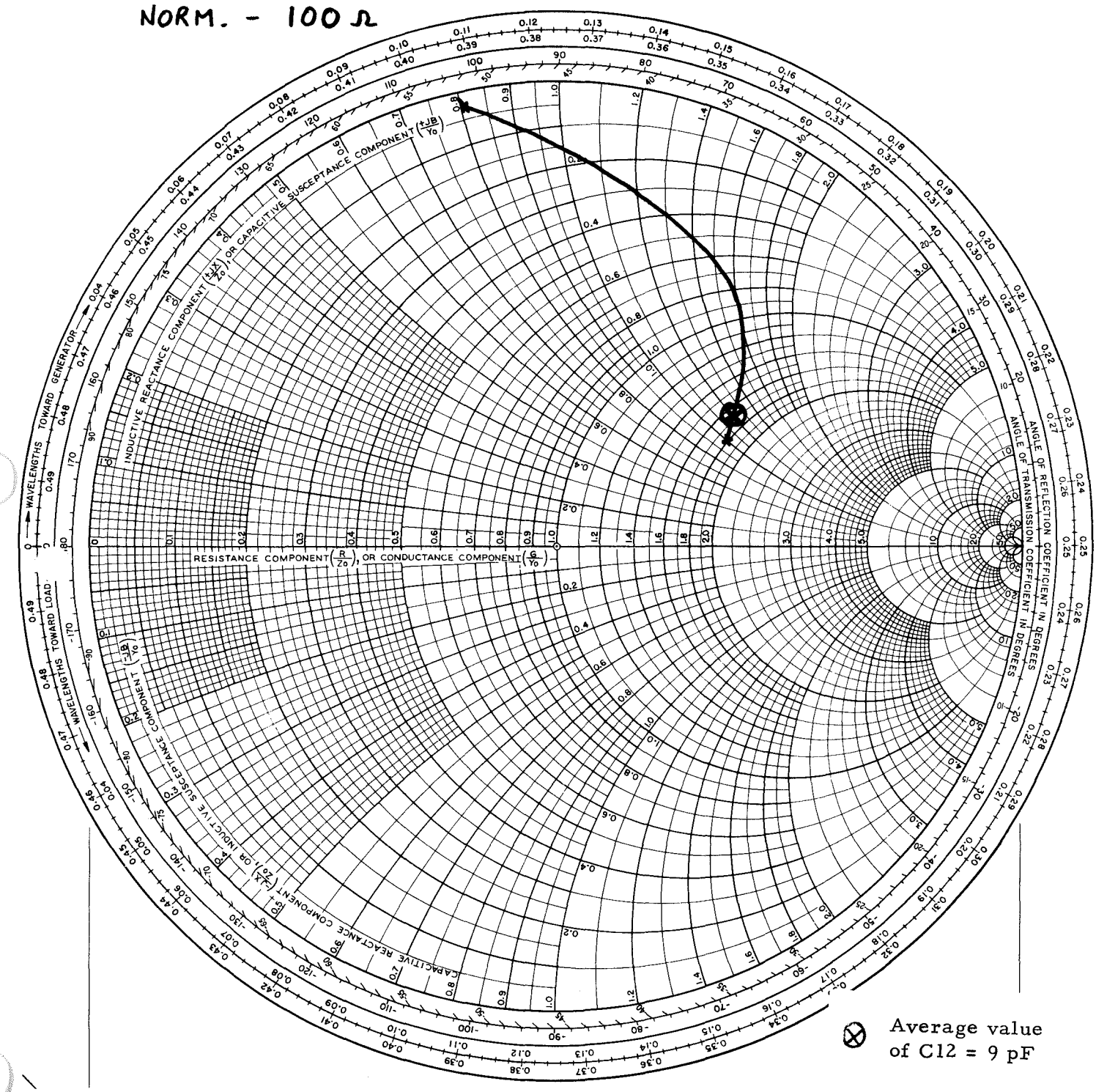


FIGURE 12. Impedance Chart for Q3 Output Network of Pre-Amplifier.

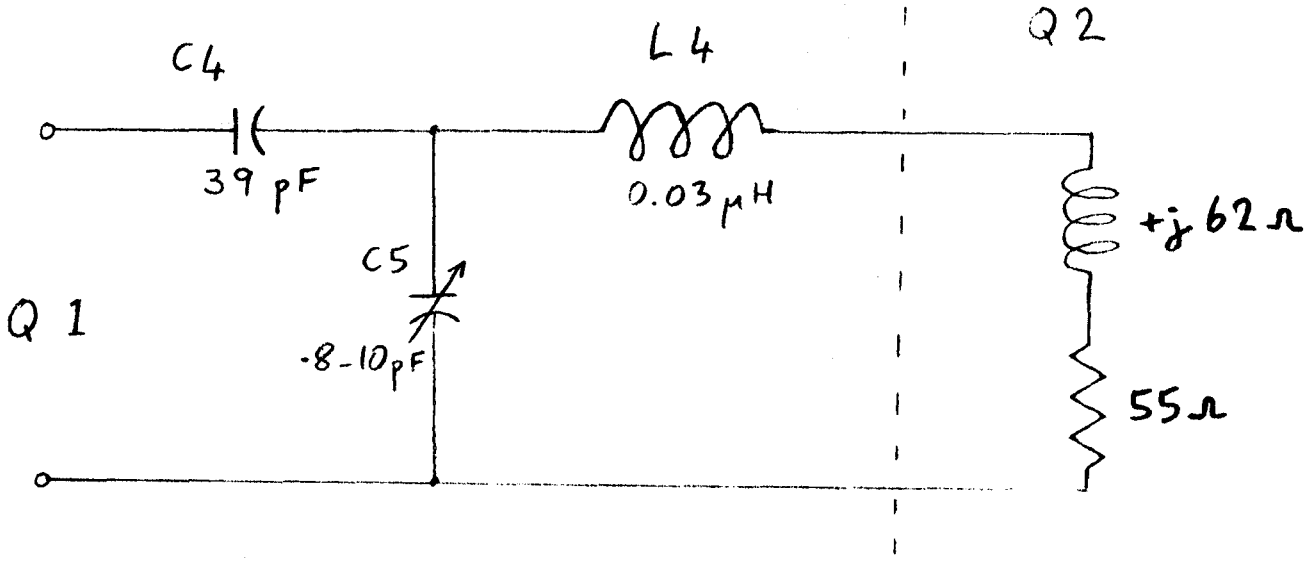
From the accumulated data on the power amplifiers SN 1, 3 and 4 the average values for the capacitor settings are C1 = 7 pF and C2 = 8 pF.

Using these values, the impedance/admittance chart was plotted, Figure 13, and gave a value of 5.0 - j 2.5 ohms for the input impedance of Q1.

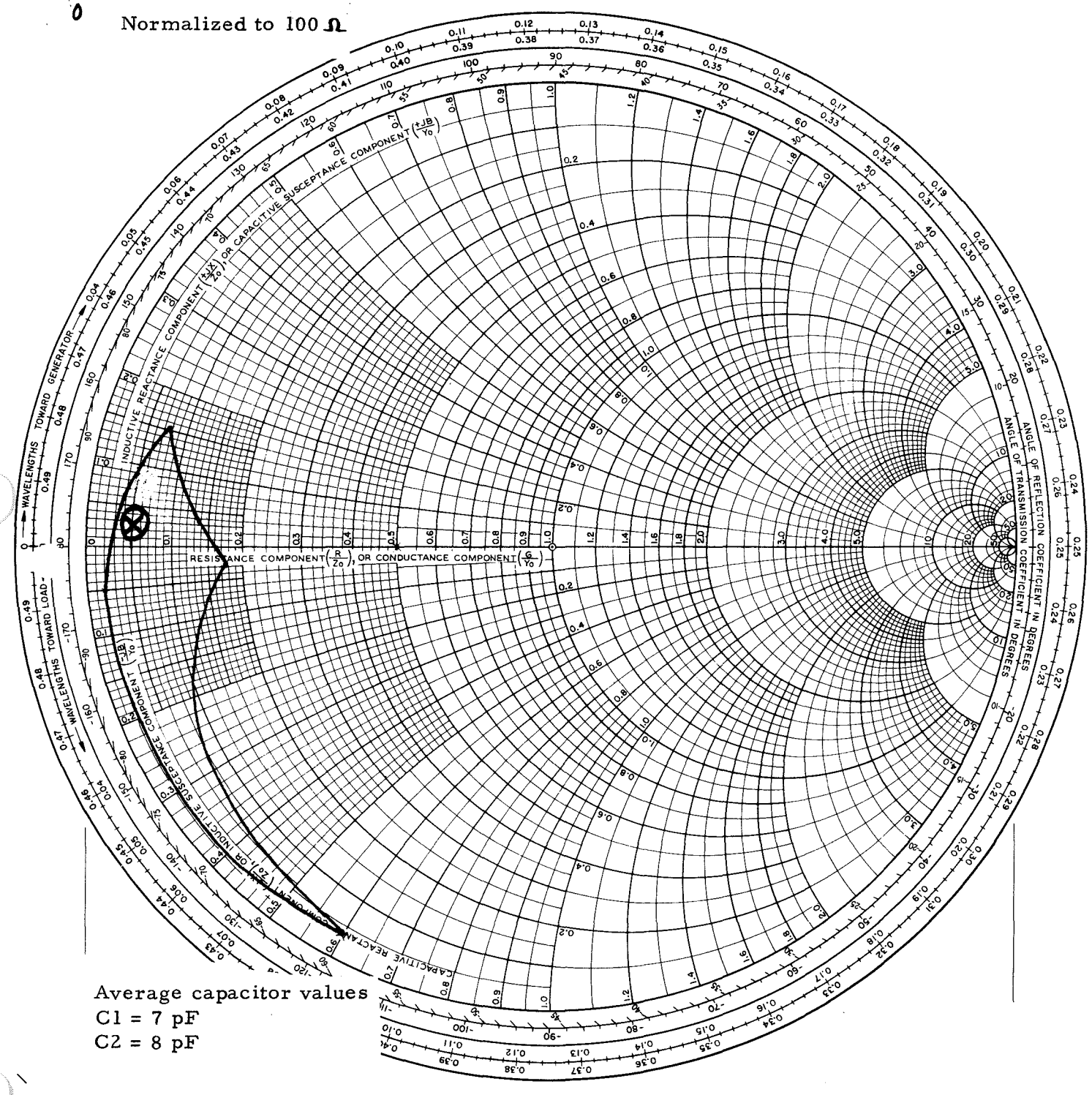
The chart also shows the variation of input impedance of Q1 that can be matched into a 50 ohm source impedance.

6.2.2 Q1 - Q2 Interstage Network

This network matches the output impedance of Q1 into the input of the doubler stage Q2. The network is of the following form:



The input impedance of Q2 was measured at 190 MHz and found to be 55 + j 62 ohms. An impedance/admittance chart was plotted, Figure 14, which shows the range of output impedance of Q1 that can be matched into Q2. With C5 in its average position, giving a capacitance of 2.5 pF, the load impedance is 95 + j 68 ohms, for the network. This matches an impedance of 95 - j 68 ohms for the Q1 output.



Average capacitor values
C1 = 7 pF
C2 = 8 pF

FIGURE 13. Impedance Chart for Q1 Input Network of Power Amplifier.

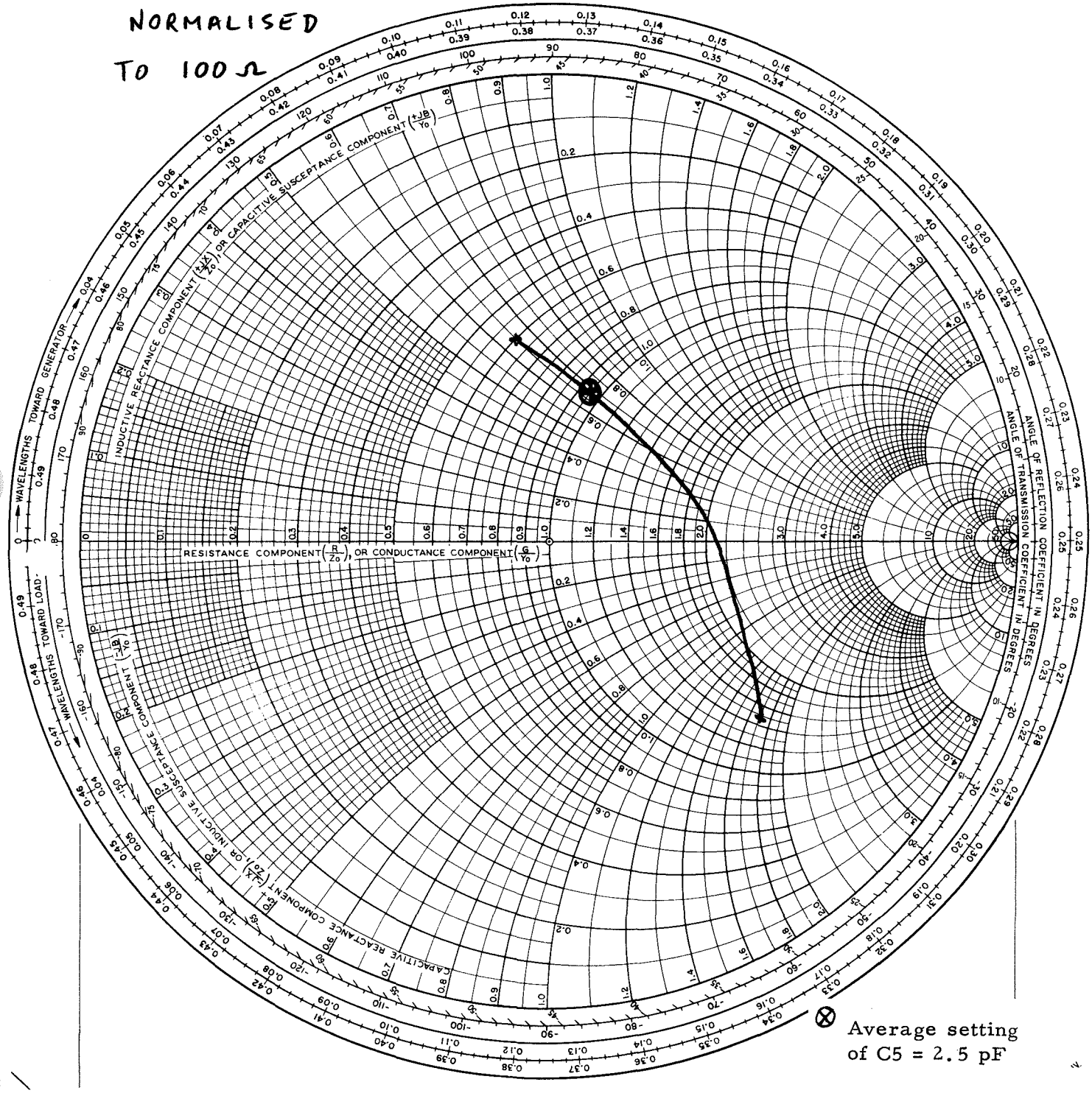
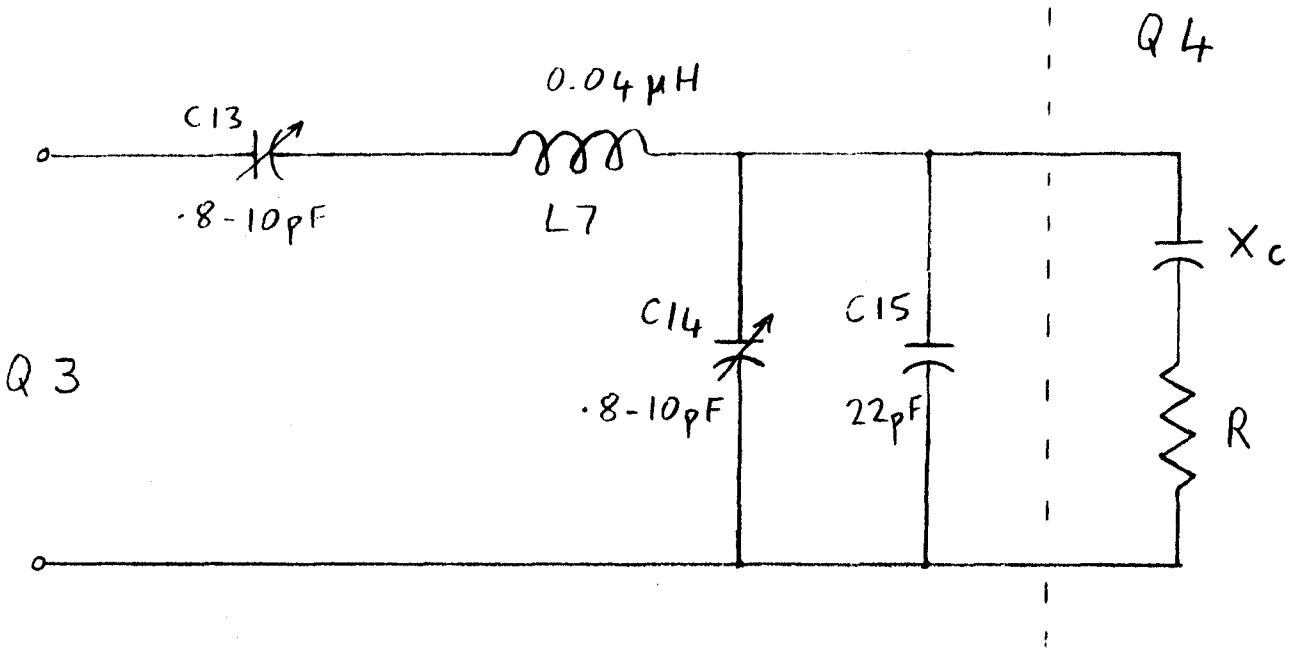


FIGURE 14. Impedance Chart for Q1 - Q2 Interstage Network of Power Amplifier.

6.2.3 Q3 - Q4 Interstage Network

This coupling network is of the following form:



Input impedance of Q4 (2N3375 at 380 MHz) was obtained from the Motorola Application Note, AN282[1], as follows:

Parallel input resistance = 8 Ω

Parallel input reactance = 50 pF = - 6 j Ω

therefore, for the series case:

$$R = \frac{8}{1 + \left(\frac{8}{6}\right)^2} = \frac{8}{2.78} = 2.87\ \Omega$$

[1] Hejhall, Roy, "Systemizing RF Power Amplifier Design", Application Note, AN-282. Motorola Semiconductor Products, Inc.

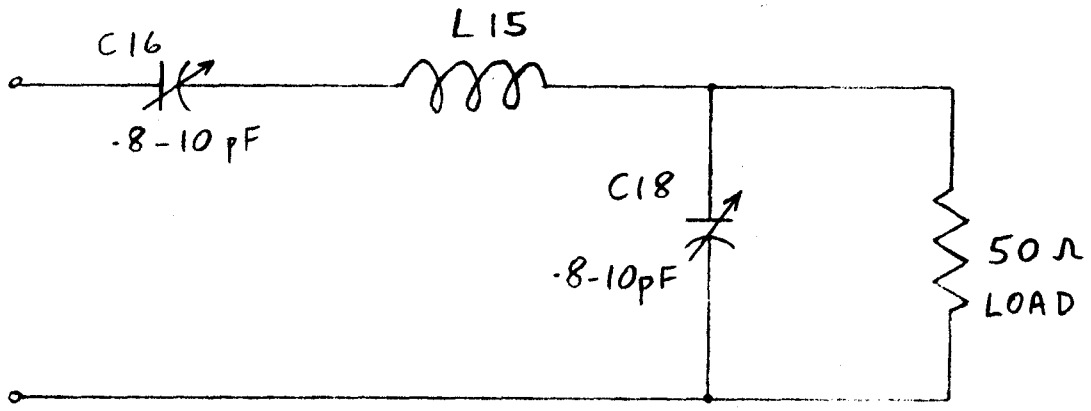
$$XC = -2.87 \times \frac{8}{6} = -j\,3.82\,\Omega$$

At 380 MHz, a 6.2 pF capacitor of the type used for C15 was measured with 1/4 inch lead lengths, and found to be 22 pF.

Using these values, an impedance/admittance chart was plotted, Figure 15 and this shows that the interstage network matches Q4 input to an impedance of 2 + j 38 ohms, for the output of Q3. With the lack of data for transistor Q3, this cannot be verified, but the real part appears to be far too small, and the imaginary part has the wrong sign. This could be checked with full data for the 2N3375 when it is available.

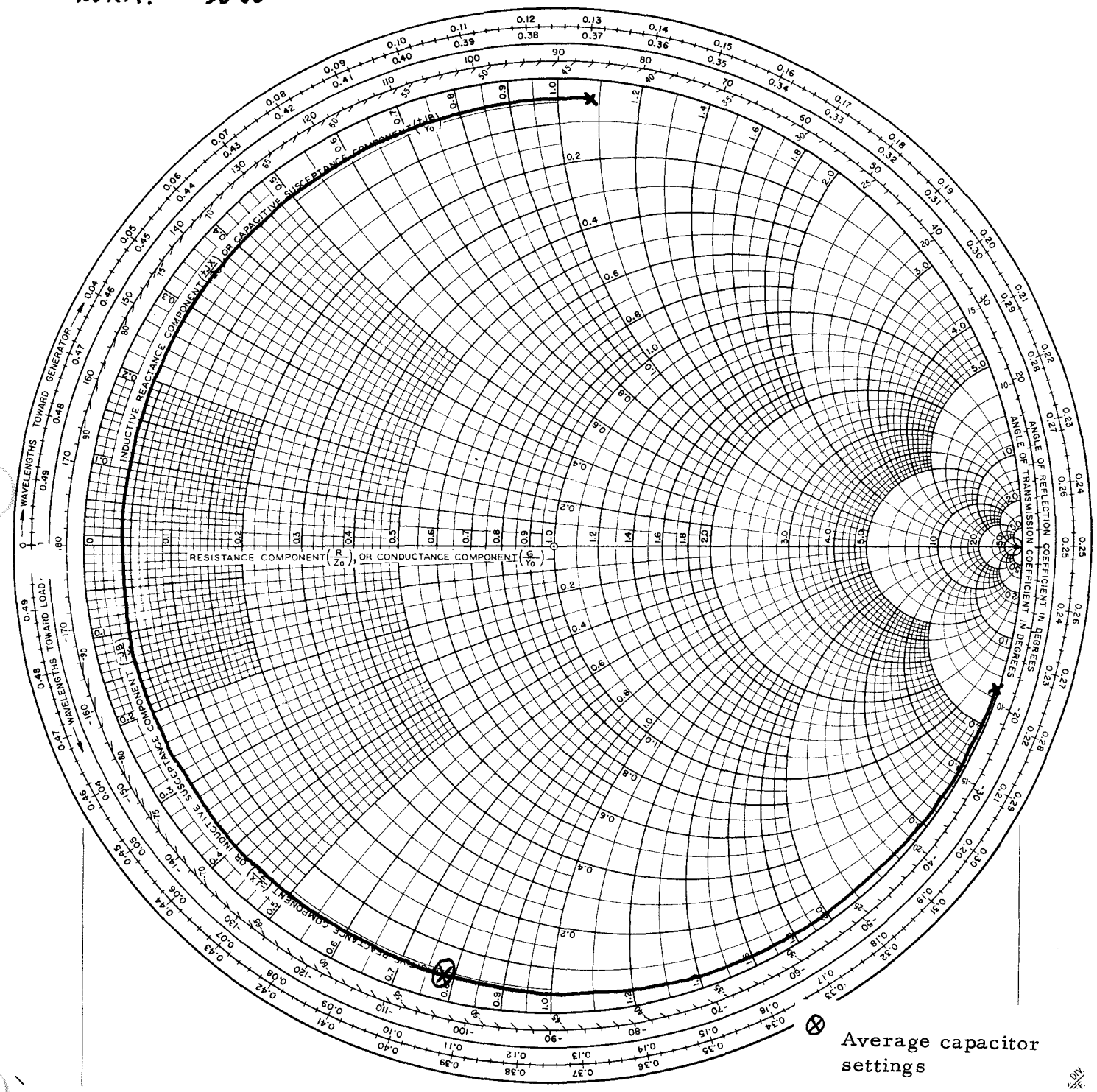
6.2.4 Q4 Output Network

This coupling network was altered to permit better matching to various load impedances. The new circuit is:



and it was this network that was analyzed. The range of output impedance of Q4 that can be matched into 50 ohms is shown in two forms on the following pages. One is an impedance/admittance chart, and the other shows output impedance matched for 1 pF variations in both of the capacitors. These figures show that if Q4 output impedance is about the value shown on the data sheet, then this network is capable of matching Q4 into 50 ohms, in series with up to j 50 ohms of either inductance or capacitance.

NORM. - 50 Ω



Average capacitor settings

FIGURE 15. Impedance Chart for Q3 - Q4 Interstage Network of Power Amplifier

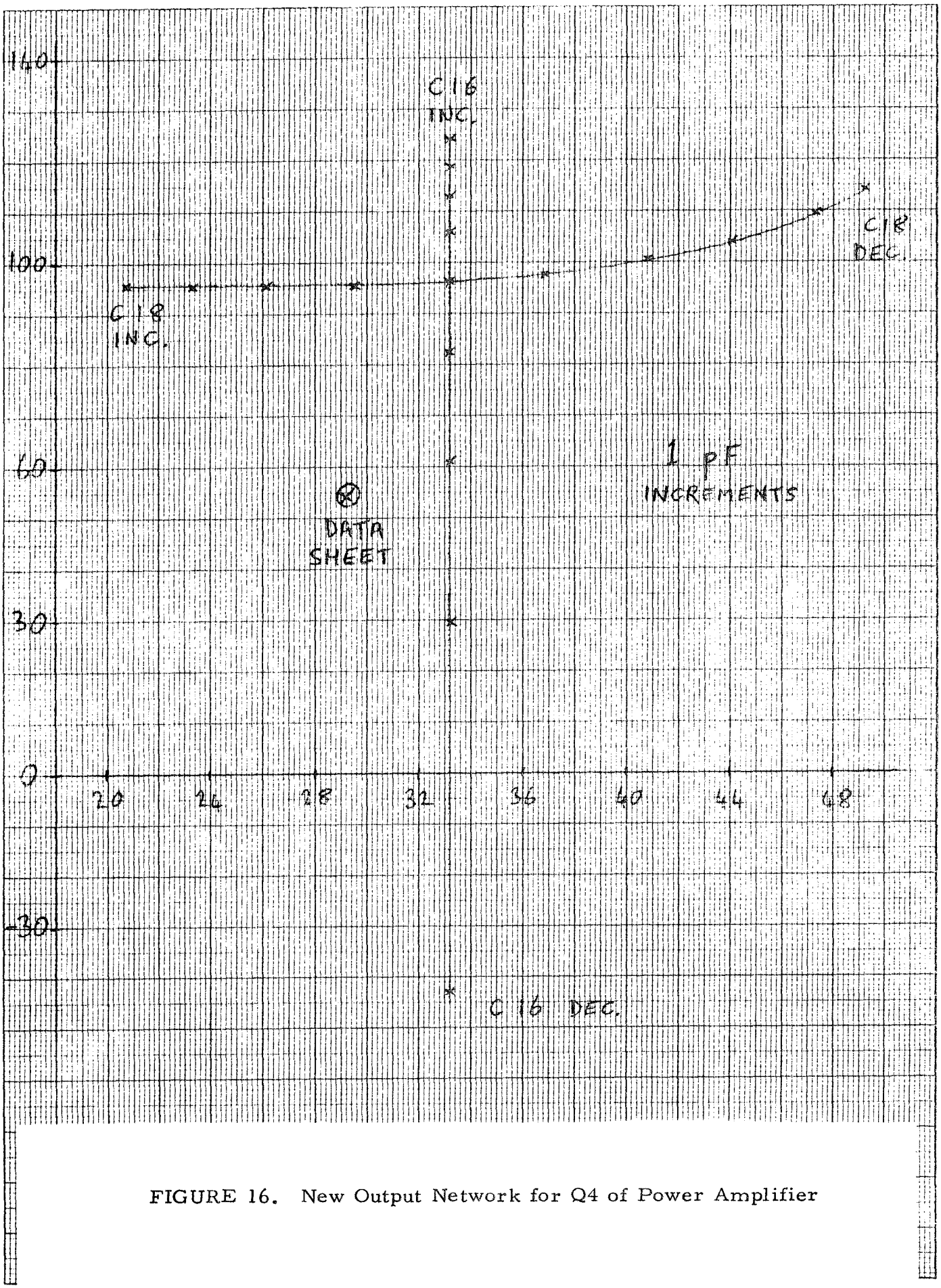


FIGURE 16. New Output Network for Q4 of Power Amplifier

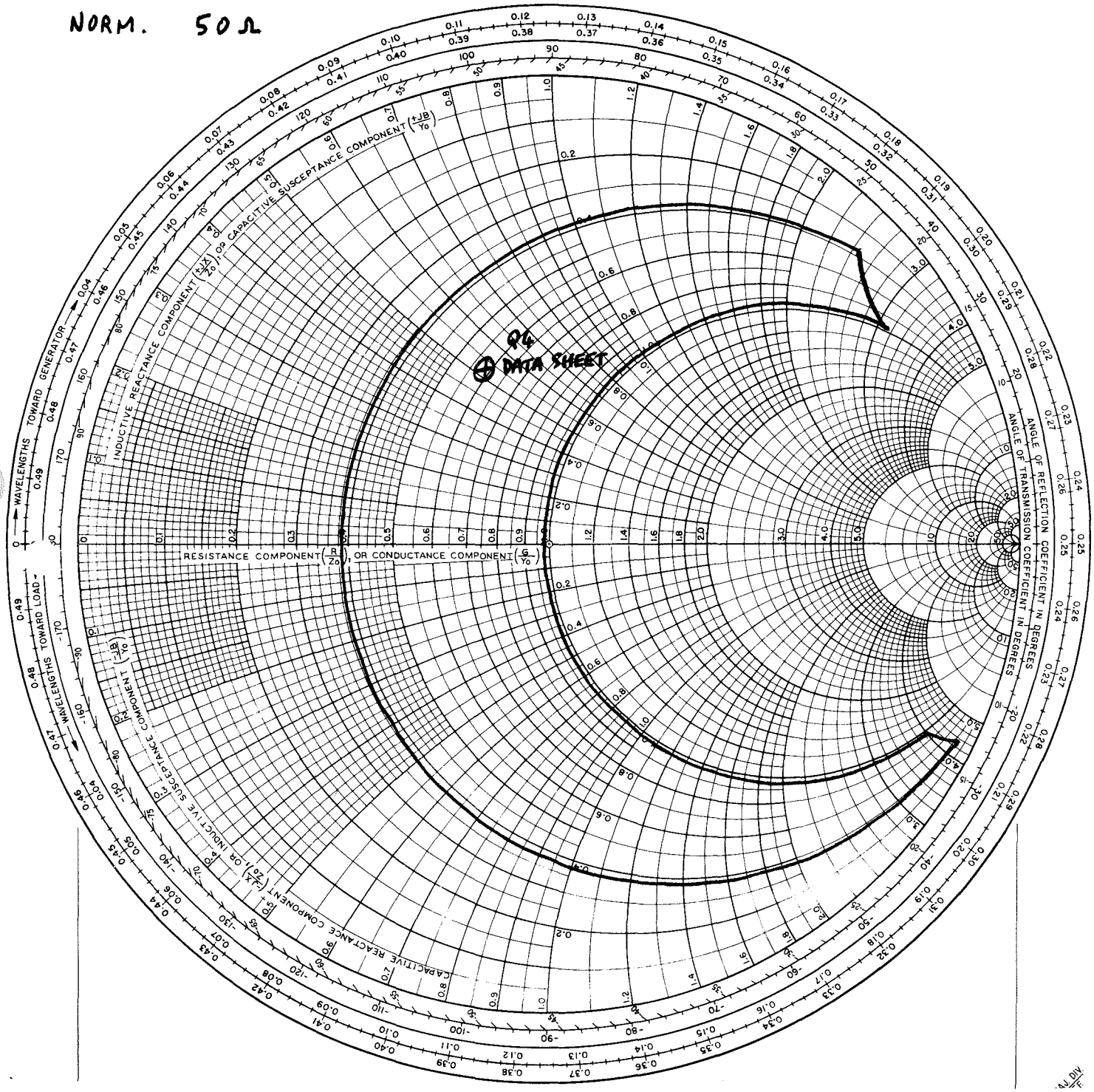


FIGURE 17. Impedance Chart for New Q4 Output Network of Power Amplifier

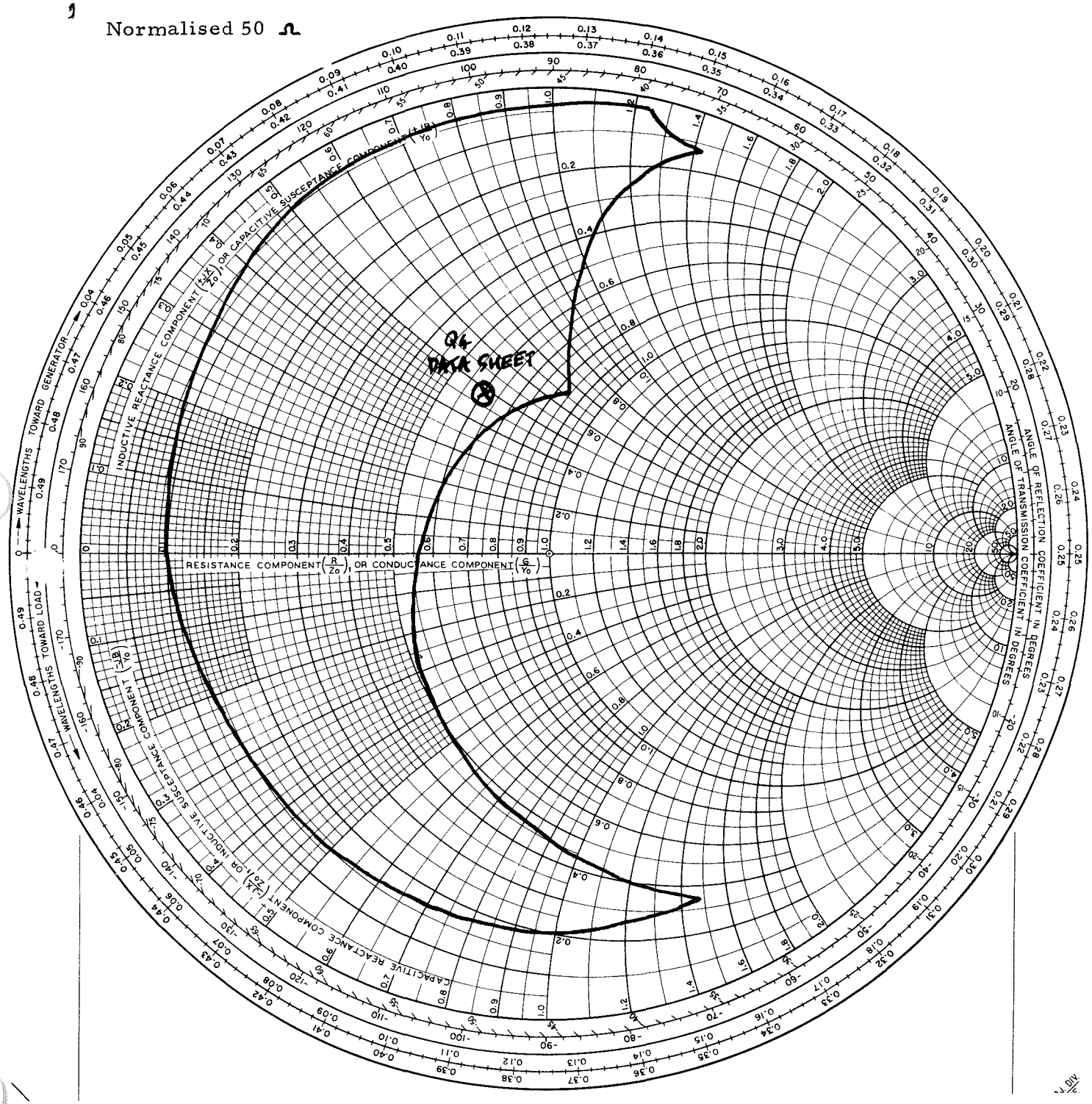


FIGURE 18. Impedance Chart for Old Q4 Output Network of Power Amplifier

The following derivation is similar to one presented in the Motorola Application Note, AN-282[1]:

For a 3 watt output at 380 MHz:

$$R_p = \frac{V_{cc}^2}{2P} = \frac{29^2}{6} = 140\,\Omega$$

From Figure 9, the parallel C_{out} = 6 pF - j 70 Ω

For the series case

$$R_s = \frac{140}{1 + (\frac{140}{70})^2} = 28\,\Omega$$

$$X_s = -28 \times \frac{140}{70} = -j\,56\,\Omega$$

Therefore the equivalent series output impedance is 28 - j 56 ohms.

---

[1] Hejhall; Ibid.

7. APPENDIX

7.1 SAMPLE CALCULATIONS FOR POWER GAIN

The Linvill method of calculation requires a means of determining power gains for terminations other than L = 1, M = 0. Using a Standard Smith Chart it is possible to plot the termination points corresponding to $Y_L + h_{22}$ for each transistor. This gives the termination points shown on Figures 6 to 9 from which the power gain may be estimated by visualizing a power-output function paraboloid intersected by the power-input plane function. Other than for L = 1, M = 0 it is not immediately obvious what the actual values of power gain are. However, a set of contour maps are available which plot the output-power paraboloid over the complete chart, and as may be expected, these contours are concentric circles. Using such a map (Figure 19) it is possible to calculate a value of P_o as a function of $P_{o(o)}$ by comparison of the contour map with the relevant Smith-Linvill Chart. Thus for the transistor Q1 of the power amplifier (Section 5.4.2.1), where $P_{o(o)} = 275$, the termination point is plotted both on the Smith chart and the corresponding point of the contour map. Notice that the circles are to different scales, but the distances of the termination points from the centers are the same fraction of their respective radii, so equivalence is established.

The point of operation of the power input function is simpler to determine since this is simply a plane of known gradient. For the same transistor as before, Q1 of the power amplifier, the input power gradient is 10 at an angle of 176° to the L axis. Also the value of input power at L = 1, M = 0 is $P_{i(o)} = 13.8$. So to calculate a value of power in at any other point it is necessary to measure back a distance x from L = 1, M = 0 along the gradient of input power to the termination point, (x is a fraction of the circle radius). The input power is then $P_{i(o)} = Gr = 13.8 - 0.42(10) = 9.6$. For a given termination it is also possible to determine the input impedance from the same Linvill model, using another set of charts (Figure 20).

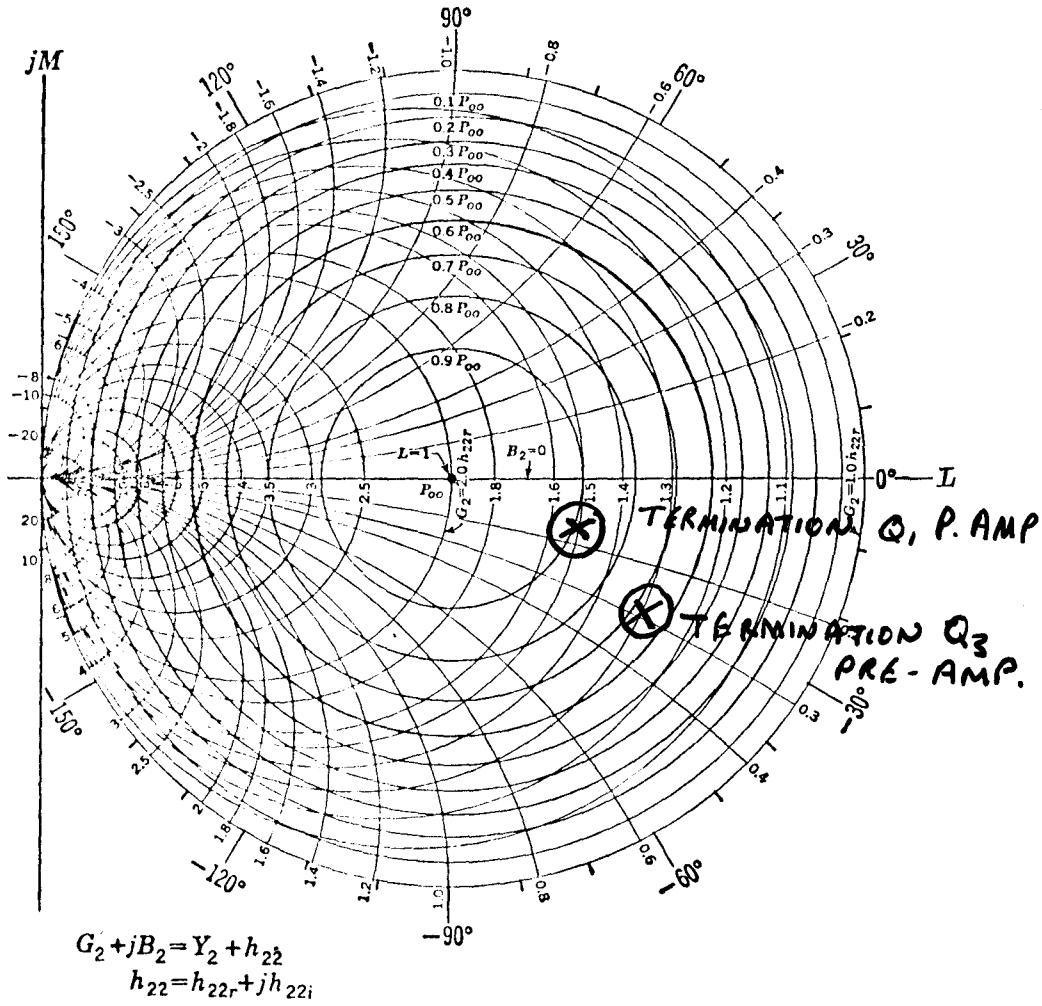
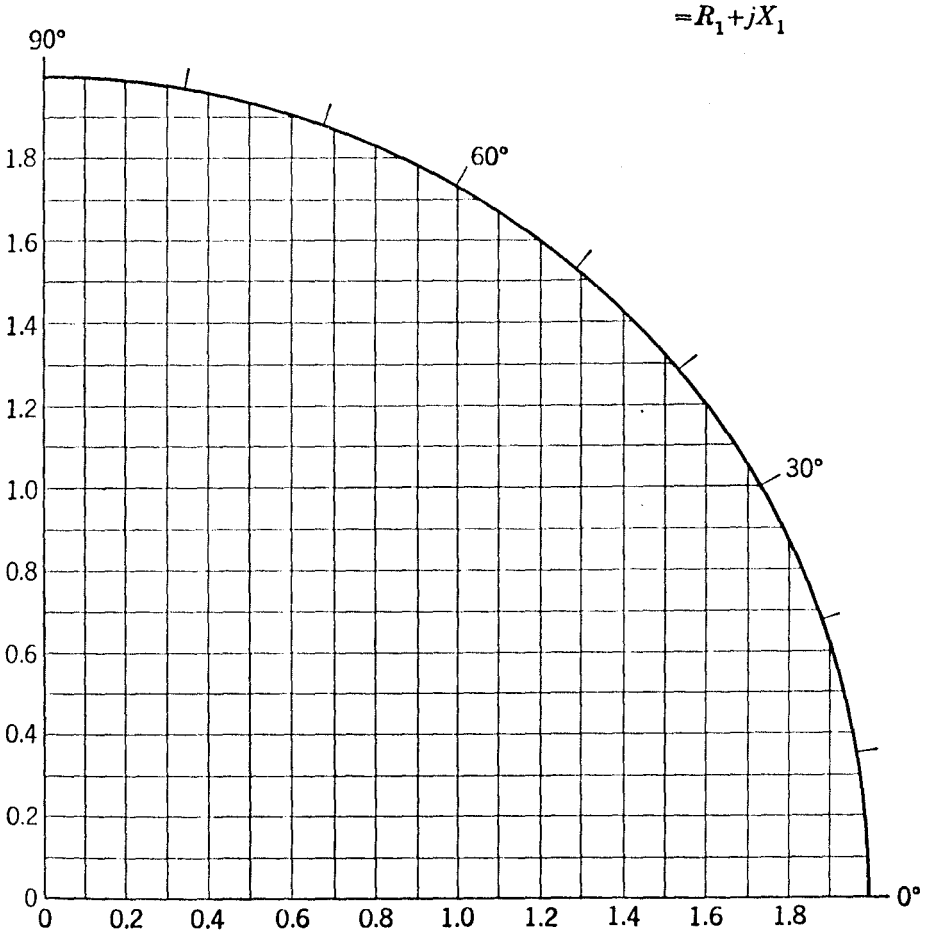


FIGURE 19. Set of Power-Output Contours for Power-Output Paraboloid, Shown Superimposed Over the Smith Linvill Graphs for the 2N3866.

$$\frac{X_1}{\left|\frac{h_{12}h_{21}}{2h_{22r}}\right|}$$

$$Z_{in}-h_{11}=-\frac{h_{12}h_{21}}{2h_{22r}}(L+jM)$$

$$=R_1+jX_1$$



$$\frac{R_1}{\left|\frac{h_{12}h_{21}}{2h_{22r}}\right|}$$

FIGURE 20. Input-Impedance Contour Matrix Overlay - Single Quadrant

These charts represent contours of constant resistive and reactive components of input impedance, since input impedance is directly related to input power for unity input current.[1] The contours reflect the input-power plane and are as expected, straight lines. The straight lines are at right angles to each other, with the resistive axis in the direction of the input gradient, so the Smith-Linvill chart needs to be superimposed over the input-impedance contour matrix to obtain an input impedance fix point. Only a single quadrant of the contour matrix is shown in Figure 20.

For the transistor Q1 the contour map is shown (Figure 21) where it can be seen that the resistive termination 'R' = -13.7 and jX = 0. The input impedance Z_{in} is then[1] $h_{11} + R + jX = 10.3 - j\,2.5$ ohms.

[1] Linvill, J. G. and J. F. Gibbons; loc sit.

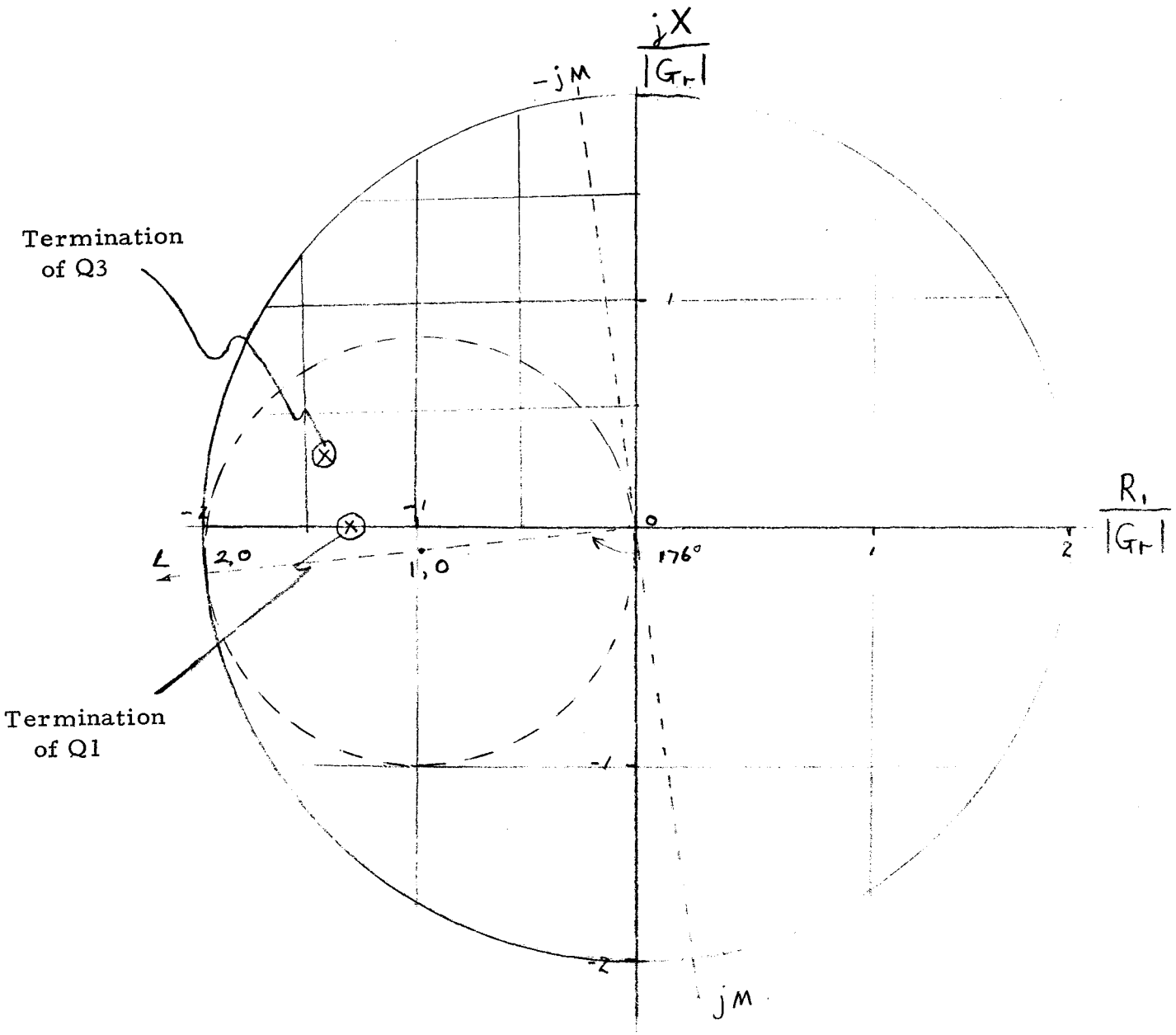
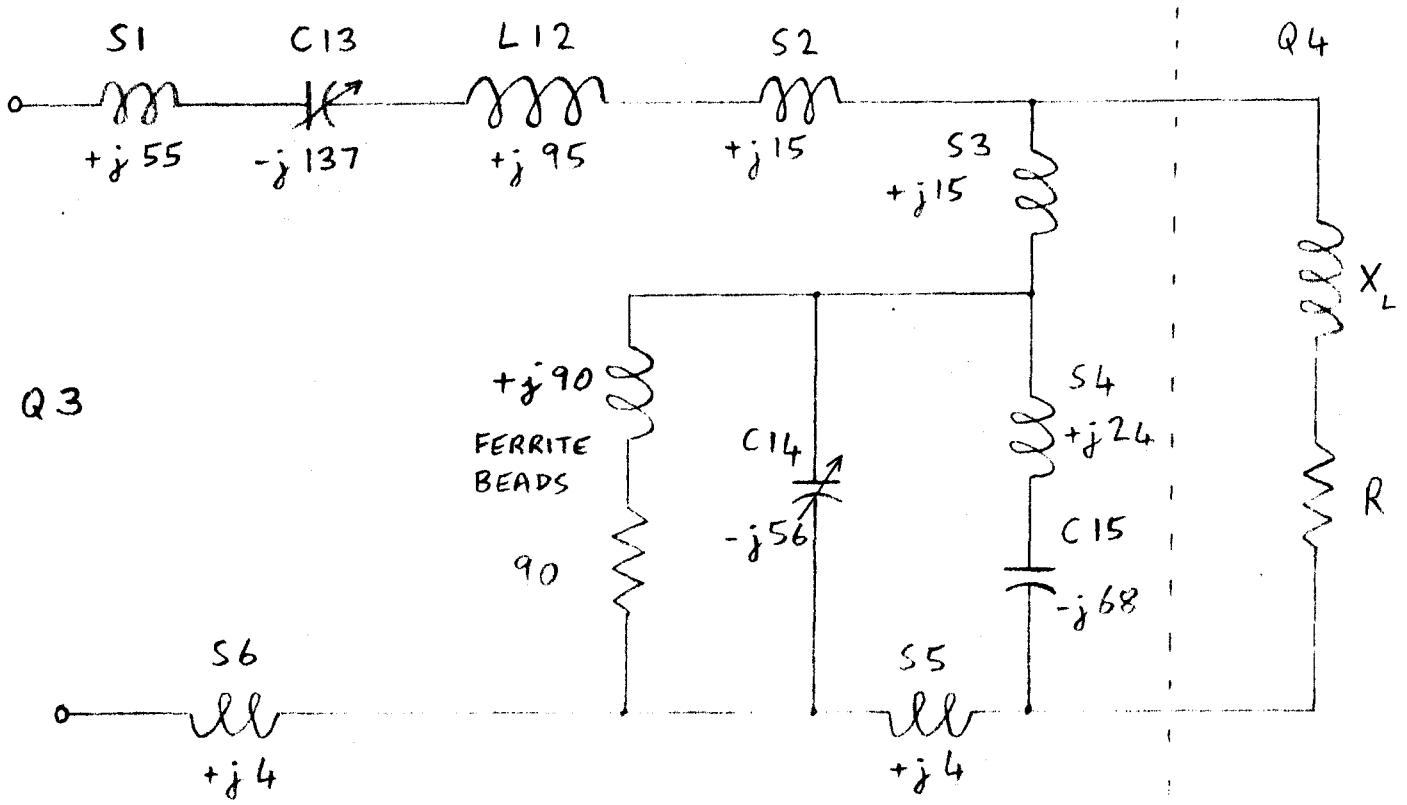


FIGURE 21. Grid in R-X Plane with Corresponding L-M Plane for 2N3866

7.2 Q3-Q4 POWER AMPLIFIER NETWORK RE-CALCULATION

On closer examination of the physical layout of the interstage network between Q3 and Q4 of the power amplifier, the reason for the discrepancy in the calculations (Section 6.2.3) became apparent. This network has been assembled with much longer lead lengths than the other networks, and previous calculations had ignored the effect of lead inductance, which has been calculated to be + j 48 ohms per inch at 380 MHz. The layout is also different in the fact that the base choke of three ferrite beads is soldered to the top of C14, and a length of wire is then connected to the base. The equivalent circuit is:



where the inductances S1 to S6 are those strays caused by the lead lengths and interconnecting wire calculated on a basis of + j 48 ohms per inch.

This circuit can be simplified by a delta-star transformation on the elements around S5, and by summing all the reactances in each branch. The value of input impedance used for Q4 is 4 + j6 ohms, a figure obtained from measurements on a 2N 3375 at 380 MHz and a power output level of three watts. The previous figure used probably was in error since the graphs for the 2N 3375 transistor input impedance have an upper limit of 250 MHz, and the 380 MHz figures were obtained by interpolation.

The equivalent circuit reduces to:

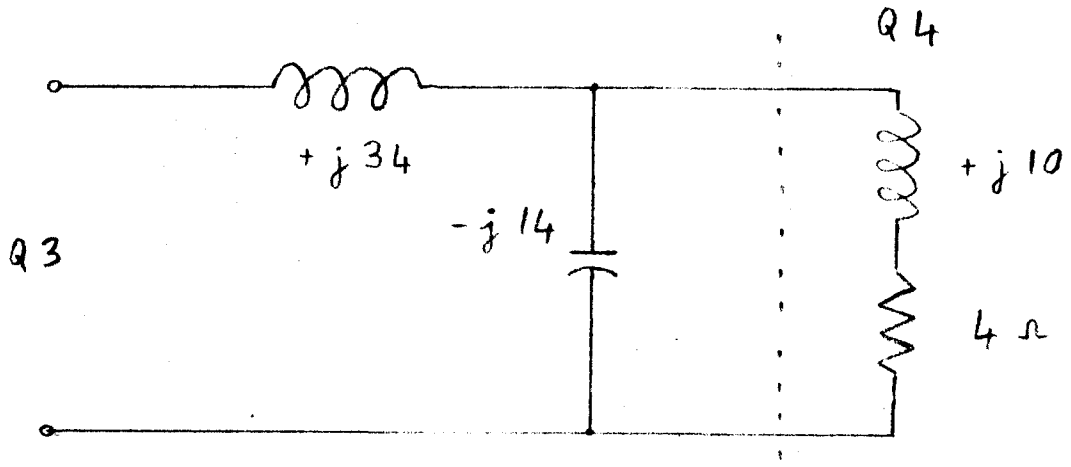


Figure 22 shows the impedance-admittance plot for the network with values of 3 pF for C13, and 7 pF for C14. This figure now shows a value of 18 + j47 ohms for the load impedance presented by the network. This is a distinct improvement on the original figure of 2-j38 ohms, the load now having the correct reactive sign, and the right order of magnitude of the real part.

This shows the variation possible by considering all stray inductances within the layout. The approach used should not be required on the other interstage networks, since lead inductance has more of an effect in the 380 MHz circuitry, and all of the remaining networks have shorter lead lengths.

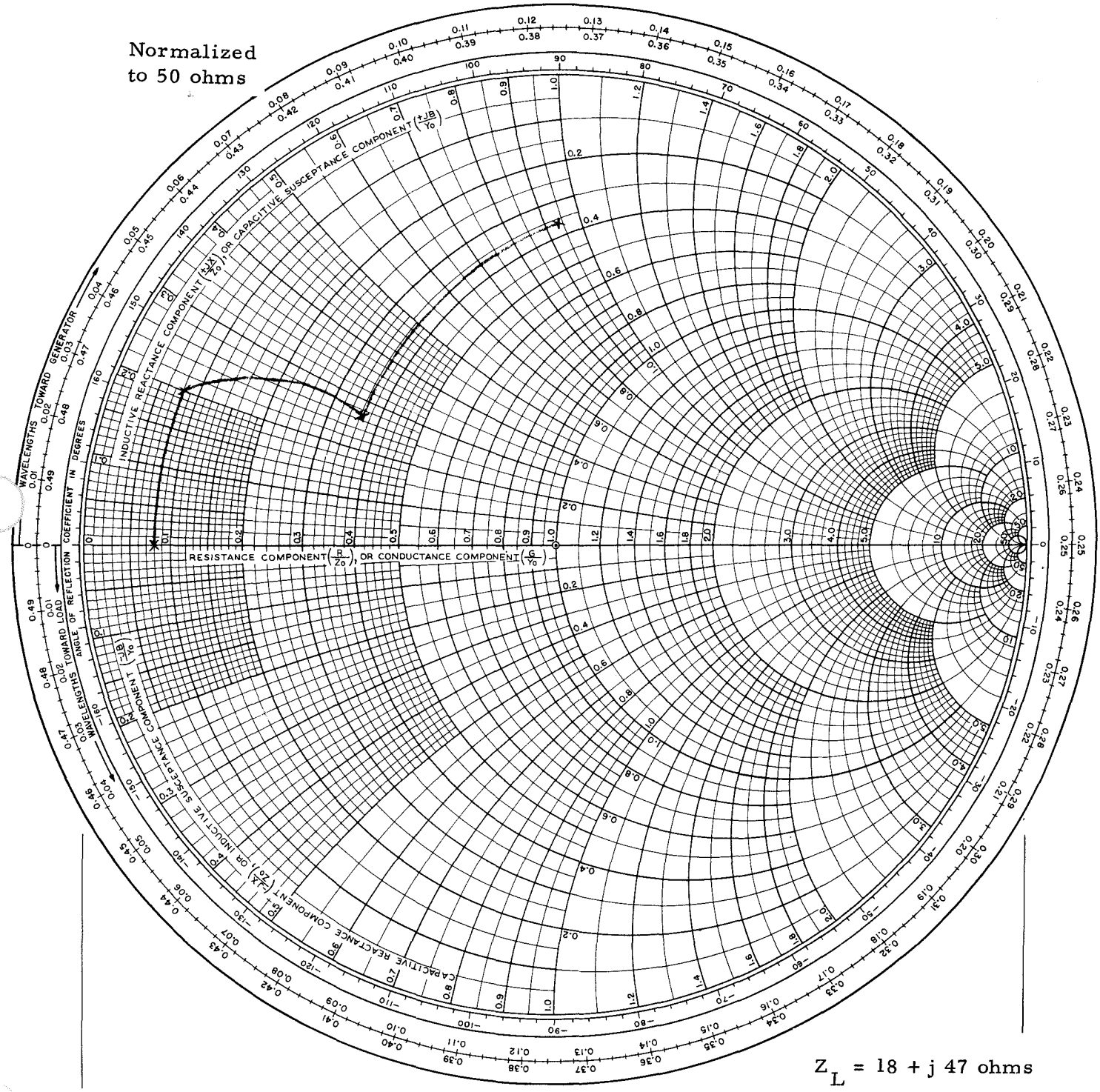


FIGURE 22. Impedance Chart for Corrected Q3 - Q4 Network of Power Amplifier

7.3 POWER AMPLIFIER - STAGES 3 AND 4

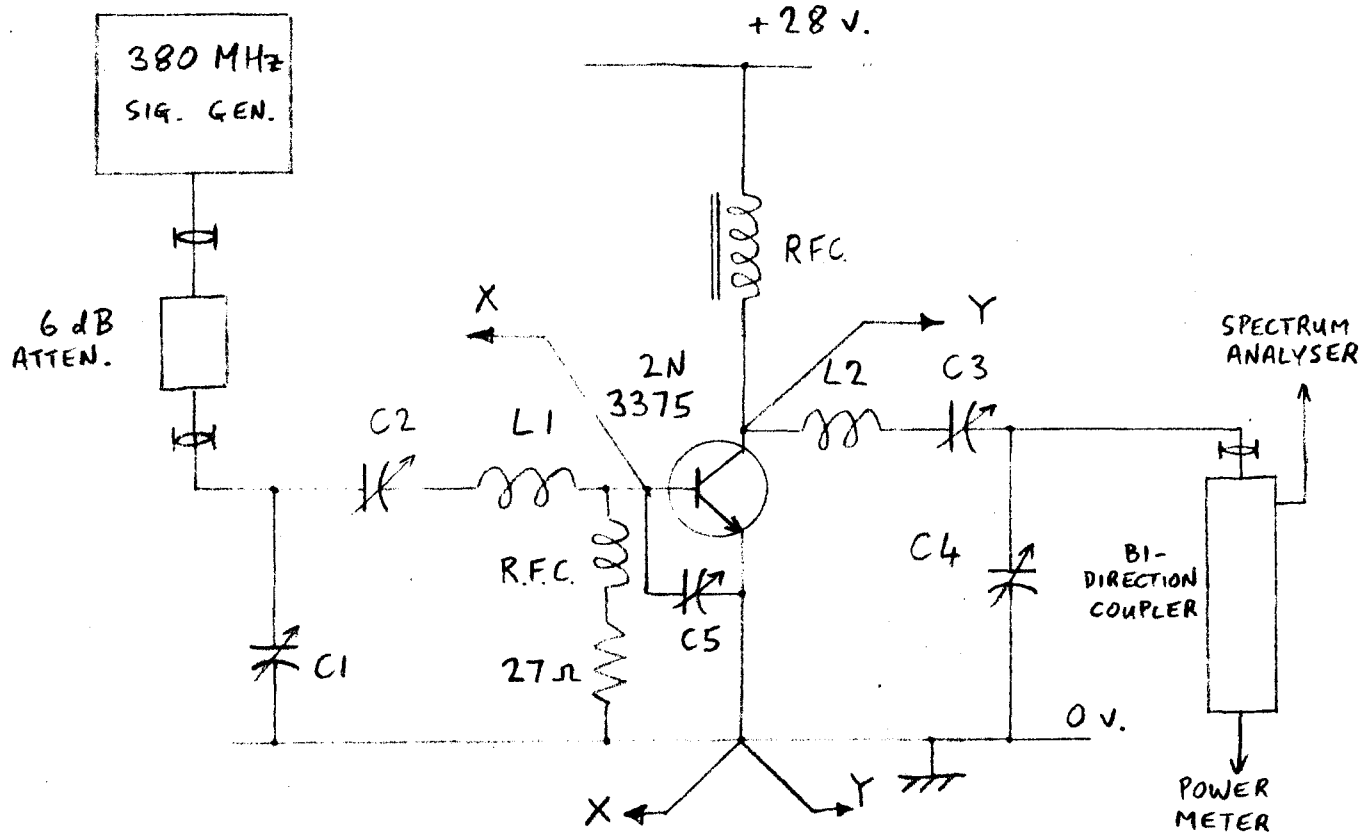
To correctly analyze these stages, large signal transistor parameters are necessary. These are not available from the manufacturer so measurements were made on a 2N3375 at the operating signal power levels. Since the transistors are operating in class C, large signal, time averaged values of 'H' parameters are required. A large 'H' is used to distinguish large signal values from small signal 'h' values. The 'H' values were obtained from a knowledge of input and output impedence (Z in and Z out) and the forward and reverse transfer ratios (H_{12}, H_{21}). Section 7.3.2 describes how Z in and Z out were obtained experimentally and section 7.3.1 describes the means of estimating H_{21} and H_{12} from the available data sheet on the 2N3375.

7.3.1 Estimation of H_{12} and H_{21}

These values were estimated in a similar way to h_{12} and h_{21} for small signals (Section 5.2.1), where $H_{21} = -j\frac{f}{380.10^6}$; and $H_{12} = \frac{H11}{jX_f}$. This approach was adopted for the following reasons: H_{12} is not made dependent as is Z_{in} and Z_{out}, instead H_{21} simply defines the ratio of output current to input current during the conduction period, and being a ratio is not dependent on conduction angle; similarly H_{12} is a function of the feedback capacitance C_{BC} which is assumed constant, and H_{11} which is determined in section 7.3.3.

7.3.2 Measurement of Z_{in} and Z_{out}

The following circuit was used to determine the input and output impedance of a 2N3375 under operating conditions similar to Q3 and Q4 of the power amplifier.



The transistor under test was a randomly selected 2N3375. The bi-directional coupler enabled a spectrum analyzer and power meter to monitor the output. The transistor was tuned for maximum power gain with variable capacitors C1 to C5 so that a conjugate match could be achieved at both input and output. Notice that the capacitor C5 is is connected directly across the base to emitter terminals of the transistor to achieve maximum gain. The full reason for needing this is discussed later in section 7.3.5.

Using a vector voltmeter, the conjugate impedances were measured as shown in directions X and Y.

The test results are as follows:

TRANSISTOR 2N3375

Power In	Power Out	Gain	Ic	Efficiency η	Z_{in}	Z_{out}
dBm	dBm	dB	mA	%	ohms	ohms
24	29	5	70	40	8+j 10	15-j46
29	34.8	5.8	175	62	4+j6	16-j52

7.3.3 Calculation of H_{11} and H_{22}

Using the following expressions it is possible to calculate H_{11} and H_{22} from a knowledge of Z_{in} and Y_o: [1]

$$Z_{in} = H_{11} - \frac{H_{12} H_{21}}{Y_L + H_{22}} \quad \ldots A$$

$$Y_o = H_{22} - \frac{H_{12} H_{21}}{H_{11} + Z_s} \quad \ldots B$$

Assuming: $H_{12} = \frac{H_{11}}{-jX_f}$ and X_f from data sheets = -j 93 Ω

H_{21} = -j 1.3 (Q3) and -j 1.2 (Q4), since from data sheets f_T (Ic = 75 mA) = 500 MHz and

f_T (Ic = 175 mA) = 460 MHz.

$$Y_L = Y_o^*$$

$$Z_{in} = Z_s^*$$

1. Linvill, J. G. and Gibbons, J. F. ; Transistors and Active Circuits, Page 245.

Using this information equations A and B reduce to the following form:

$$Z_{in} = H_{11} - \frac{H_{21}}{(-j93)(Y_o^* + H_{22})} \quad \ldots C$$

$$Y_o = H_{22} - \frac{H_{11} H_{21}}{(-j93)(H_{11} + Z_{in}^*)} \quad \ldots D$$

Equations C and D are two simultaneous equations with two unknowns H_{11} and H_{22}. Z_{in} and Y_o are known from measurements. An iterative method of solving equations C and D was employed by substitution of the small-signal values as a first solution. A computer terminal was employed to reduce the arithmetic involved and the solutions of H_{11} and H_{22} rapidly converged to the following values:

Transistor	Power In	Power Out	P Gain	H_{11}	H_{22}	f_T
	dBm	dBm	dB	ohms	mmhos	MHz
Q3	24	29	5	22+j25	18+j25	500
Q4	29	34.8	5.8	10.7+j96	17.4+j26	460

7.3.4 Linvill Analysis for Q3

Using the H values calculated above it is possible to generate a Linvill model as follows.

$$H_{11} = 22 + j16$$

$$H_{22} = 18 + j25$$

$$H_{21} = -j\,1.3$$

$$H_{12} = -0.17 + j\,0.24$$

Figure 23 shows the relevant Smith-Linvill Chart.

Peak of power output function = $\frac{H_{21}^2}{4H_{22r}}$ = 23.5

At which power-input function = $P_{i(o)}$ = 2.13

Slope of power-input function = $G_r = \left|\frac{H_{12}\,H_{21}}{2H_{22r}}\right|$ = 10.6

Angle of G_r with L-axis θ = arg $(-H_{12}\,H_{21})$ = 145°

$C = 2\,\frac{P_{o\,(o)}}{P_{i\,(o)}}\,\frac{L_{12}}{L_{21}}$ = 0.79

which 'd', the distance of termination for maximum power gain from L=1, M=O along power-input gradient, is $\frac{1-\sqrt{1-C^2}}{C}$ = 0.5

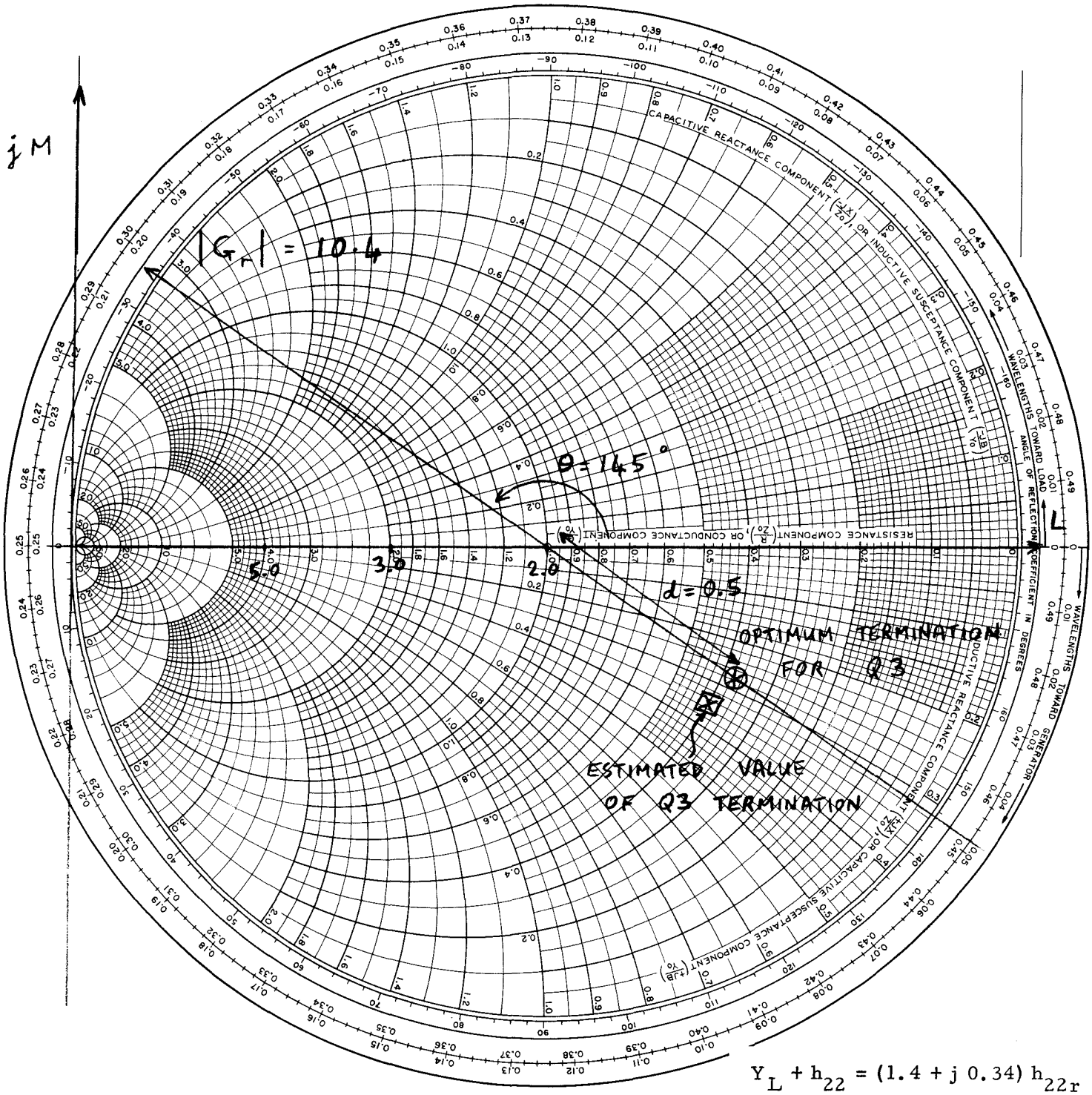
At which point, power gain = $\frac{0.75\,P_{o\,(o)}}{P_{i(o)} - 0.5\,(G_r)}$

= 3.5 dB

It will be noticed that the gain predicted from the above Linvill analysis is only 3.5 dB, whereas 5 dB was obtained from power measurements. Although the limited accuracy of the Linvill analysis with the particular H values employed may be responsible for most, or all, of the discrepancy, it is interesting to notice the effect of changing certain parameters. The value of H_{21} used in the foregoing calculations was -j 1.3 which is predicted from a f_τ of 500 MHz. A change in f_τ to 530 MHz brings H_{21} up to -j 1.4, which when substituted in the above Linvill Analysis gives a predicted power gain of 4.2 dB. 'f_τ' data is not available for the particular transistors used, excepting for the data-sheet information applicable to a commercial 2N3375, which gives f_τ = 500 MHz at Ic = 75 mA (Q3) and f_τ = 460 MHz at Ic = 175 mA (Q4). Similarly the feedback capacitor C_{BC} can only be estimated to a first order approximation from the data given in the data sheets. From the data sheets the output capacitance is stated to be 9 pF at 380 MHz, of which half may reasonably be attributed to C_{BC} and half to C_{BE}.[1] This gives -j93 ohms as the feedback impedance.

In short, given a 1 pF change in the capacitance and an f_τ of 530 MHz, the gain would equal the maximum achieved in the power measurements. A selection process on Q3 and/or Q4, to find above average transistors would appear to be necessary to achieve full gain.

1. RCA Review, June 1965, Generation of Microwave Power, Page 303.

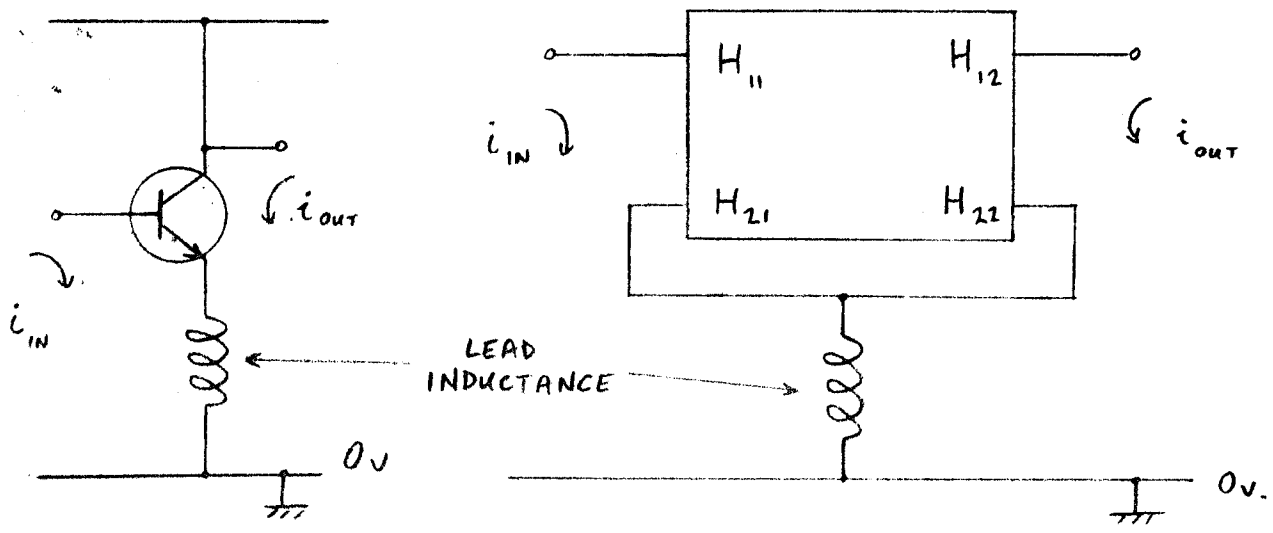


$$Y_L + h_{22} = (1.4 + j\,0.34)\,h_{22r}$$

FIGURE 23. Smith-Linvill Chart for Q3 Power Amplifier (2N3375 Common Emitter)

7.3.5 Effect of Emitter-Lead Inductance

It is very interesting to calculate the effect of taking the capacitors C7 and C12 to chassis ground, rather than to the emitter terminal of Q3 as in the power amplifier. It was found in the impedance measurements (Section 7.3.2) that it was necessary to connect a tuning capacitor directly to the emitter and base terminals to realize full power gain. This is due to the small lead inductance associated with the strap connecting the emitter to ground. Although this inductance can be tuned out, it is part of both the input and output circuit and changes the transistor's parameters.



This means that the 'H' parameters must be modified to include the inductance. The new set of parameters are:

$$H_{11}' = 22 + j16 + jX_L$$

$$H_{12}' = \frac{22 + j16 + jX_L}{-j13}$$

$$H_{21}' = -j13$$

$$H_{22}' = (18 + X_L) + j25$$

where jX_L is the reactance of the emitter lead.

Calculating all the Linvill parameters, it can be shown that as jX_L is increased the maximum power gain is progressively reduced. For X_L = j5 ohms, the maximum gain is reduced by 2 dB, and for X_L = j10 ohms, the maximum gain is down by 5 dB. It would seem that the model considered for Q3 would yield no power gain for X_L = 8 ohms. It is reasonable to assume jX_L to be at least + j5 ohms, so it becomes apparent why it is so necessary to connect the input tuning circuit as close to the emitter terminal as possible.

7.3.6 Power Amplification Stage Q4

Assuming a value of f_T given in the data sheets for the 2N3375 of 460 MHz, the following Linvill analysis was developed.

$$H_{11} = 10.7 + j9.6$$
$$H_{22} = 17.4 + j26 \quad \left.\right\} \text{Section 7.3.3}$$
$$H_{21} = -j1.2 \quad (f_T = 460 \text{ MHz})$$
$$H_{12} = \frac{H_{11}}{-j93} = 0.10 + j0.11$$

The maximum point of the power-output function = $P_{o(o)}$

$$\text{where } P_{o(o)} = \frac{H_{21}^2}{4H_{22r}} = 20.7$$

At which point the input-power function = $P_{i(o)}$

$$\text{where } P_{i(o)} = [2(H_{11r})(H_{22r}) - \text{Re}(H_{21})(H_{12})]\frac{1}{2H_{22r}}$$

$$\text{gives } P_{i(o)} = 6.5$$

Also, the gradient of the input power function = $G_{(r)}$

$$\text{where } G_r = \frac{H_{12}H_{21}}{2H_{22r}} = 5.2$$

The angle made by G_r with the L-axis = θ

$$\text{where } \theta = -\arg(-H_{12}H_{21}) = 140^\circ$$

The critical factor C = 0.81, which gives 'd' the distance from the center of the LM plane along which maximum power occurs = 0.5.

Using the power overlay charts (Appendix 7.1) the maximum power gain is 3.8 = 5.8 dB. The optimum termination point is shown in Figure 24, the Smith-Linvill chart for this transistor.

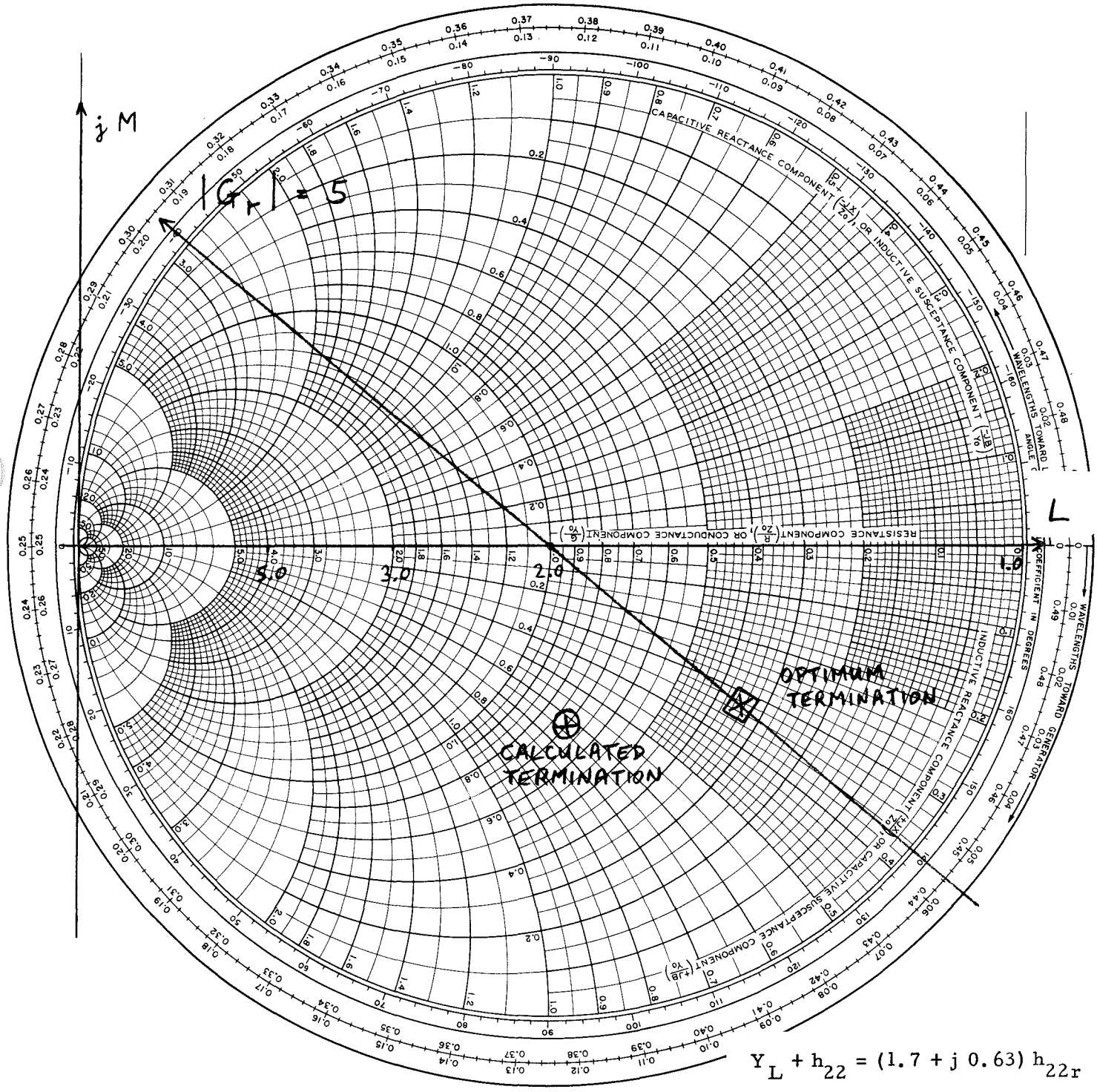
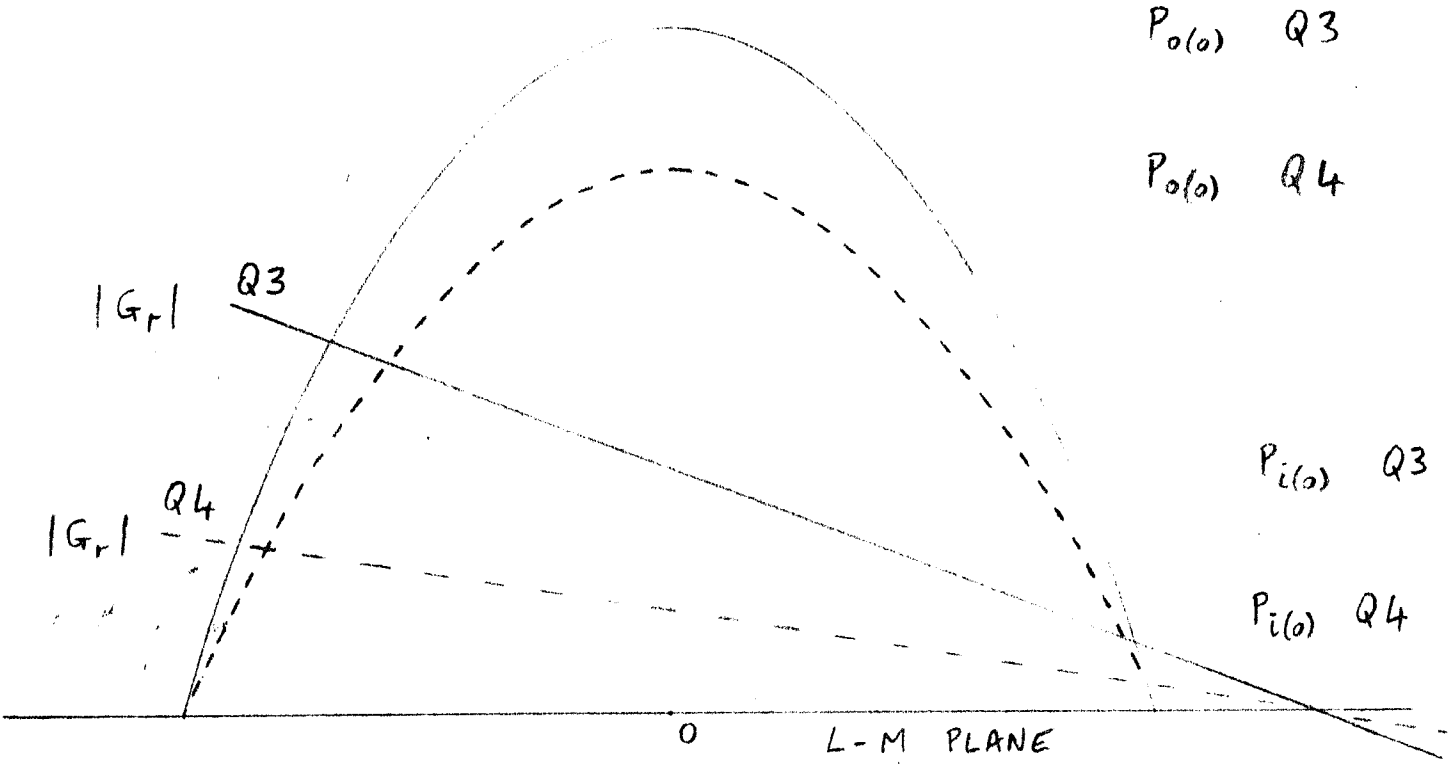


FIGURE 24. Smith-Linvill Chart for Q4 of Power Amplifier.

It will be noticed that for Q4, the power input plane has halved its slope, whereas the power-output parabaloid is only 20% reduced in height. This consequently gives increased gain for the higher power-level. A comparative pair of sections through the gradient of input power and L = 1, M = O are superimposed below:



It will be noticed that over the power-output levels considered (1 watt to 3 watts) the transistors Q3 and Q4 are unconditionally stable, since the power-input function cuts the LM base plane outside the paraboloid. This shows that the power gain obtained is the maximum that can be obtained from two 2N3375 transistors at these frequencies.

7.4 Q4 OUTPUT NETWORK RE-CALCULATION

This output network was re-calculated when the average capacitor settings of 1.5 pF for C16 and 6 pF for C18 gave a capacitative load for Q4. It was decided that the value of reactance of 190 ohms taken for the coil L15 (0.08 μ H) was in error due to the self-capacitance present in this four turn coil, the largest in all of the 380 MHz circuitry. Since no equipment was available to measure the effective inductance at 380 MHz, a plot was made of capacity required for resonance versus $1/\text{freq.}^2$ to find the effect of self-capacitance.[1]

This curve was plotted at frequencies from 80 to 250 MHz using a Boonton RX bridge, and by interpolating to 380 MHz, an effective reactance of +j350 ohms was calculated. (See Figure 25). Using this value for L15, and the average values quoted for C16 and C18, a impedance - admittance chart was plotted and is shown in Figure 26. This gives a value of 33 +j40 ohms for the load impedance for Q4. It is possible that this figure will not correspond to the optimum since this is one of the networks that is deliberately detuned to lose excess power gain.

[1] Radiotron Designer's Handbook, RCA Corp., 1953, page 453.

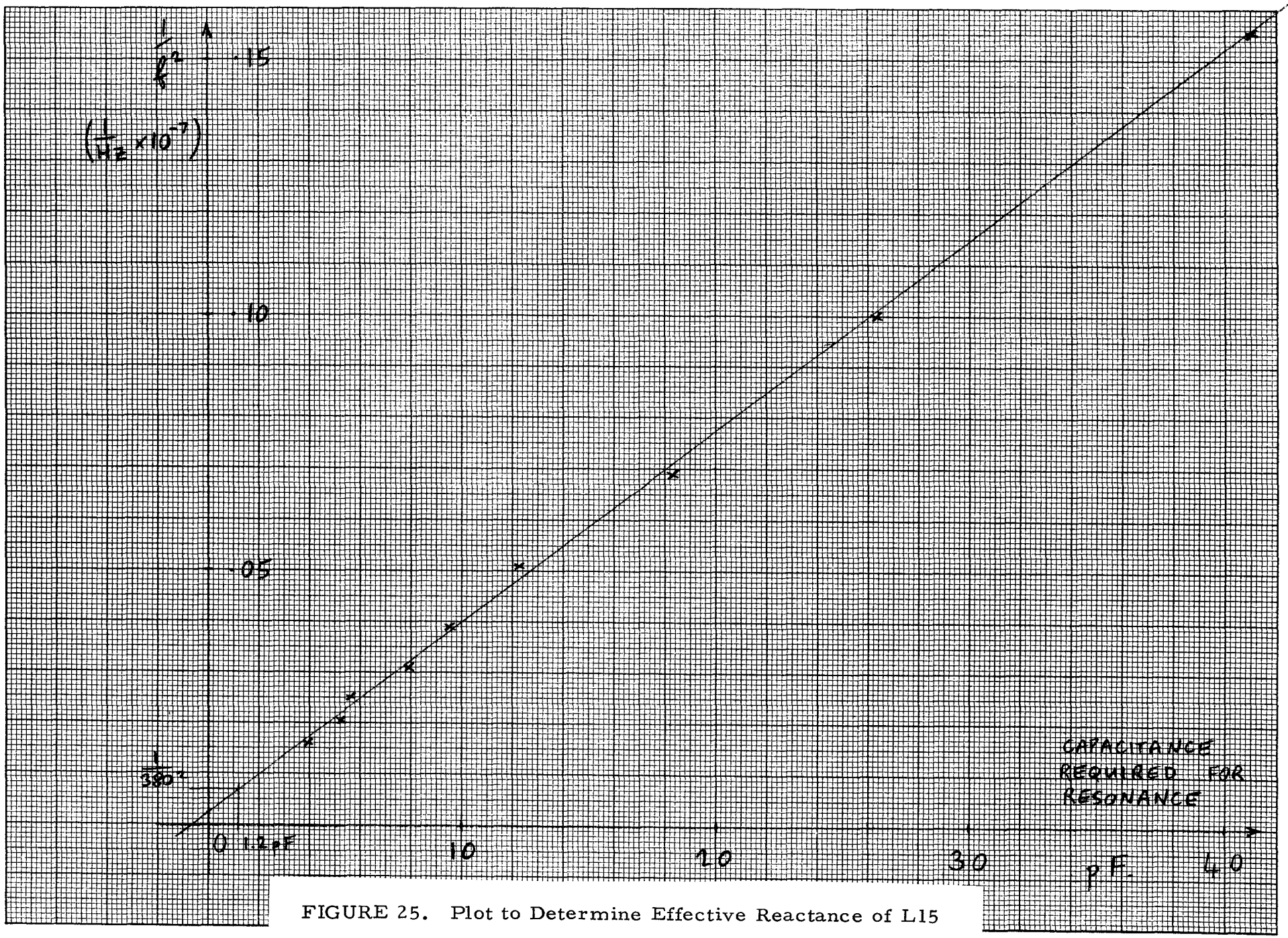
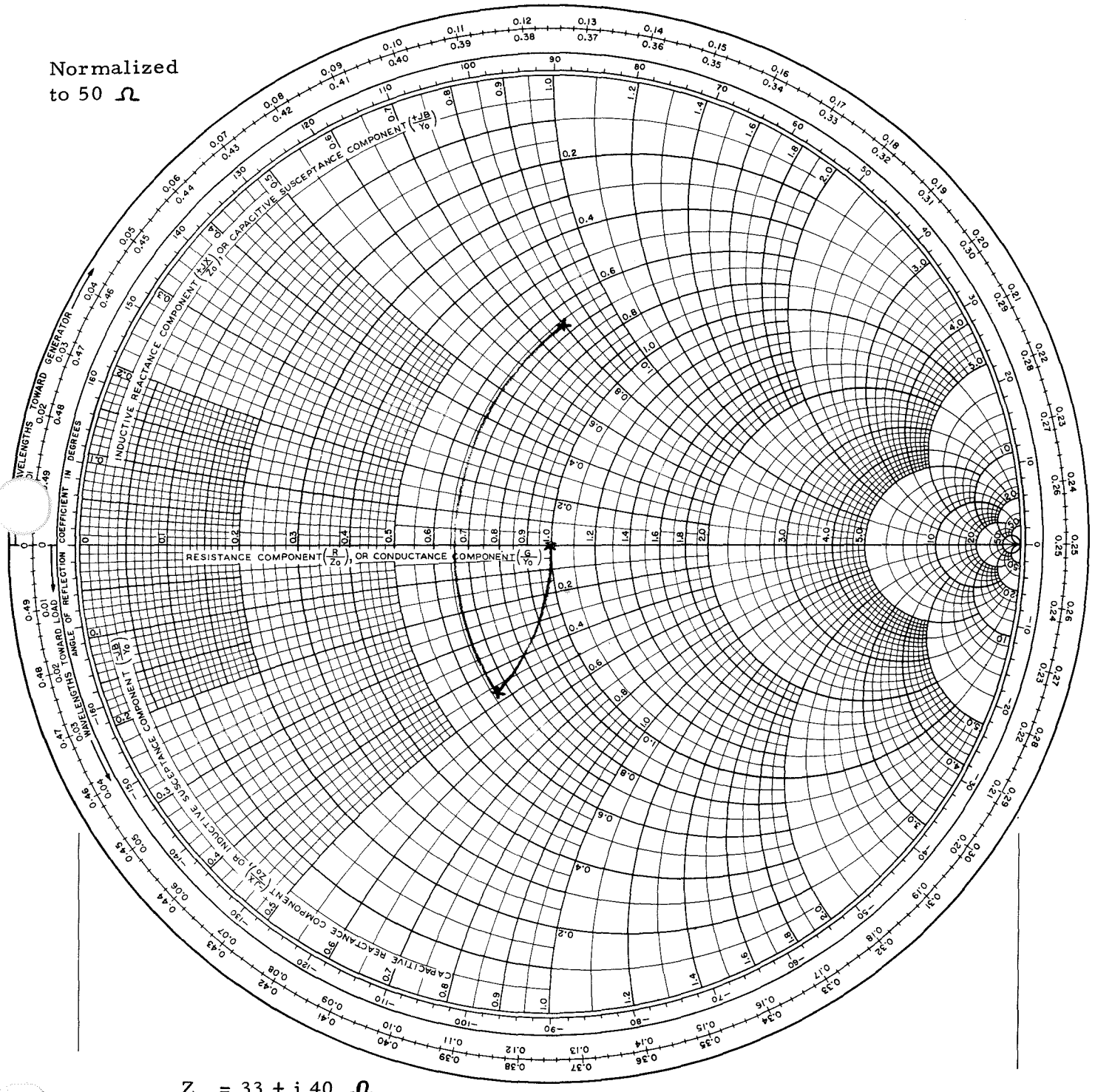


FIGURE 25. Plot to Determine Effective Reactance of L15



$Z_L = 33 + j\,40\ \Omega$

FIGURE 26. Average Load Impedance of Q4 New Output Network of Power Amplifier