Bendix
Aerospace Systems Division

ALSEP Array E
Command Decoder
Breadboard Test Report

NO.	REV. NO.
ATM-985	

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The following ATM has been prepared to document the testing and test results of the command decoder breadboard for Array E.

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Prepared by: V. C Kemp.
V. C. Kemp

Prepared by: G. W. Alexander
G. W. Alexander

Approved by: B C McLeod
B. C. McLeod

List of Diagrams

1.0 DATA DEMODULATOR BOARD (Drawing No. 2349346)

1.1 PHASE LOCK LOOP

1.1.1 Lock and Capture Frequency Ranges

These were measured by injecting a variable amplitude and frequency sine wave at the RXMAP input and monitoring the operational amplifier output at AR 3 pin 7, with an oscilloscope on a suitable d.c. range. As the system comes into lock the output of AR 3 jumps to a d.c. level proportional to the phase difference between the two oscillators. The capture range was measured by approaching the VCO free running frequency from both higher and lower frequencies until phase lock was achieved in less than 2 seconds. The capture range is then the difference between these frequencies. The lock range was measured by taking the system out of lock at frequencies above and below the VCO free running frequency. The lock range is then the difference between these two frequencies.

This was repeated for various amplitudes of the input signal and the results are plotted in Figure 1.

1.1.2 Capture Time

The capture time is defined as the time between applying the data at RXMAP and a permanent threshold signal appearing at U8E output.

This was measured when applying the minimum specified 1 and 2 KHz data stream to the RXMAP input. The VCO free running frequency was varied by a variable resistor in place of R9. The threshold signal was monitored at the output of U8E pin 2.

The data stream was switched manually and a triggerable counter was initiated by the data stream and stopped when the threshold signal appeared. The counter then displayed the time between these two events.

The threshold signal was also used to trigger an oscilloscope to ensure that the counter had been stopped at the leading edge of a permanent threshold signal. This was found necessary since the threshold signal sometimes went high intermittently as the system came into lock. For the larger offset VCO frequencies the oscilloscope reading was used to correct the timer reading, due to the problem of threshold "bounce". The measurement was repeated about 20 times for each value of VCO free running frequency and an average value taken.

The VCO free running frequency was measured for each set of readings by grounding R_9 at the AR 3 end and measuring the frequency at U3B pin 9. These results are plotted in Figure 2.

1.1.3 VCO Frequency

(a) The VCO frequency was measured on a digital frequency counter monitoring U3B pin 9. A variable frequency sine wave was applied to RXMAP input and the d.c. output of operational amplifier AR 3 pin 7 was measured on a D.V.M. The input frequency was varied and the output of AR 3 and the VCO frequency were measured. The results are plotted in Figure 3.

(b) The variation of the VCO free running frequency with temperature was measured, with the phase lock loop open. This was done by disconnecting R4 and R 12 from U 1 and grounding them. The results are plotted in Figure 4.

(c) The variation of the VCO free running frequency with the voltage supplies was measured with the P.LL open as in (b). No change was recorded for the +5 volt and -12 volt lines, but the variation with the +12 volt line is recorded in Figure 5.

1.1.4 The Open Loop Frequency Gain Response of the Loop Filter

This was measured for the initial system with breaks at 0.17, 10.8, 1060 and 1800 Hz. The variable frequency was injected at R_3 and with switch U1 6-5 closed, the output AR3/7 was monitored with an oscilloscope. These results are plotted in Figure 6.

1.1.5 The Closed Loop Frequency Response of the Phase Lock Loop

This was measured with the set up shown in Figure 16. The phase lock loop was broken at AR 3 output and a unity gain operational amplifier was inserted. The op amp enables the closed loop to be perturbed by a variable frequency sine wave. The closed loop transfer function is then given by the ratio of the AR 3 output to the input sine wave disturbance. The gain was measured directly from the magnitudes of the two sine waves on the oscilloscope and the phase measurement was performed by a Lissajous technique on the scope. The closed loop results were reflected through a Nicholls Chart to obtain an open loop Bode plot. The Bode plot is shown in Figure 8, together with the theoretical curves.

1.1.6 P.S R Characteristic

This was measured using the test set up shown in Figure 17. The phase lock loop is broken by disconnecting the switches at U1/2 and U1/3 and disconnecting R 3 at the junction with R 2. A special purpose variable phase sine/square wave oscillator was used together with an inverter to supply synthetic signals to the PSR input and switching lines. The oscillator provided a sine wave output together with a variable phase square wave with a calibrated phase control. The frequency was set at 1 KHz and a set of voltage readings at AR 3/7 was obtained for various sine wave amplitudes and phase differences. The slopes of a family of PSR output volts versus phase shift curves are plotted in Figure 7.

1.1.7 The Static Phase Error of the Phase Lock Loop

This was measured for the maximum and minimum input signal voltage. The measurement was made by injecting a variable sine wave signal at RXMAP and measuring with an oscilloscope the phase difference in μsec between the signals at AR 1/7 and U5 B/9. These results are shown in Figure 9.

1.2 DATA DEMODULATOR

1.2.1 Threshold Response to Noise

The response of the threshold to a noise input was measured using the test set up of Figure 18. The noise was derived from two sources; firstly, a white noise generator followed by a filter amplifier with a

roll off of 200Hz, secondly, a Motorola receiver with no input signal. The noise was injected at RXMAP input. The duration of the false threshold high pulse was measured with the circuit in Figure 18, by gating the threshold with a 1 ms clock in a binary counter. Then the outputs of the binary to decimal converter were monitored with a digital counter. The number of counts N_n' recorded on the nth channel is given by

$$N_n' = N_n - N_{n+1}$$

Where N_n is the number of counts of threshold pulses n milliseconds in duration. Each decimal output channel was monitored one at a time by the counter for a period sufficient to give a meaningful number of samples (about 50). The results are plotted in Figures 10 and 13, for various analog threshold voltages, (measured at the junction of R 28 and R 29, and varied by adjusting R 29).

1.2.2 Threshold Response to Signals and Noise

The response of the threshold circuit to noise was measured by monitoring the NRZ data output, when a noisy baseband signal of all 1's was injected at the RXMAP input. The test circuit is shown in Figure 19. A series of curves of number of false data pulses (when NRZ output indicated a zero) versus signal noise ratio were plotted for various analog threshold voltages and the results are shown in Figure 11.

1.2.3 Minimum Input Voltage Requirements

The data input level was reduced to the data demodulator until the threshold circuit removed the data output. This level was determined for various analog threshold voltages and these results plotted in Figure 12.

1.2.4 Photographs of the Philco and Motorola receiver noise power spectra are shown in Figure 14.

1.2.5 A series of 'scope photos of the demodulator are shown in Figure 15.

(1) Top - One/zero baseband data input
Middle - One/zero data output
Bottom - 2 KHz clock

(2) Top and Middle - PSR outputs in P. L. L.
Bottom - One/zero data output

(3) Top and Middle - PSR outputs in Data Detector
Bottom - One/zero data output

(4) Top and Middle - Comparator inputs in Data Detector
Bottom - One/zero data output

(5) Top - Capacitor Discharge Pulse
Middle - 2 KHz
Bottom - One/zero data output

(6) Top - Uplink Clock (UCK)
Upper Middle - Gate Clock (GCK)
Lower Middle - Parity Clock (PCK)
Bottom - One/zero data output

2.0 TESTING OF LOGIC BOARDS

2.1 DECODE GATE BOARDS

The two decode gate boards where tested with a seven bit input command and command execute pulse provided from a switch panel. Each of the 104 commands were individually tested and found to be the correct command signal for the code inserted.

2.2 CONTROL LOGIC BOARDS

These were tested by using a Bendix SS1100 Signal Simulator, and two external clock sources to simulate uplink and downlink timing. The uplink clock (1 KHz) provided four clock pulse phases, and a clock signal to the SS1100 (Figure 21). The SS1100 has the capability of sending a 21 bit sequence at any repetition rate, with a choice of idle bits in between the sequences. This was used to send the Array E address (octal 151) followed by a command complement and a command. Since this sequence was programmed on individual switches, deliberate address or parity errors could be introduced. The downlink timing simulator produced the CWE clock, shift line (SLIZN) and data demand, all with the correct phase relationship (Figures 22 and 23).

Testing was carried out by providing various commands and checking the events sequence of address recognition, parity checking, command execution, CVW production and reset conditions. Various errors in the address and command complement were introduced, and their effect noted. Commands were sent to switch the command decoder into the LSP data mode, and a check was made on this alternative reset mode.

2.3 INTEGRATION OF DATA DEMODULATOR AND CONTROL LOGIC

The already tested data demodulator board was connected to a control logic board, and the control logic tests repeated with data processed by the demodulator. The data was still generated by the SS1100, but a special test board was constructed to generate a biphase modulated signal (Figure 20). This check assured that all the phases of the data demodulator clock were correct with respect to each other and to the NRZ data generated.

2.4 POWER RESET CIRCUIT

This circuit is used three times in the command decoder, on the command sequencer, and each of the data demodulator boards. The circuit was tested by applying a 10 mS ramp function on the 5 volt logic supply lines, and ensuring that the power reset pulse was negative for a measurable time after V_{cc} had exceeded 4.5 volts. This 4.5 volt figure is the minimum V_{cc} at which Texas Instruments will guarantee that their 54L logic will work. The value of the capacitor C is 1.0μF in the data demodulator circuits, but is 6.8 μF in the command sequencer circuit. This would expand the time scale seven times, and ensure that this circuit would work with a 70 mS V_{cc} rise time.

3.0 TESTING OF BREADBOARD

3.1 BREADBOARD INTEGRATION

All the boards were now inserted into the rack except for the command sequencer, and a check was carried out on every command, with first side A powered, and then side B. This process was then repeated with the command decoder in the LSP reset mode. From this test it was concluded that the method of implementation of redundancy was correct.

3.2 COMMAND SEQUENCER

The command sequencer board was then inserted in the rack, and its functions checked. Firstly, the ripple-off circuit was checked by generating a variable width negative pulse corresponding to the reserve power signal RESZP. This signal was out of phase with any of the other command decoder signals.

Each output was checked for correct timing (Figure 24) and to ensure that a pulse was completed (8 mS long) even if the reserve power signal had returned high during its period. A check was also made to ensure that the system inhibited itself if the input pulse finished after the last command pulse was generated. A separate command or power reset was then required to return the circuit to its active state.

The repeated command sequencer and uplink switch circuit was next tested with a simulated 90th frame mark and a Word Three (Figure 25). The repetition rates were speeded up to cycle in 4 minutes instead of 60 hours. This circuit was then checked at this high repetition rate, and the command OR circuit checked for both A and B sides, and also for the ripple-off commands.

3.3 POWER CONSUMPTION MEASUREMENTS

The whole command decoder breadboard rack was placed in a temperature chamber, and all of the power supply currents measured at 20°C temperature intervals.

The currents taken by the 5 volt supply lines are shown in Figure 27 for nominal, high and low variations of voltage at various temperatures. Figure 28 shows the results for the + and -12 volt lines. No plots are shown for voltage variations of the 12 volt lines since the current variation was less than 100 mV at all points. The 12 volt non-redundant supply was between 40 and 60 μ A on both the positive and negative lines.

3.4 INTEGRATION WITH DATA PROCESSOR

The final test carried out with the command decoder breadboard was that of integration with the data processor. The two units were hooked up with a 3 ft. interface cable, and both units worked well (Figure 29). This was quite a severe test for the logic to drive a 3 ft. line in a noisy environment, but no problems were experienced once a single point ground system was implemented for the power supplies and test equipment. In flight hardware, this length has been designed to be less than 10 inches.

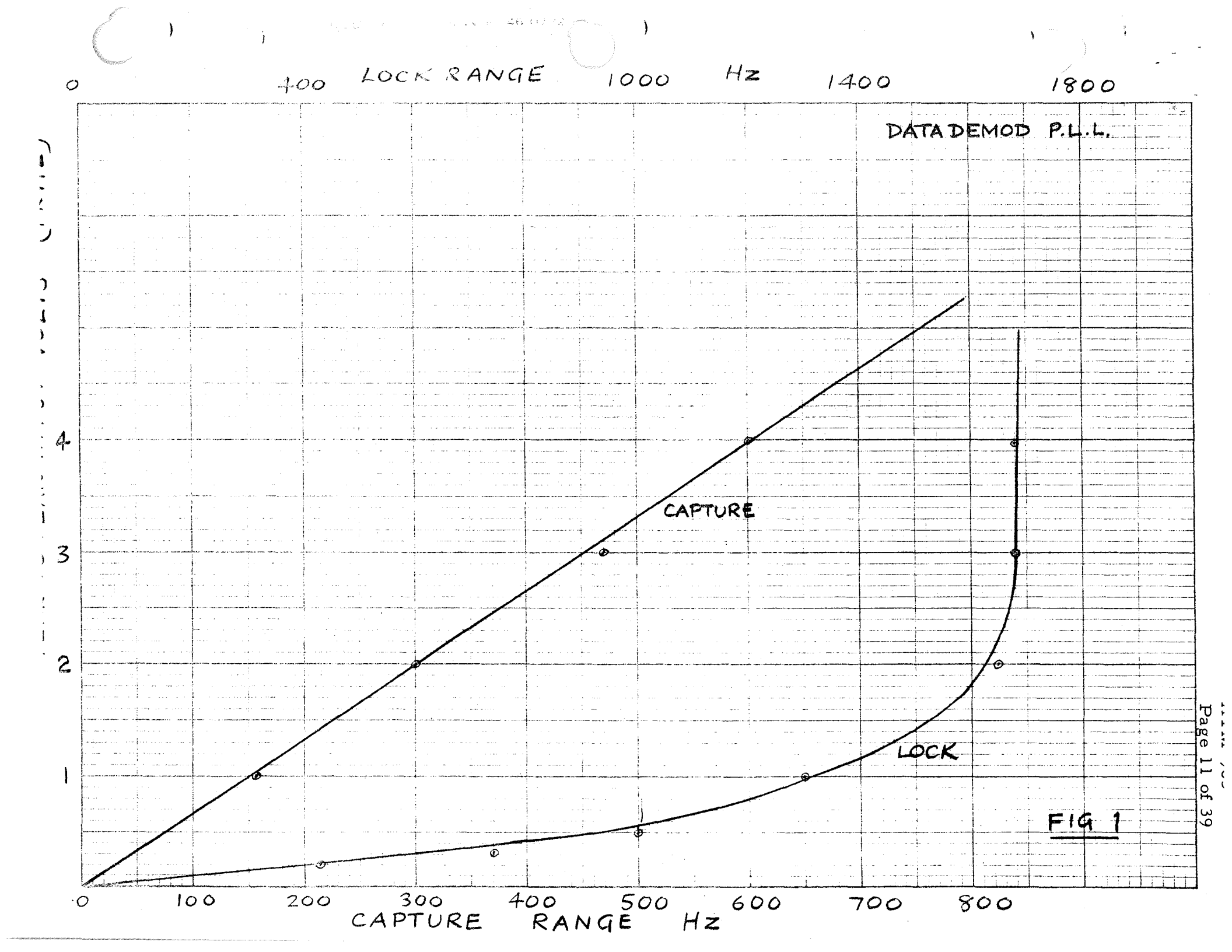

0
400
LOCK RANGE
1000
Hz
1400
1800
DATA DEMOD P.L.L.
4
3
2
1
CAPTURE
LOCK
0
100
200
300
400
500
600
700
800
CAPTURE RANGE Hz

FIG 1

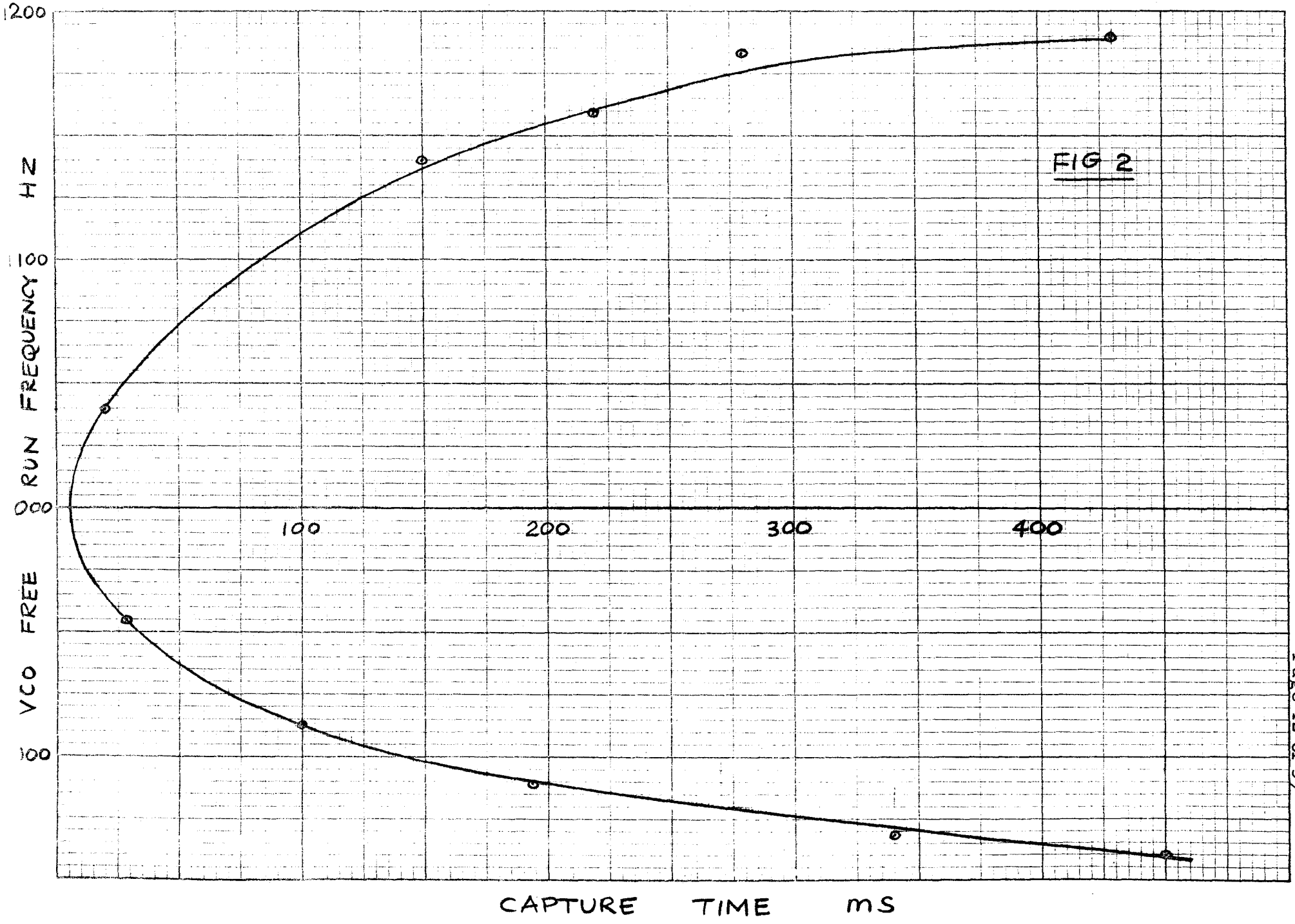
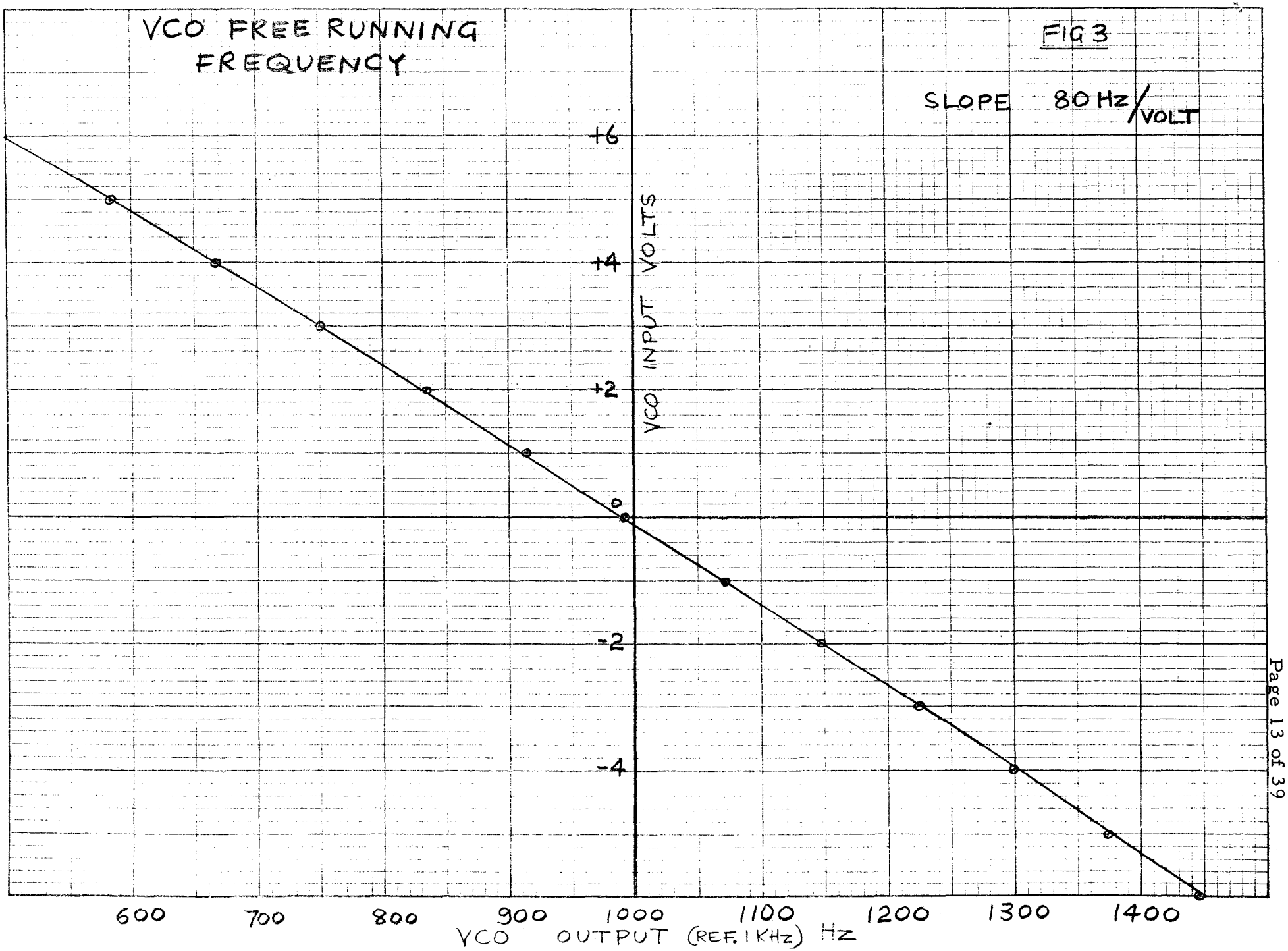

1200
100
000
100
200
300
400
HZ
RUN FREQUENCY
VCO FREE
CAPTURE TIME MS

FIG 2


VCO FREE RUNNING FREQUENCY
FIG 3
SLOPE 80 Hz/VOLT
+6
+4
+2
0
-2
-4
VCO INPUT VOLTS
600
700
800
900
1000
1100
1200
1300
1400
VCO OUTPUT (REF. 1 KHz) Hz

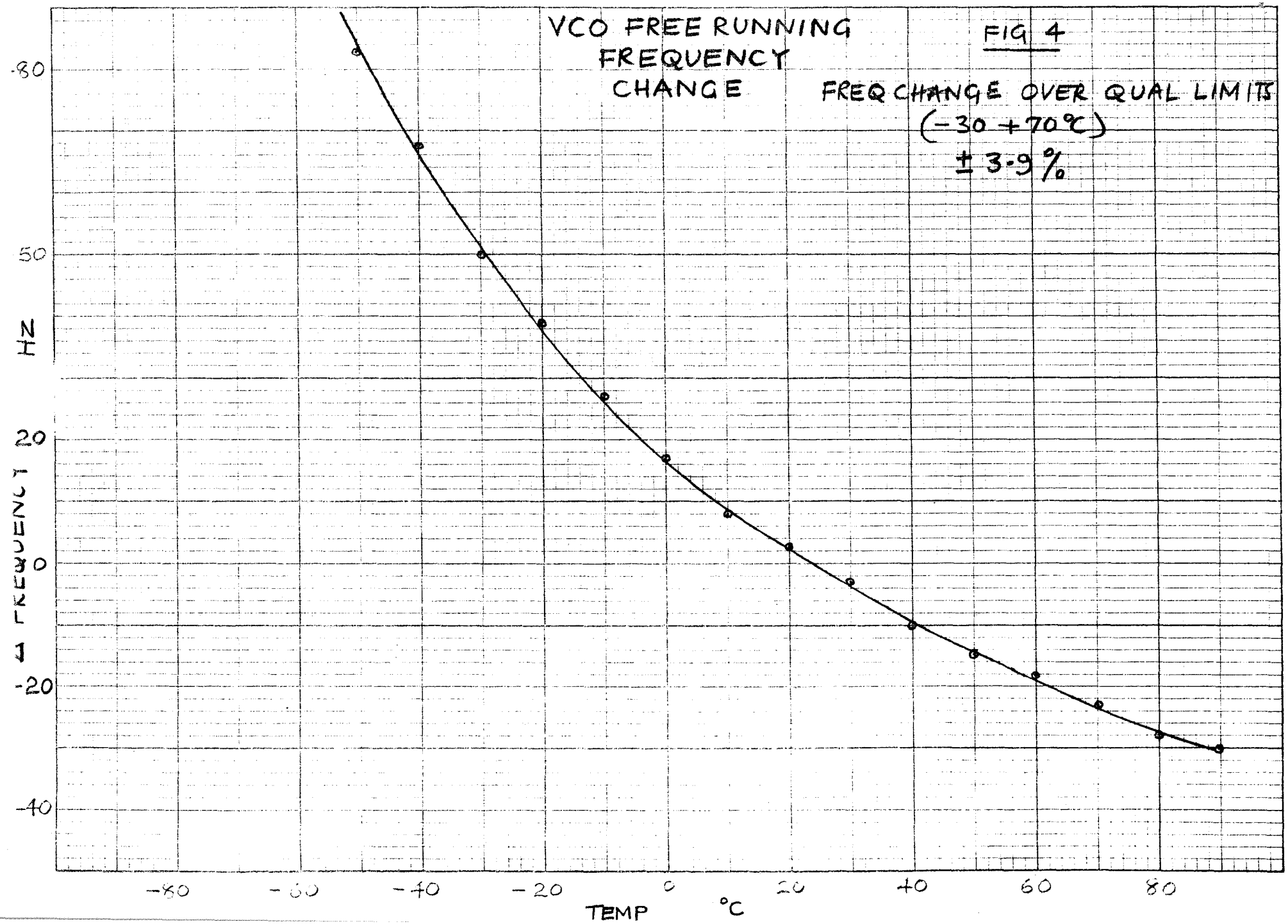
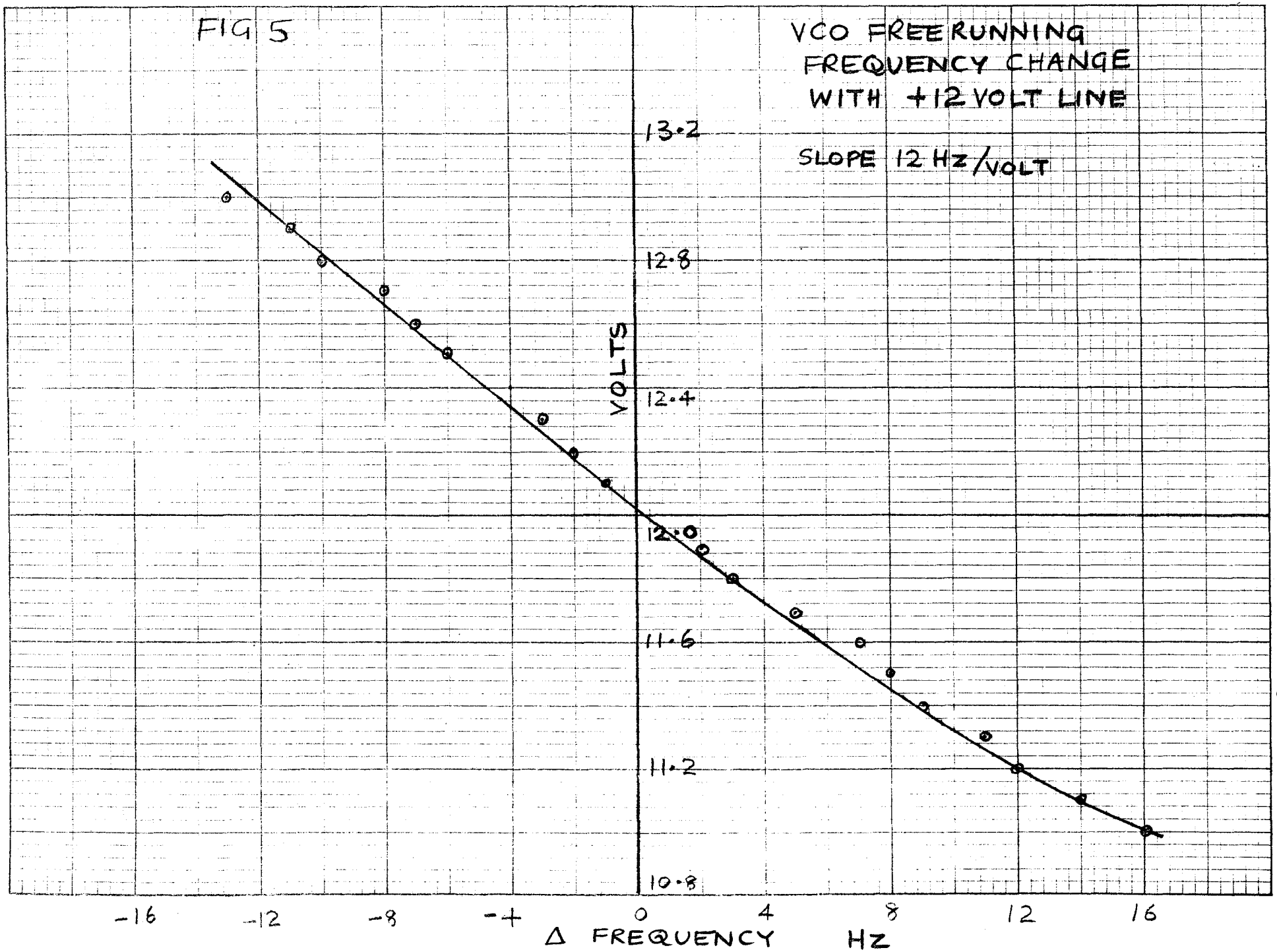
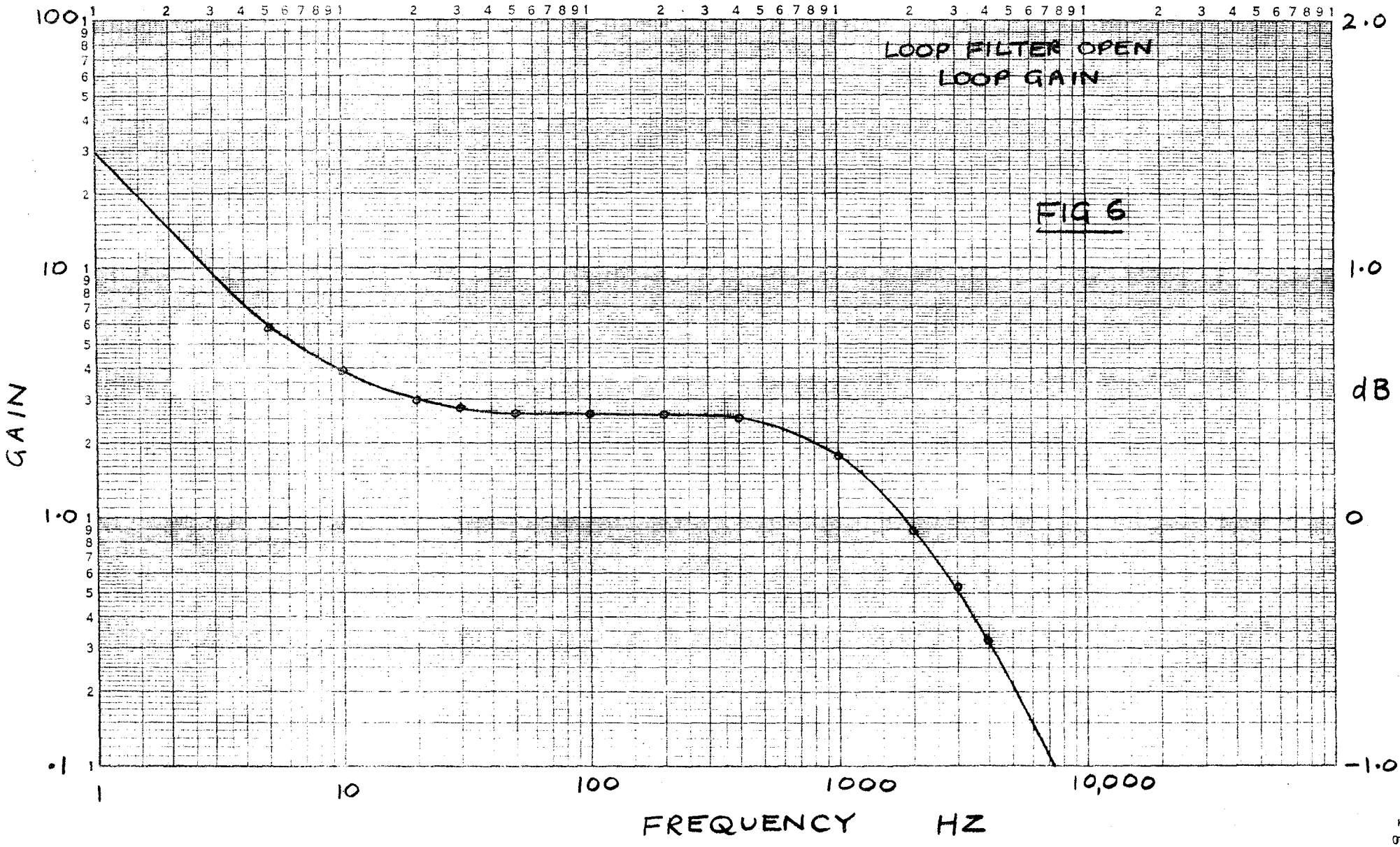
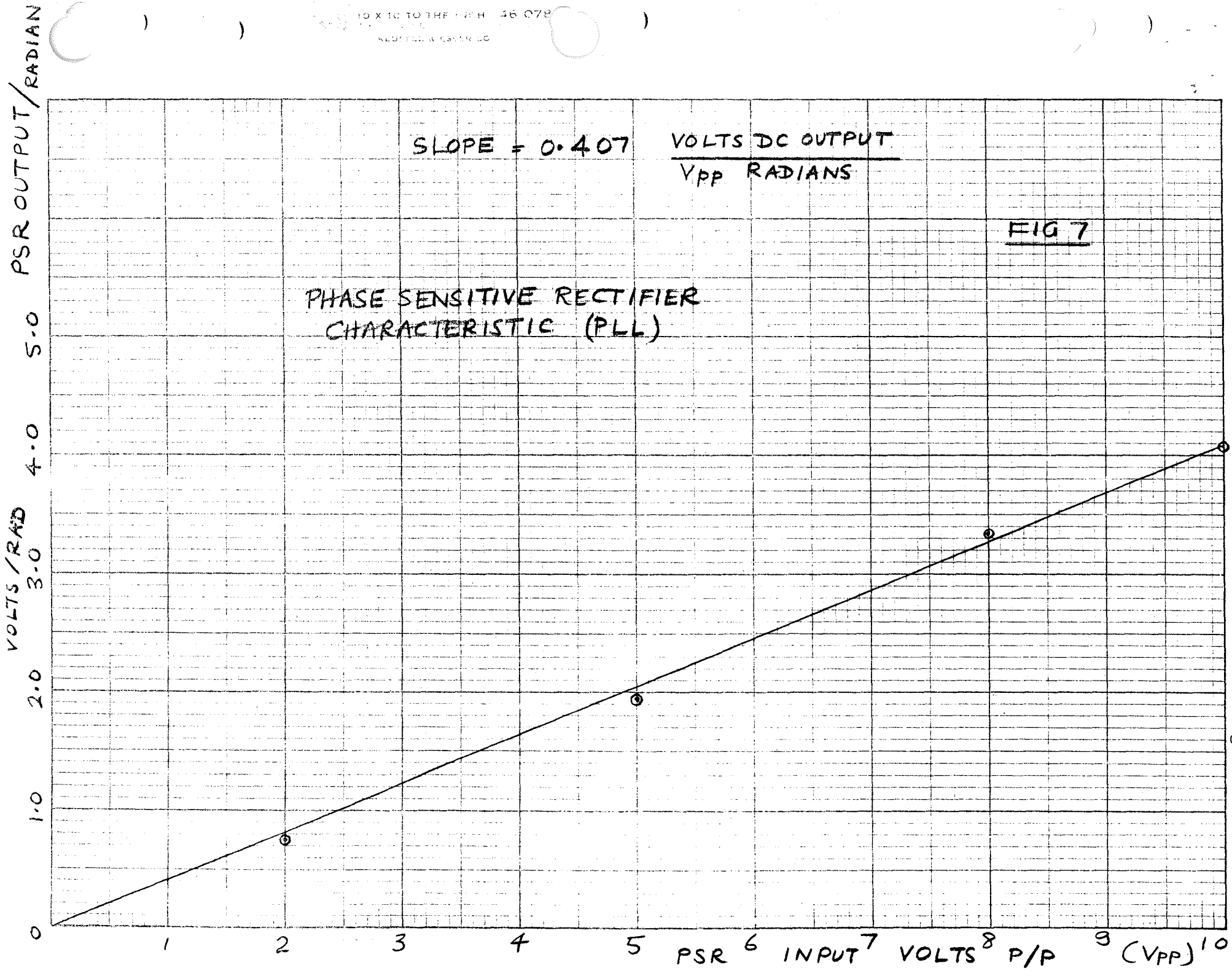

VCO FREE RUNNING
FREQUENCY
CHANGE
FIG 4
FREQ CHANGE OVER QUAL LIMITS
(-30 +70°C)
± 3.9 %
80
50
20
0
-20
-40
FREQUENCY
IN
KHz
-80
-60
-40
-20
0
20
40
60
80
TEMP °C

FIG 5




LOOP FILTER OPEN
LOOP GAIN
FIG 6
GAIN
dB
FREQUENCY HZ
100
10
1.0
.1
2.0
1.0
0
-1.0
1
10
100
1000
10,000


PSR OUTPUT/RADIAN
VOLTS/RAD
0
1.0
2.0
3.0
4.0
5.0
1
2
3
4
5
6
7
8
9
10
PSR INPUT VOLTS P/P (VPP)
SLOPE = 0.407
VOLTS DC OUTPUT
VPP RADIANS
FIG 7
PHASE SENSITIVE RECTIFIER
CHARACTERISTIC (PLL)

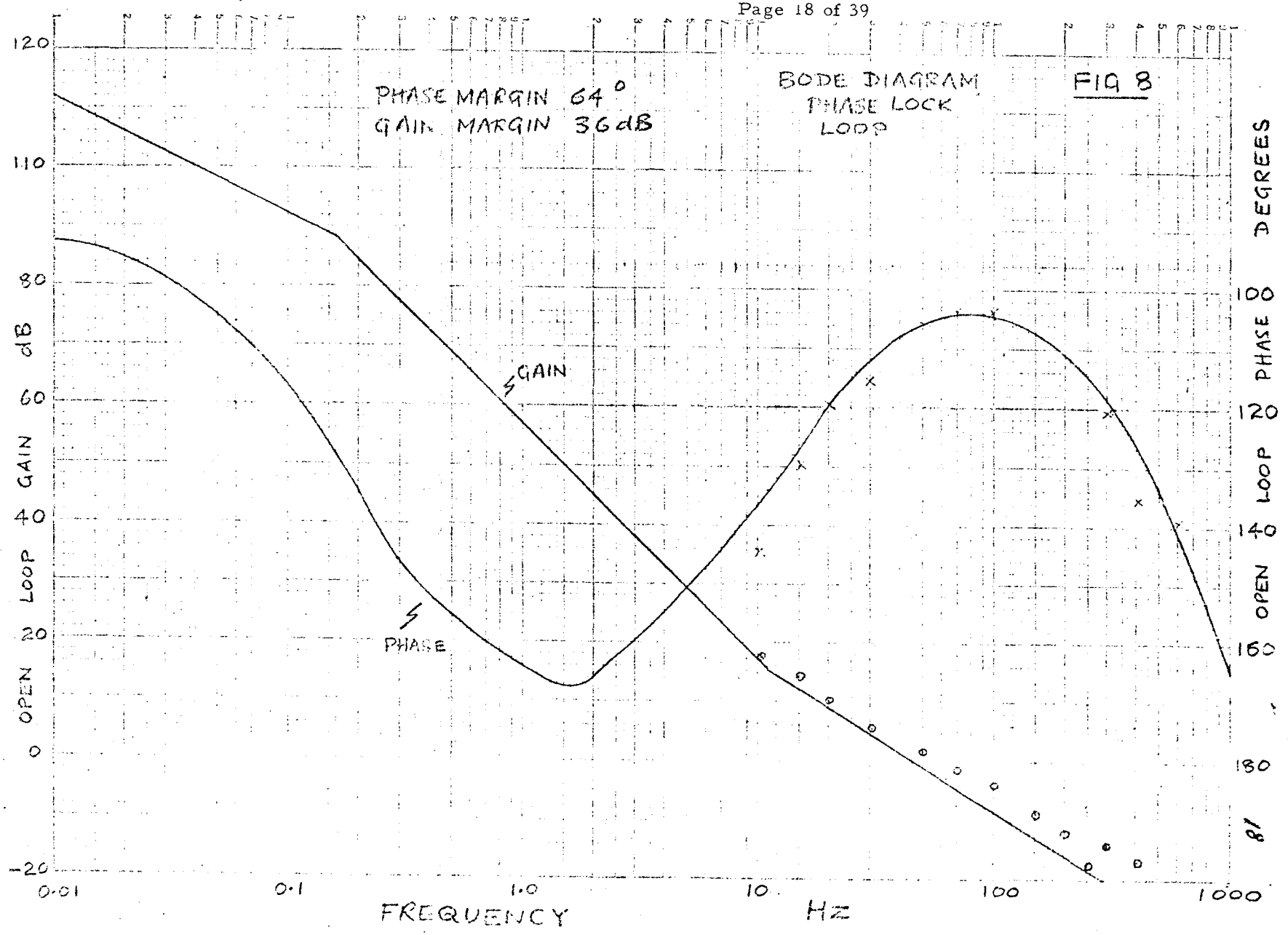
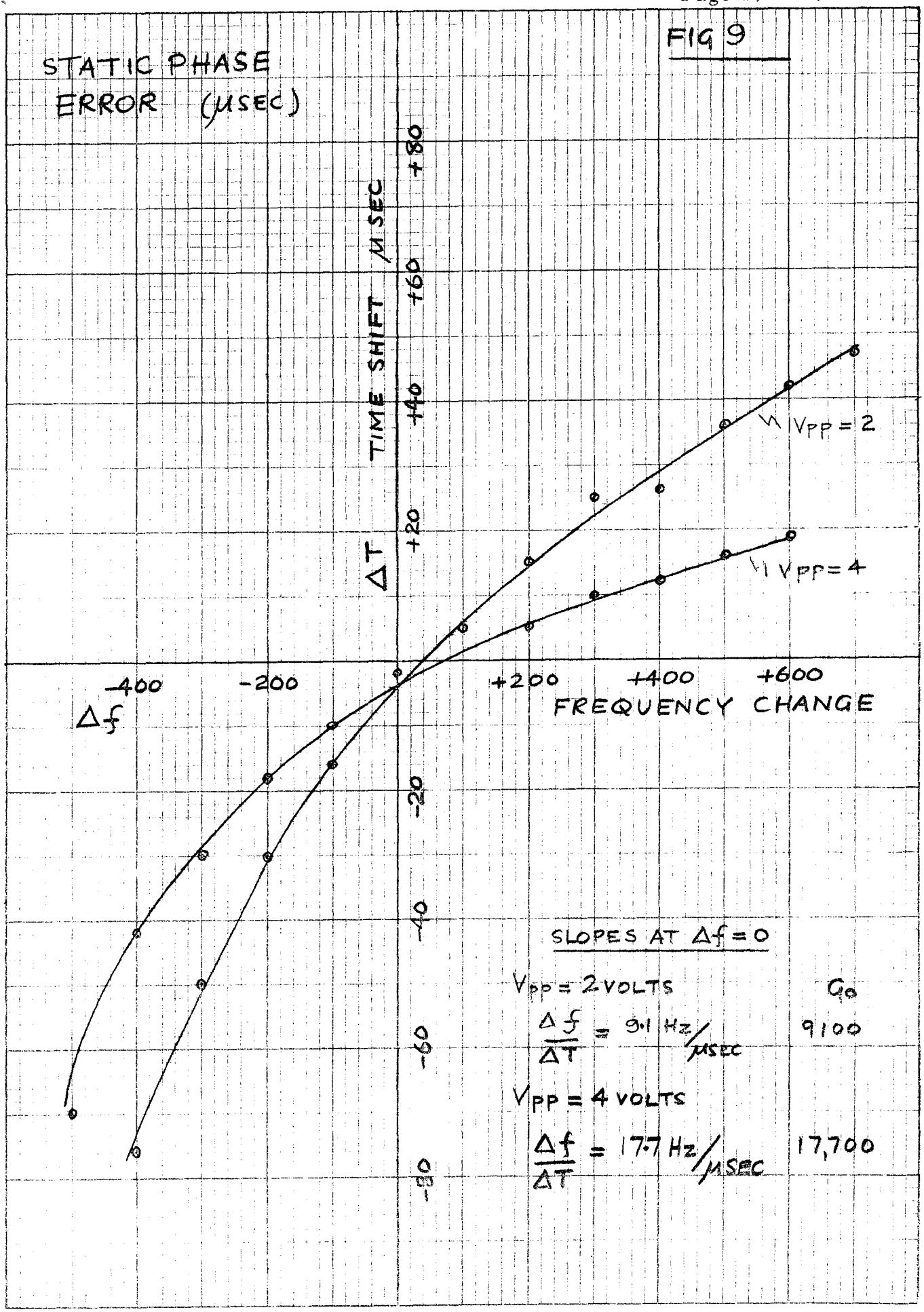

PHASE MARGIN 64°
GAIN MARGIN 36dB
BODE DIAGRAM
PHASE LOCK
LOOP
FIG 8
GAIN
PHASE
OPEN LOOP GAIN dB
120
110
80
60
40
20
0
-20
OPEN LOOP PHASE DEGREES
100
120
140
160
180
0.01
0.1
1.0
10
100
1000
FREQUENCY
HZ

FIG 9



SLOPES AT $\Delta f = 0$

$V_{PP} = 2$ VOLTS $\quad G_o$

$\frac{\Delta f}{\Delta T} = 9.1$ Hz/μSEC $\quad 9100$

$V_{PP} = 4$ VOLTS

$\frac{\Delta f}{\Delta T} = 17.7$ Hz/μSEC $\quad 17{,}700$

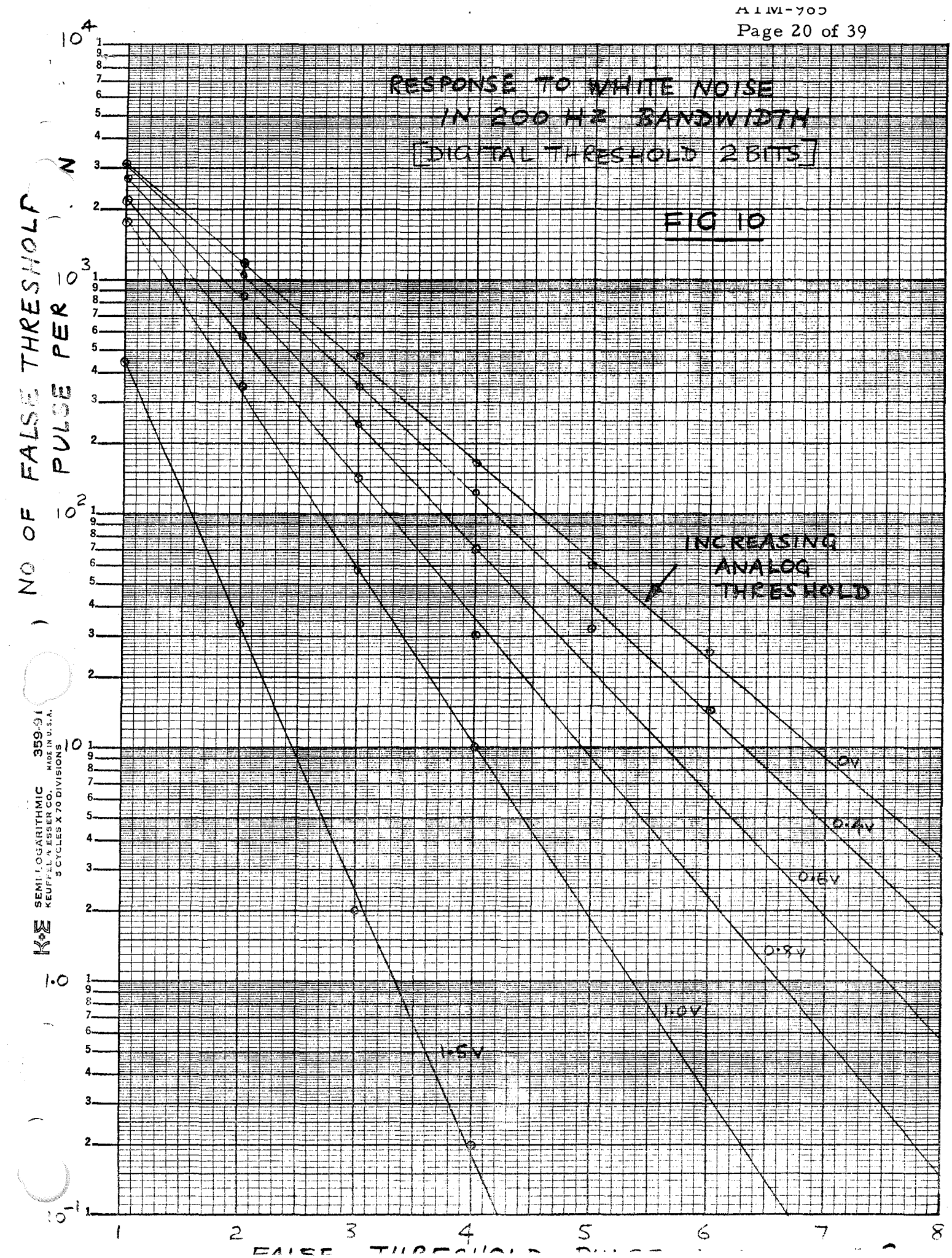
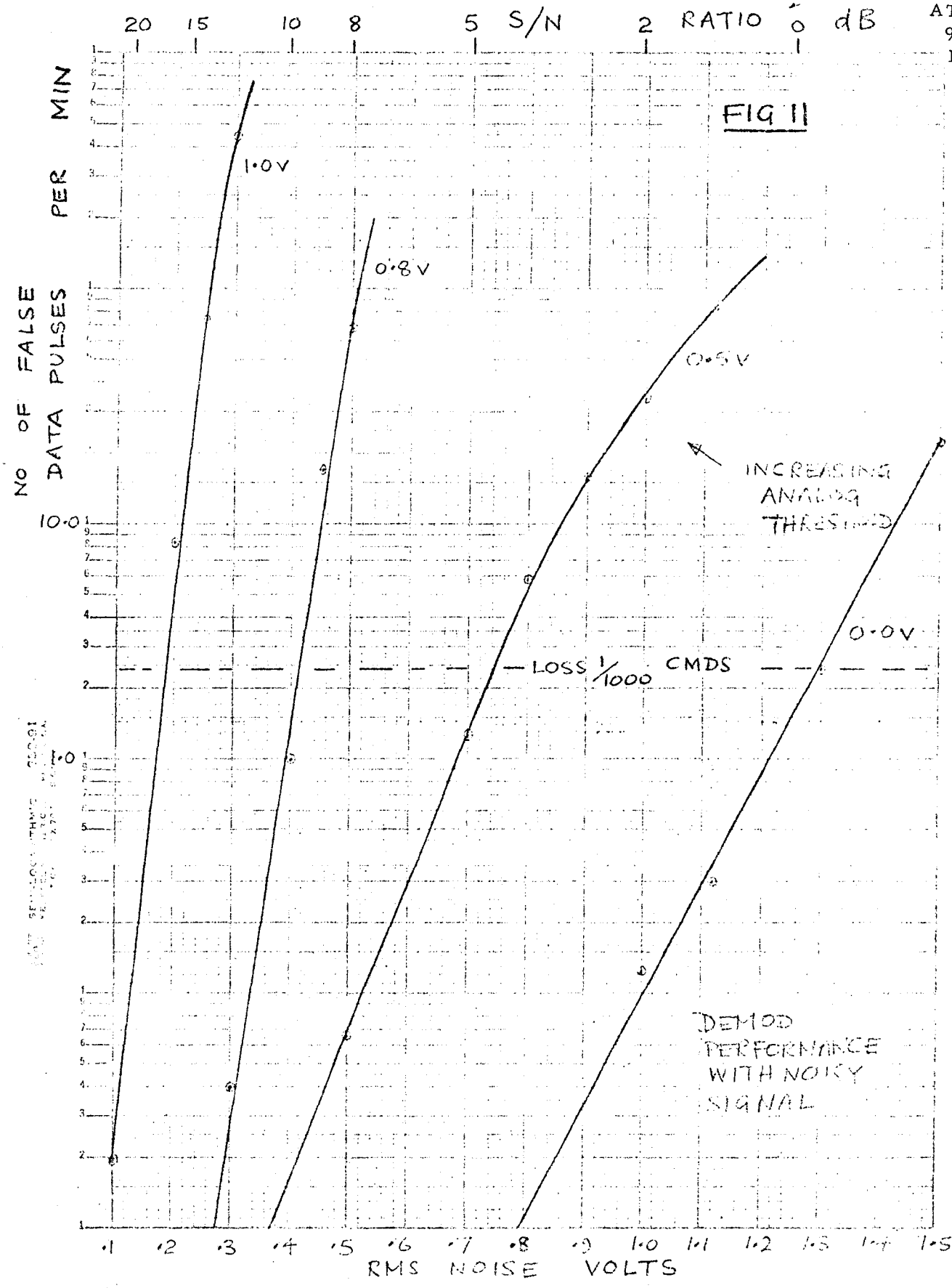

RESPONSE TO WHITE NOISE
IN 200 HZ BANDWIDTH
[DIGITAL THRESHOLD 2 BITS]
FIG 10
NO OF FALSE THRESHOLD PULSES PER N
INCREASING ANALOG THRESHOLD
0V
0.4V
0.6V
0.8V
1.0V
1.5V
SEMI LOGARITHMIC 359-91
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS
FALSE THRESHOLD PULSE

FIG 11


20 15 10 8 5 S/N 2 RATIO 0 dB
NO OF FALSE DATA PULSES PER MIN
1·0V
0·8V
0·5V
0·0V
INCREASING ANALOG THRESHOLD
LOSS 1/1000 CMDS
10·0
1·0
DEMOD PERFORMANCE WITH NOISY SIGNAL
·1 ·2 ·3 ·4 ·5 ·6 ·7 ·8 ·9 1·0 1·1 1·2 1·3 1·4 1·5
RMS NOISE VOLTS

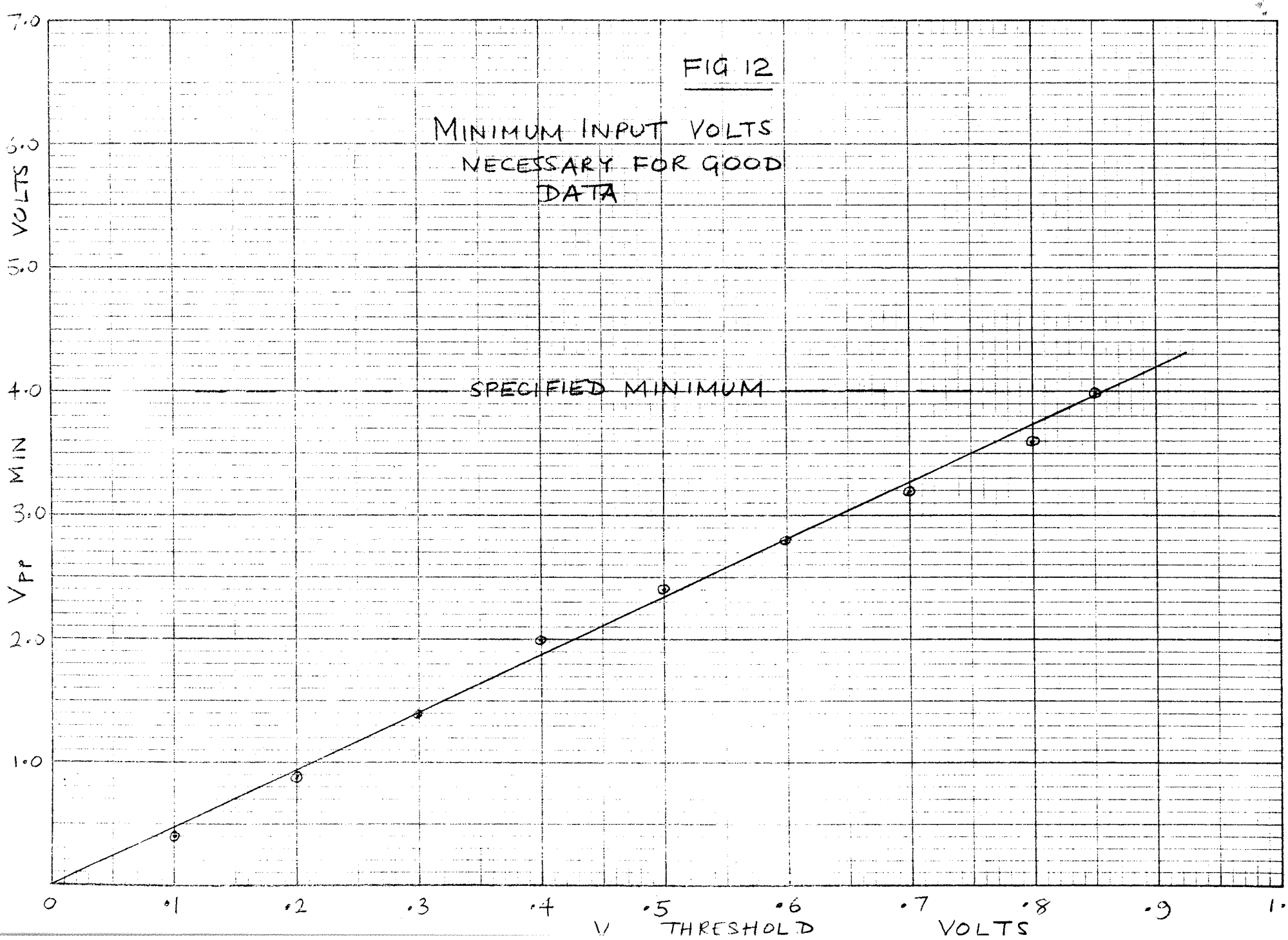


FIG 12
MINIMUM INPUT VOLTS
NECESSARY FOR GOOD
DATA
SPECIFIED MINIMUM
7.0
6.0
5.0
4.0
3.0
2.0
1.0
V_{PP} MIN
0
.1
.2
.3
.4
.5
.6
.7
.8
.9
1.0
V THRESHOLD VOLTS

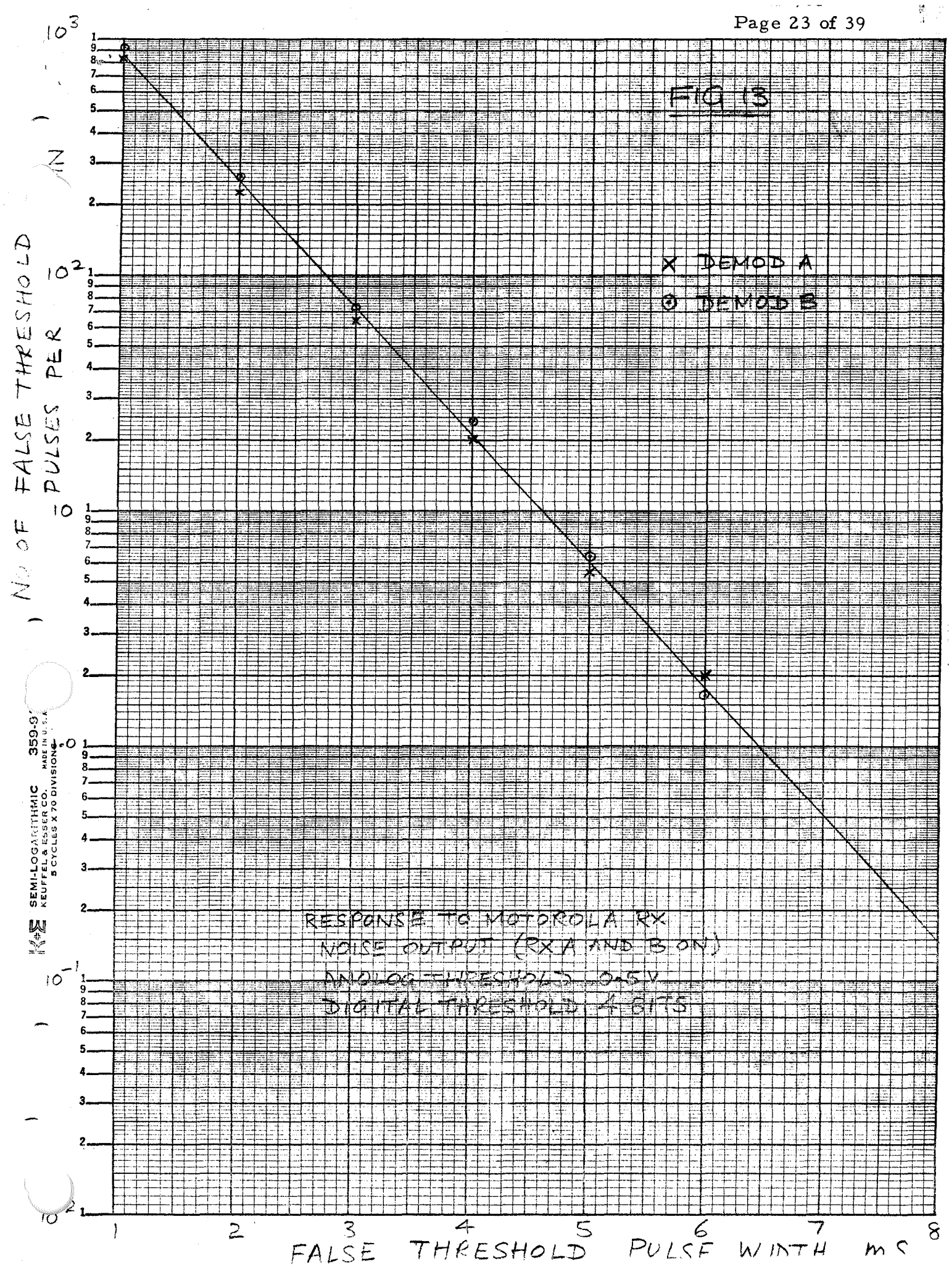
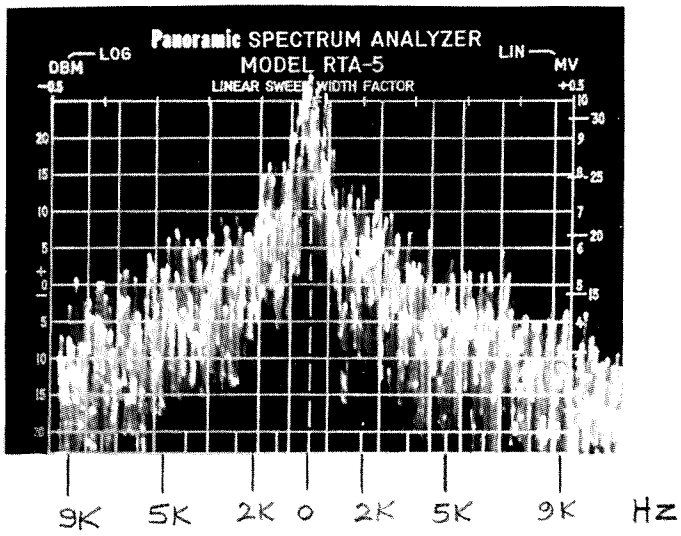
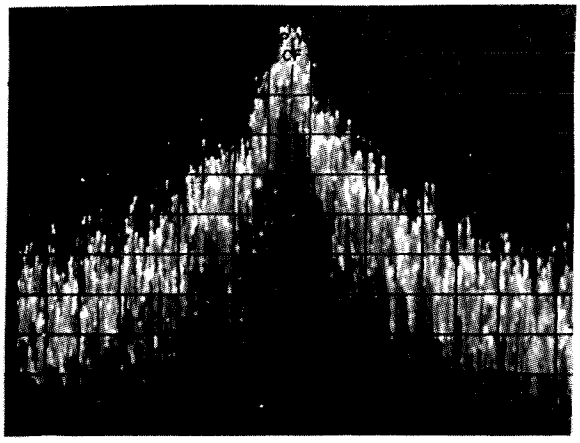


FIG 13
X DEMOD A
⊙ DEMOD B
NO OF FALSE THRESHOLD PULSES PER N
RESPONSE TO MOTOROLA RX
NOISE OUTPUT (RX A AND B ON)
ANALOG THRESHOLD 0.5V
DIGITAL THRESHOLD 4 BITS
FALSE THRESHOLD PULSE WIDTH mS
SEMI-LOGARITHMIC 359-3
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS

FIG 14

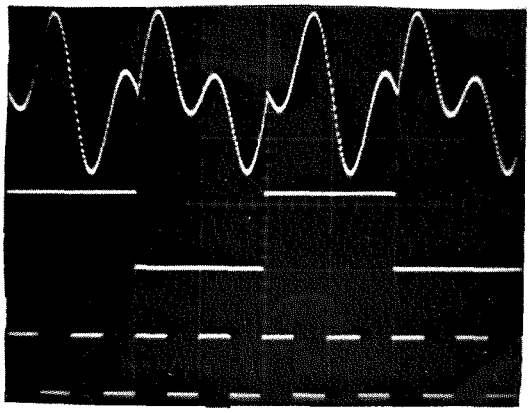
MOTOROLA RX (10 V_{PP} CLIPPED)



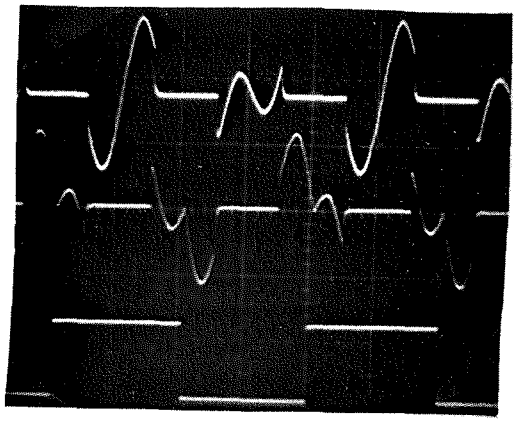


PHILCO RX
(21 V_{PP})

RECEIVER NOISE SPECTRA

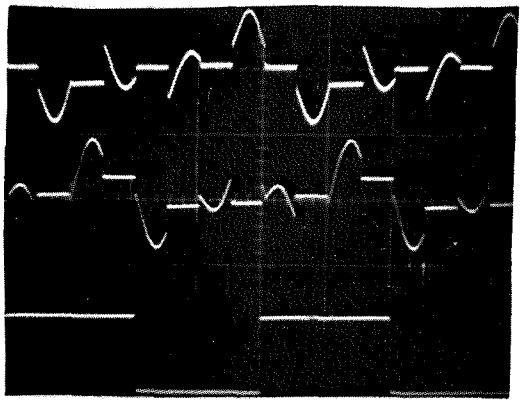


(i)

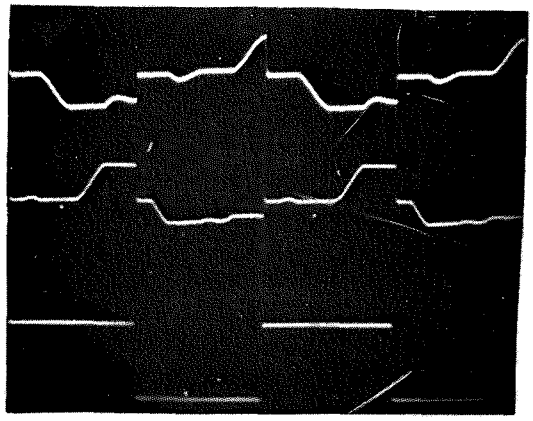


(ii)

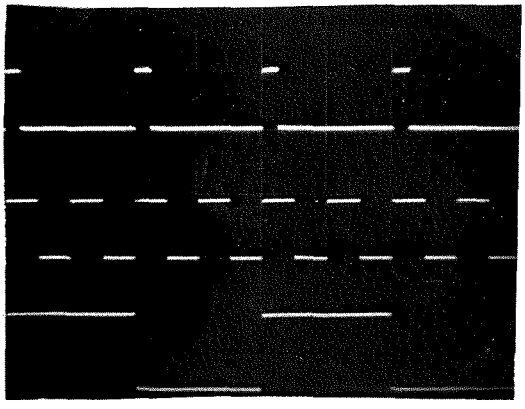
FIG 15



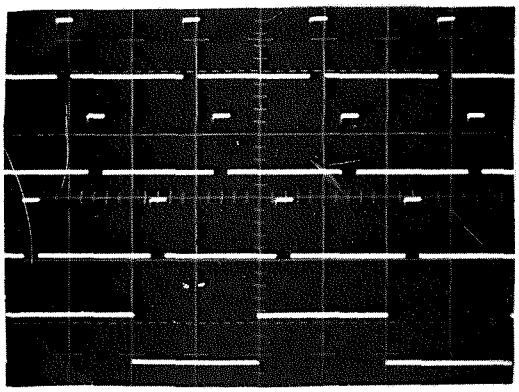
(iii)



(iv)



(v)



(vi)

TEST SET UP FOR CLOSED LOOP FREQUENCY RESPONSE

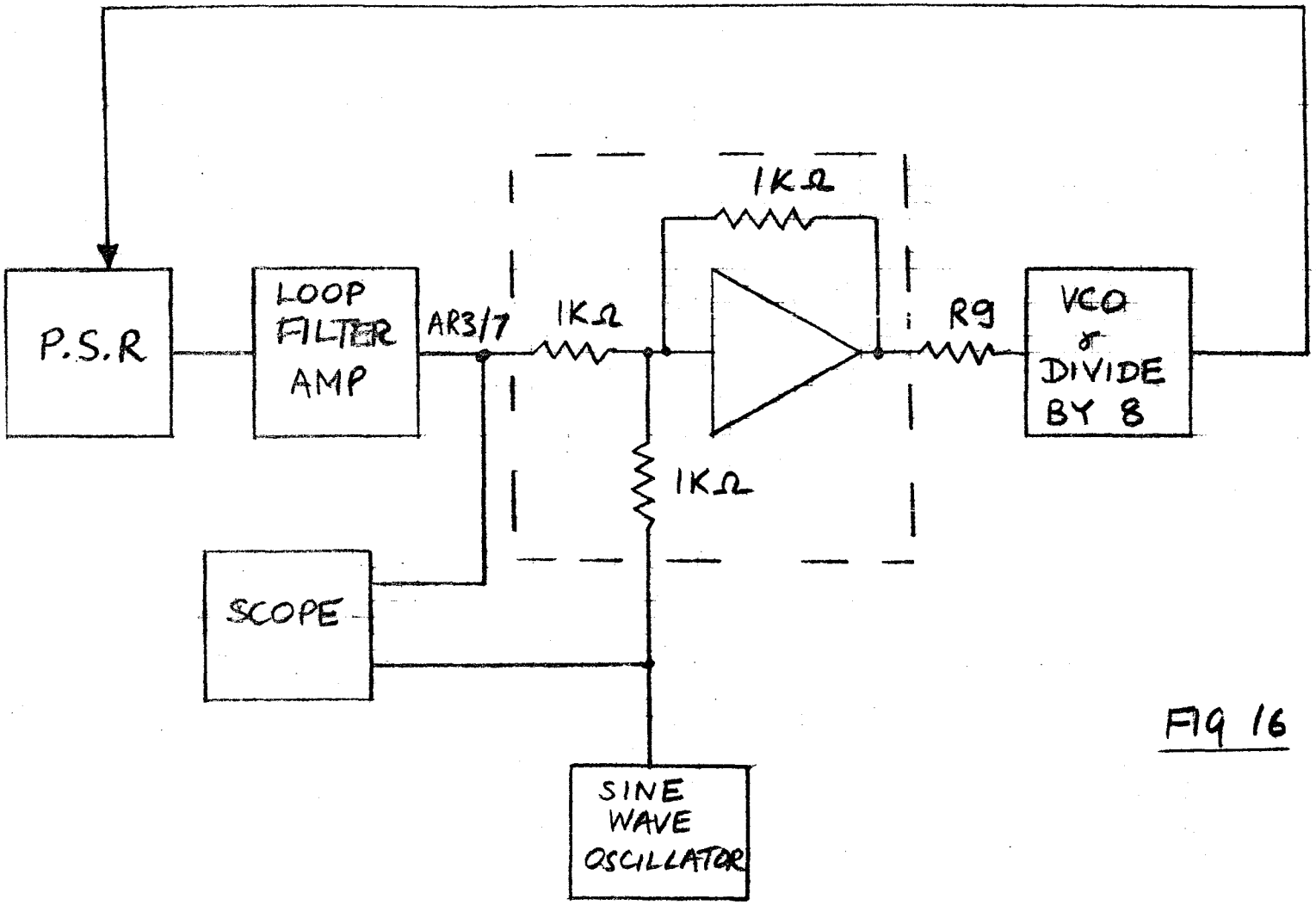
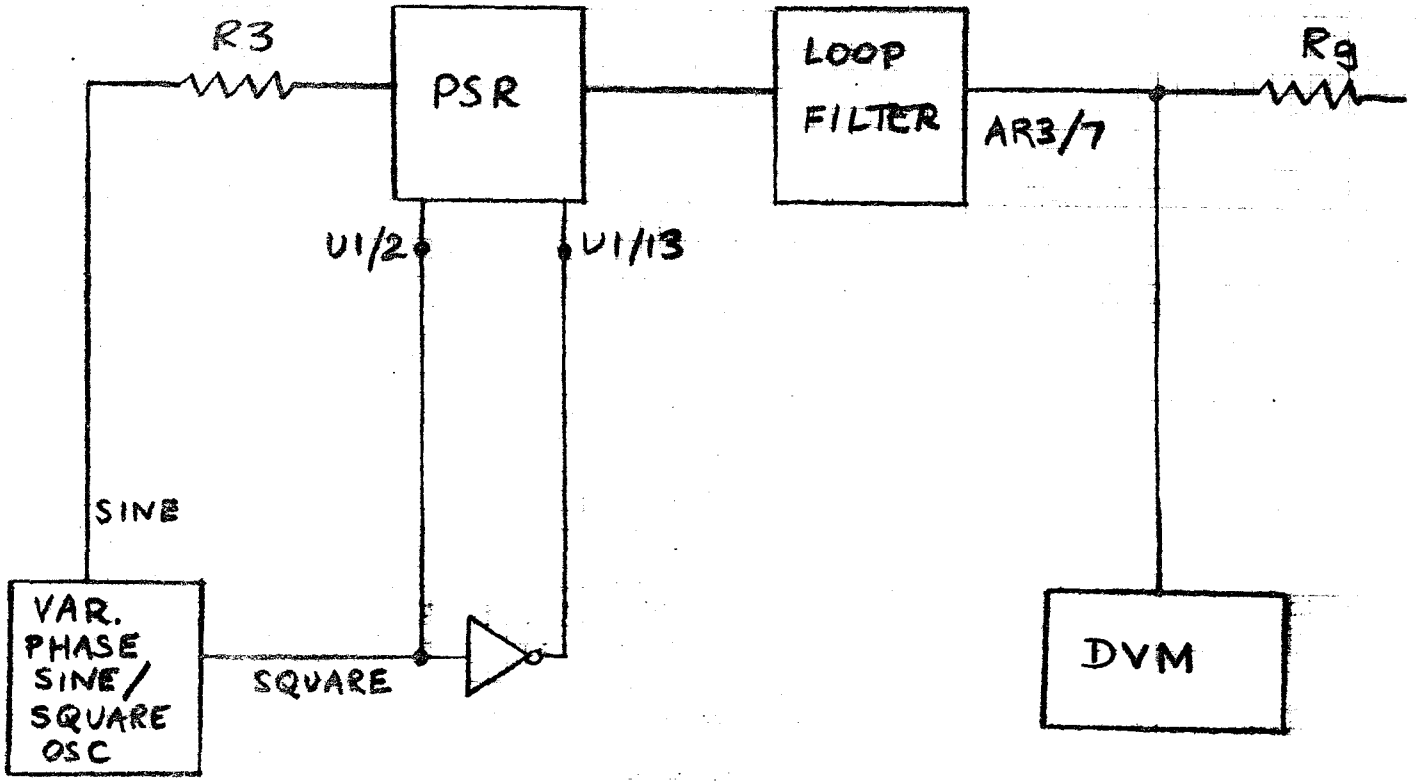


Fig 16



TEST SET UP FOR PSR CHARACTERISTIC

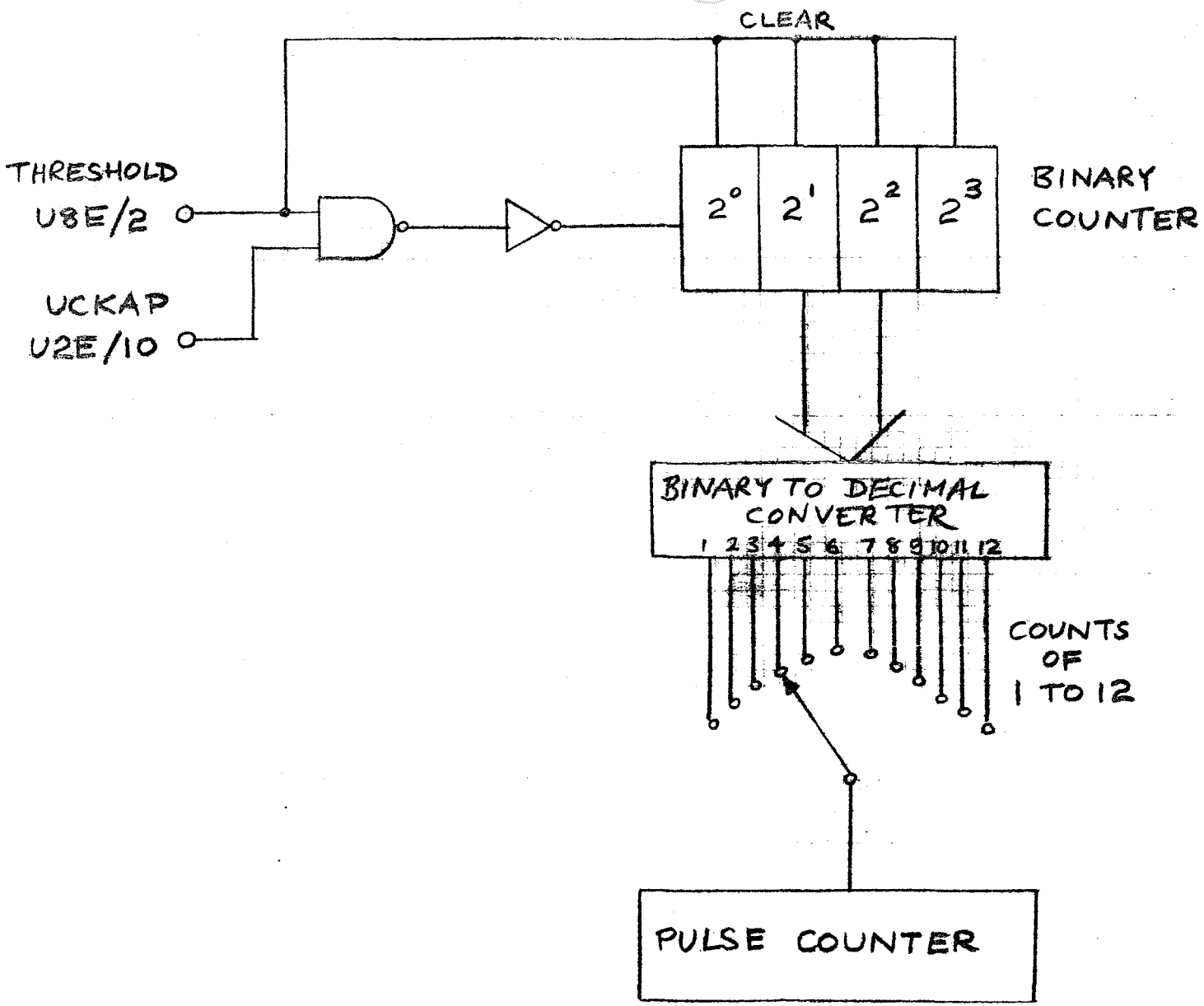


FIG 18

THRESHOLD ANALYSIS SET UP

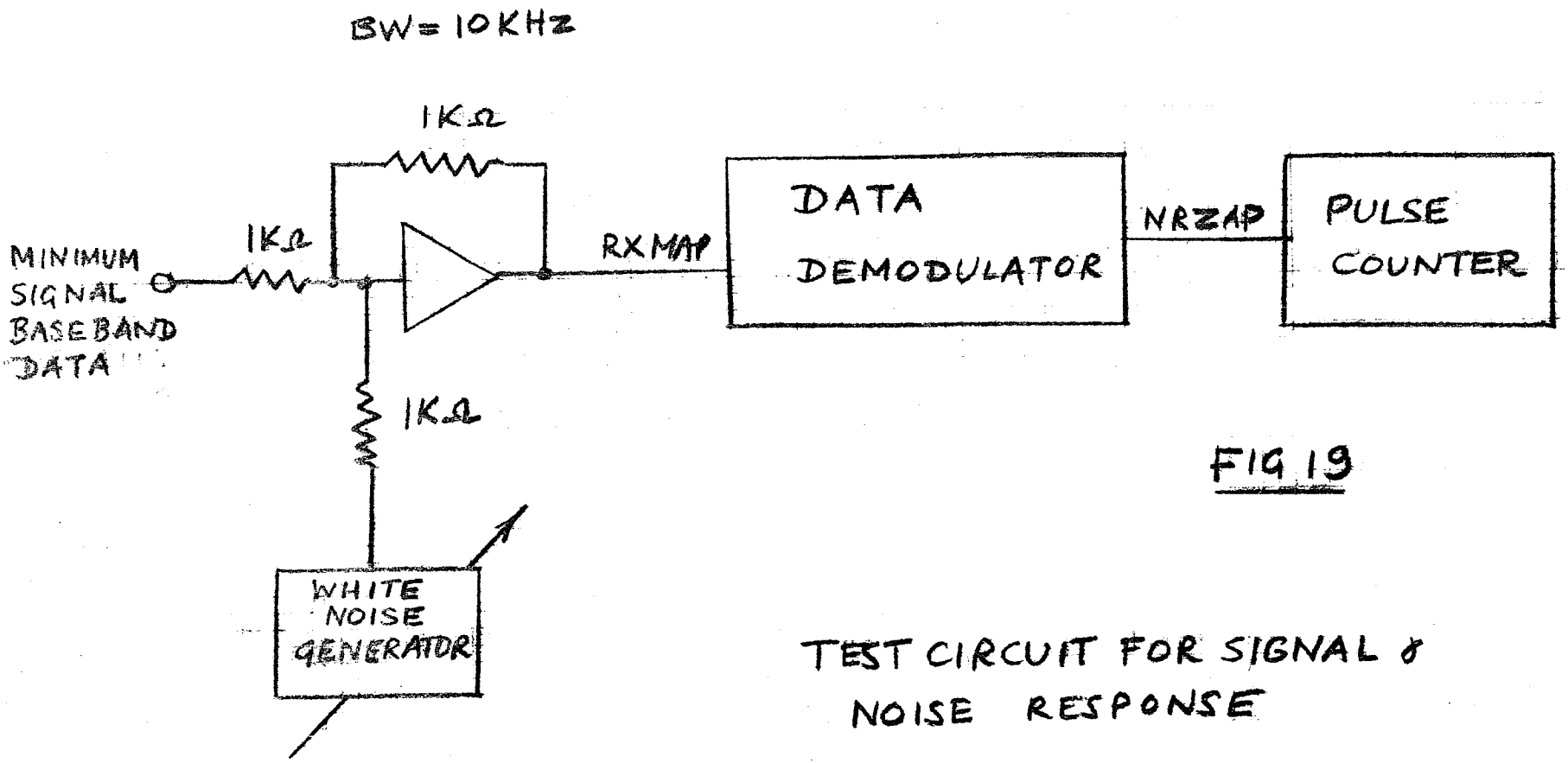
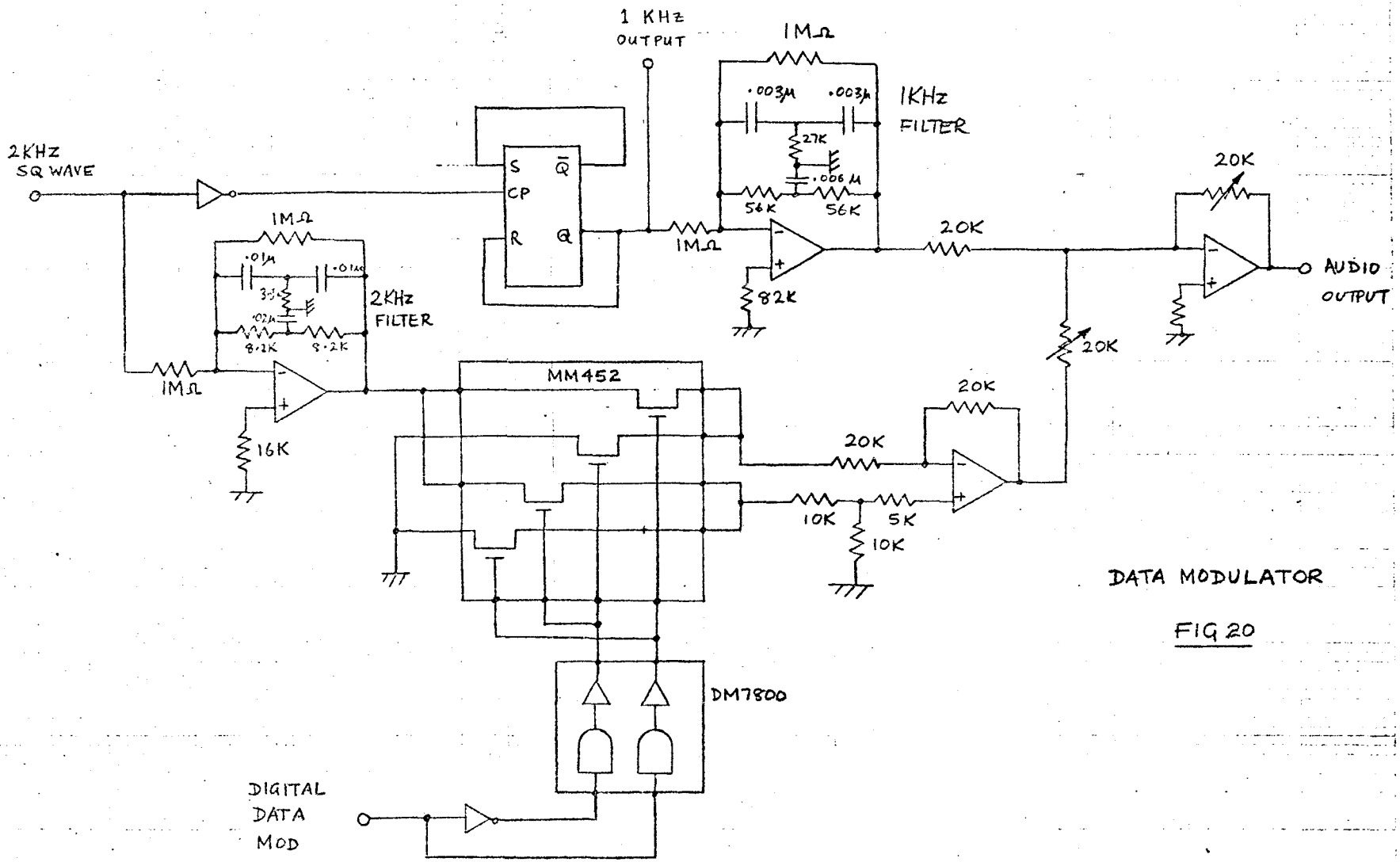


FIG 19

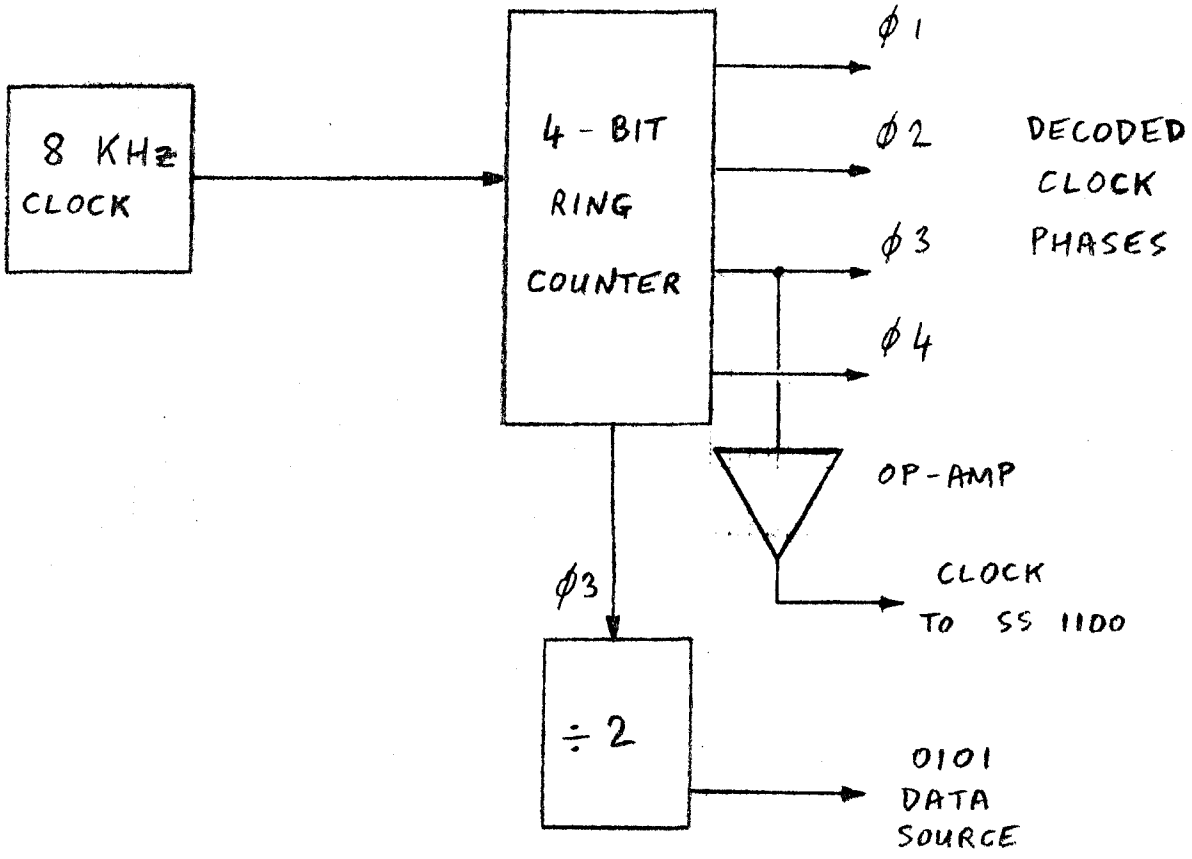
TEST CIRCUIT FOR SIGNAL & NOISE RESPONSE

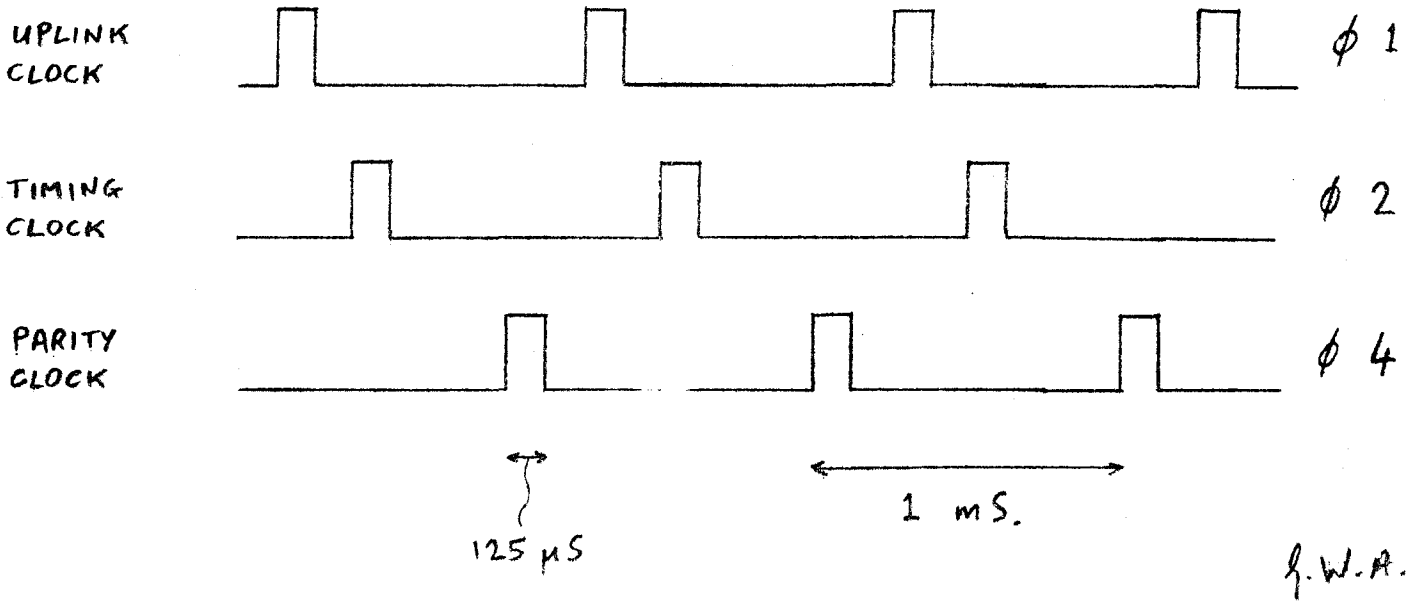


DATA MODULATOR

FIG 20

FIG. 21 UPLINK CLOCK GENERATOR





G.W.A.

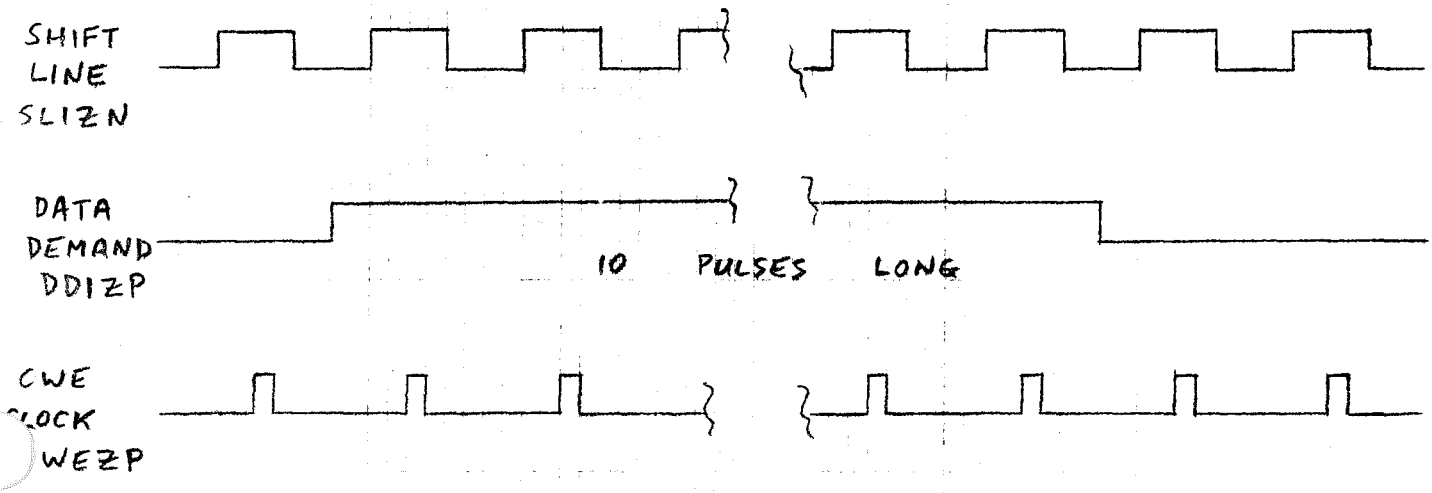
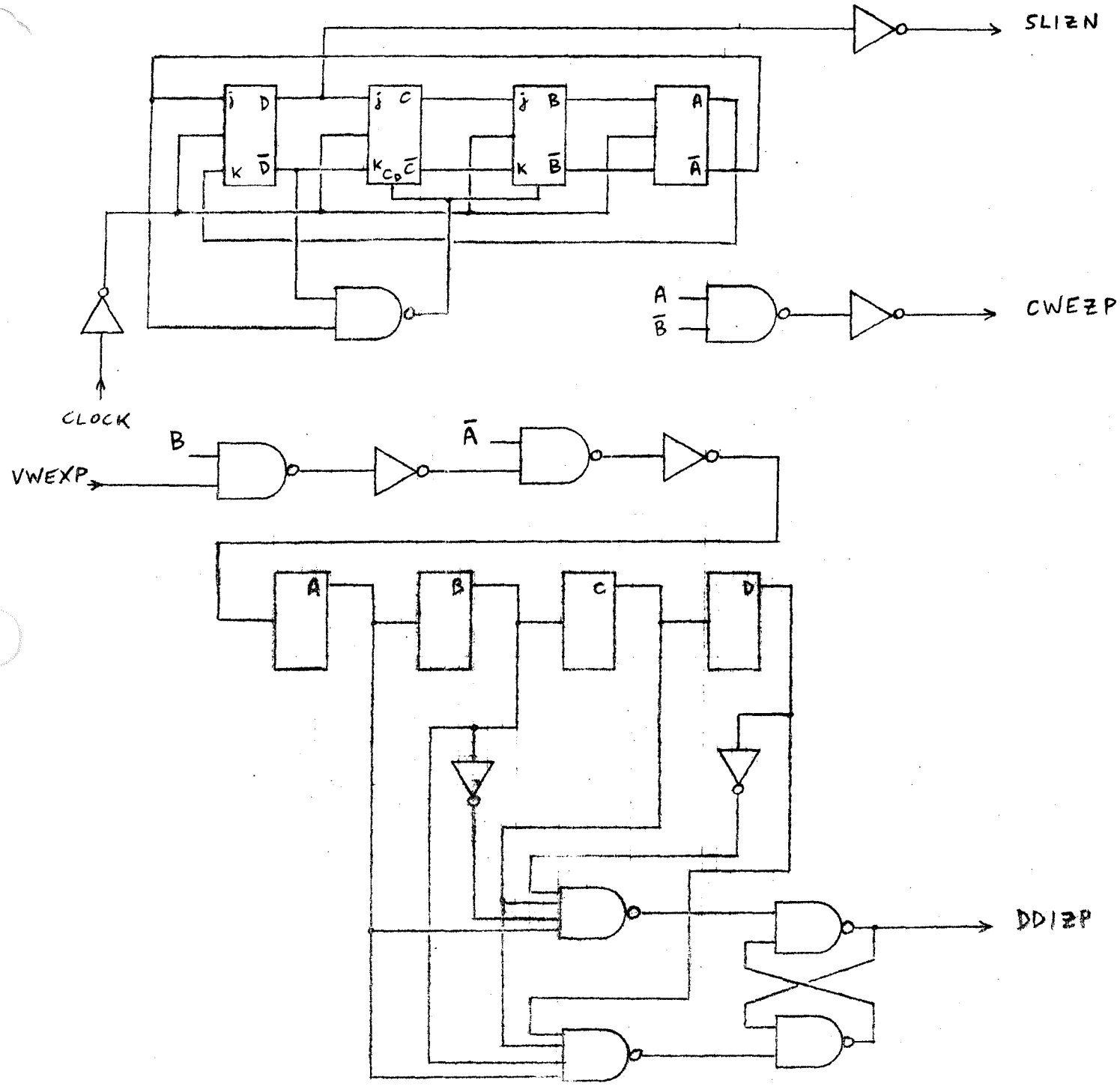


FIG. 22 DOWNLINK TIMING SIGNALS



DATA PROCESSOR SIMULATOR

FIG. 23 CVW TIMING SIGNALS

R.W.A.
12-4-70

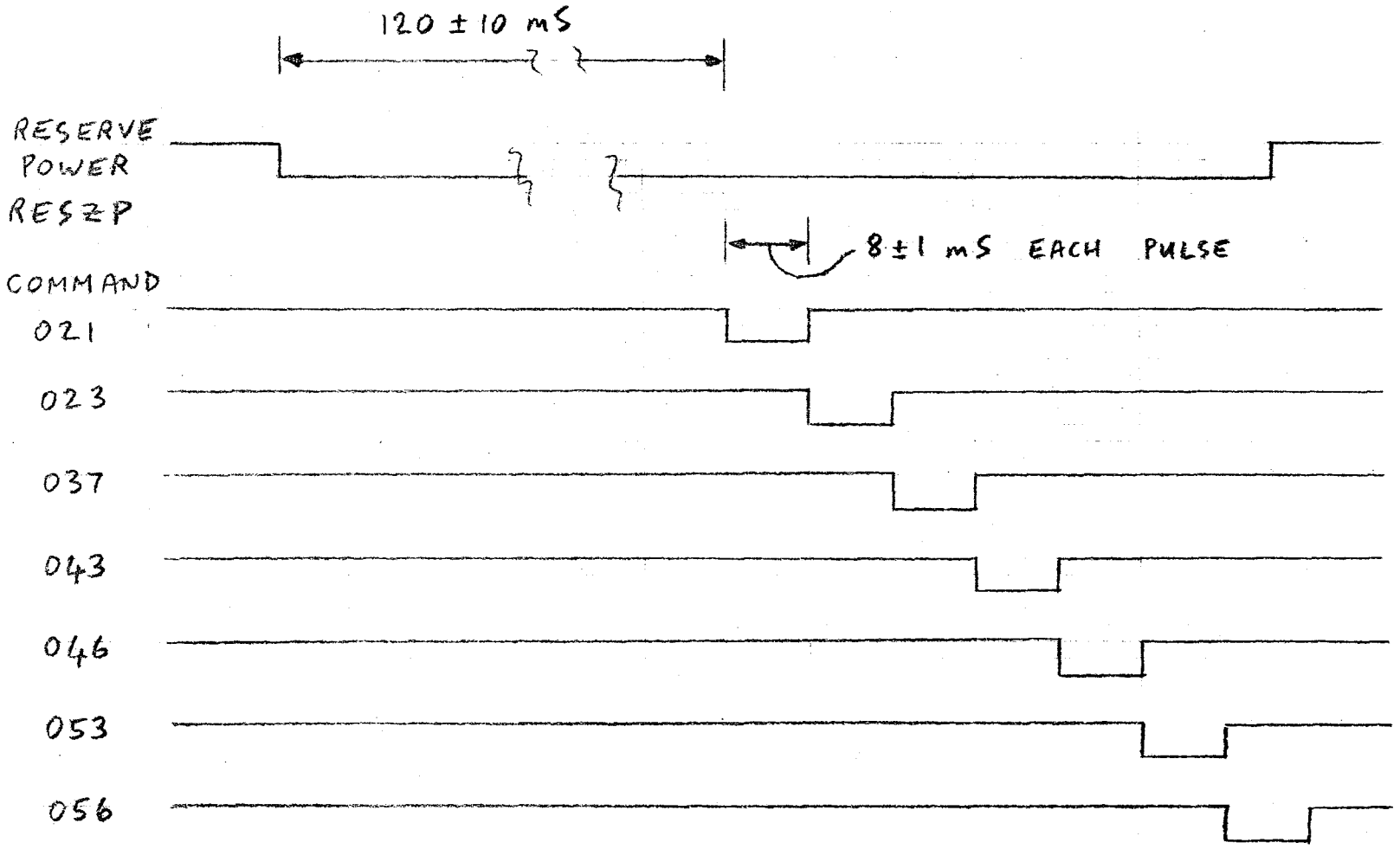


FIG. 24 RIPPLE - OFF COMMAND OUTPUT

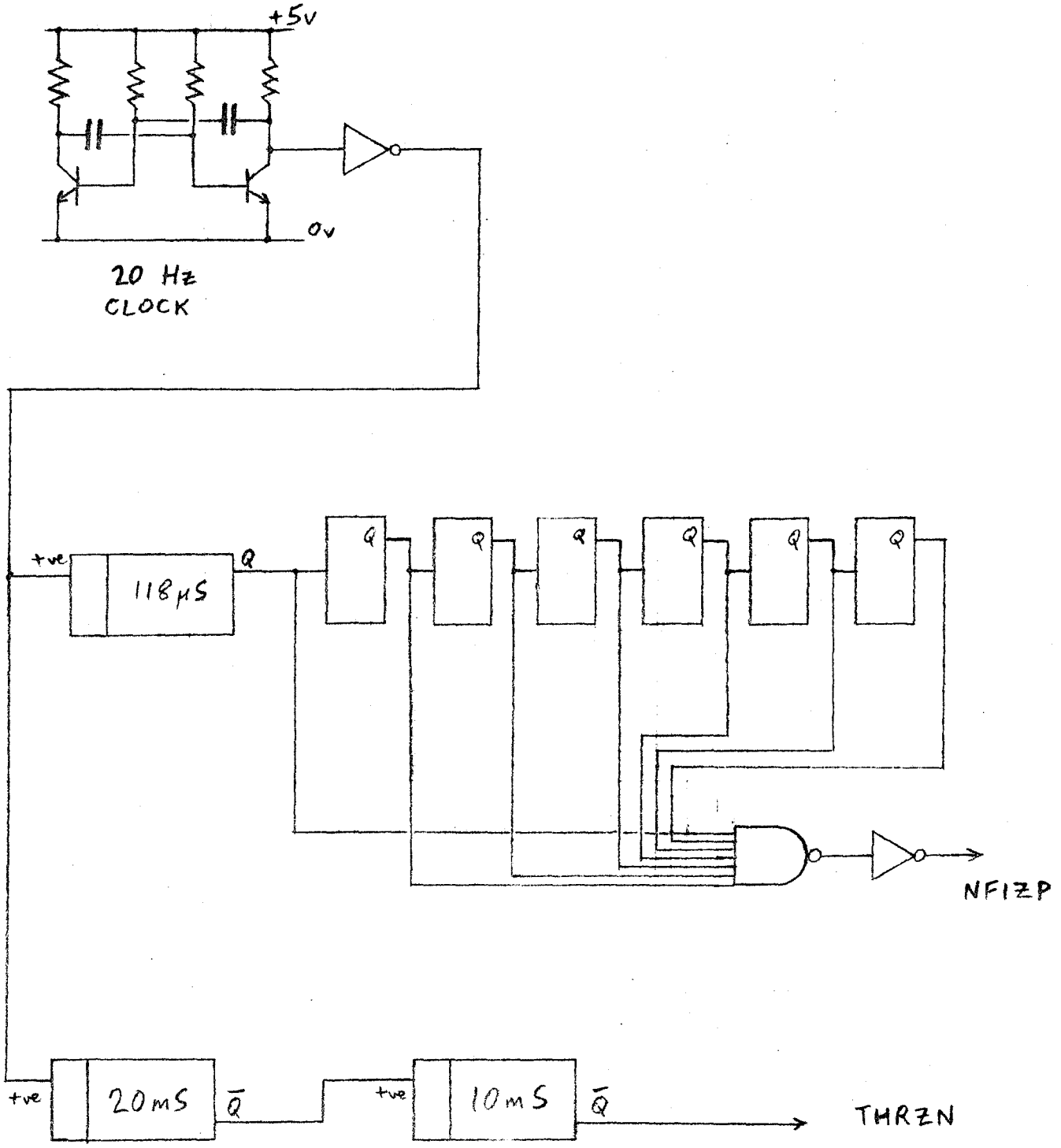
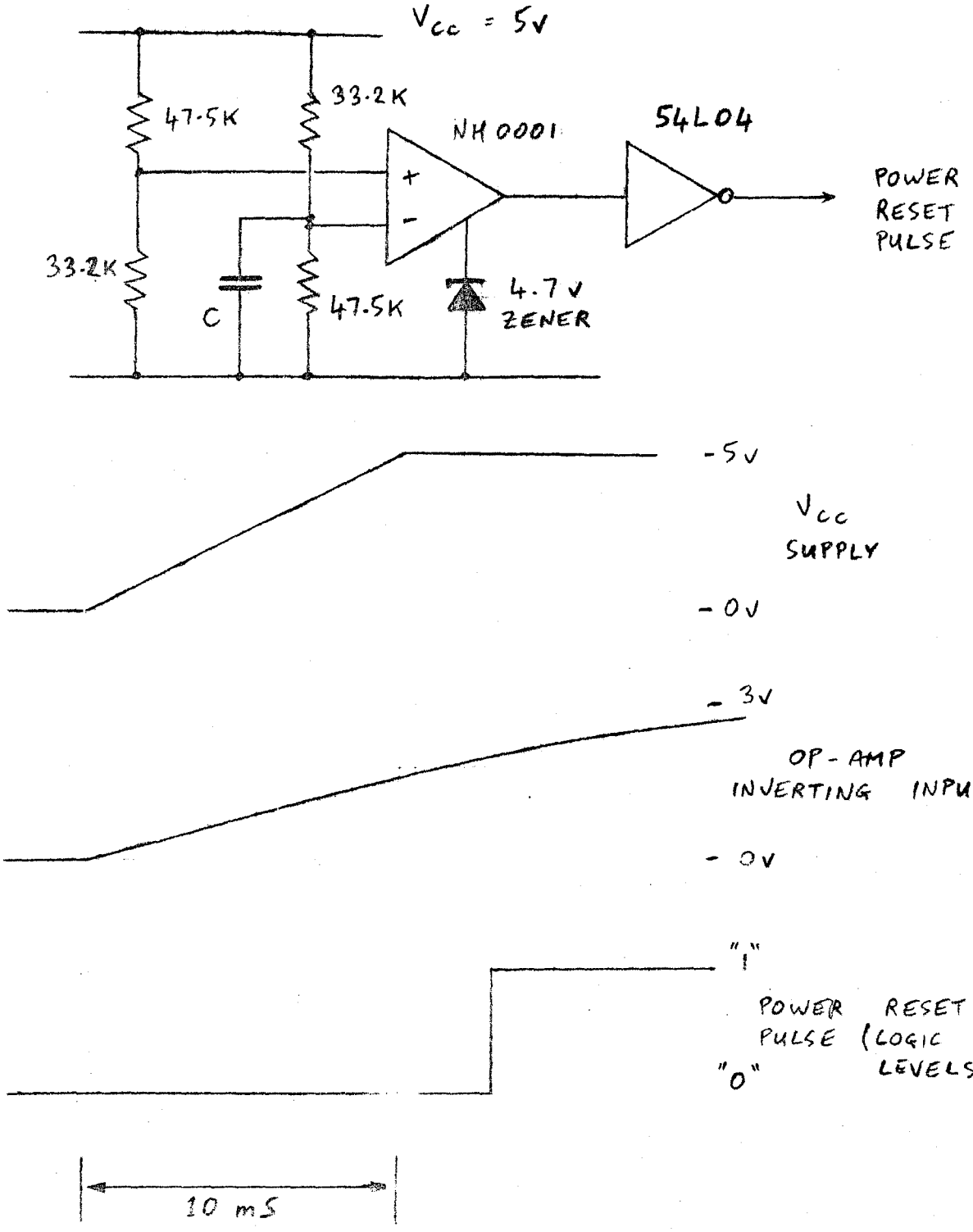


FIG. 25

REPEATED COMMAND TEST SET

Q.W.A
12-9-70

FIG. 26 POWER RESET CIRCUIT



f.W.A
1-25-71

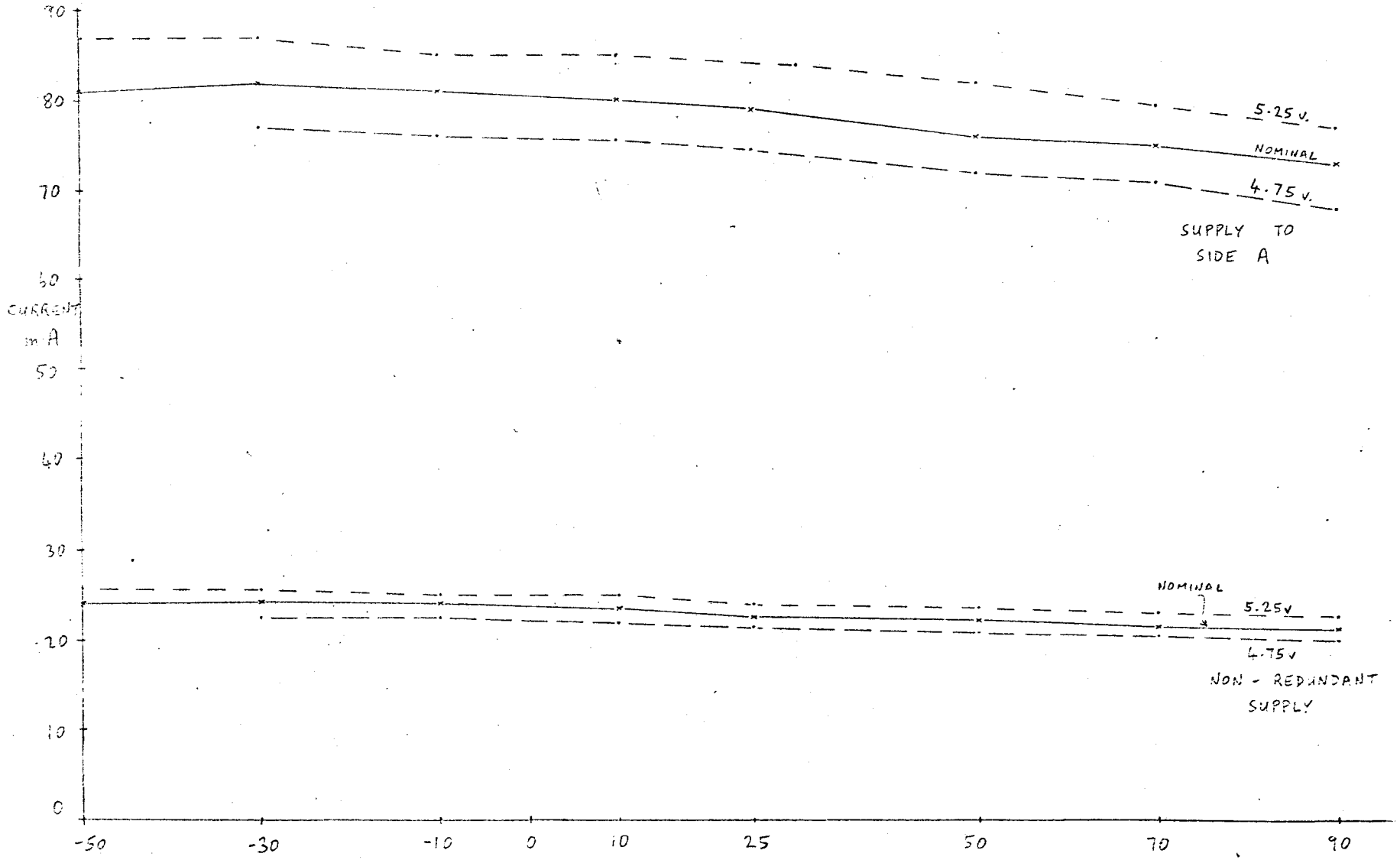


FIG. 27 5 VOLT SUPPLY VARIATIONS WITH TEMPERATURE

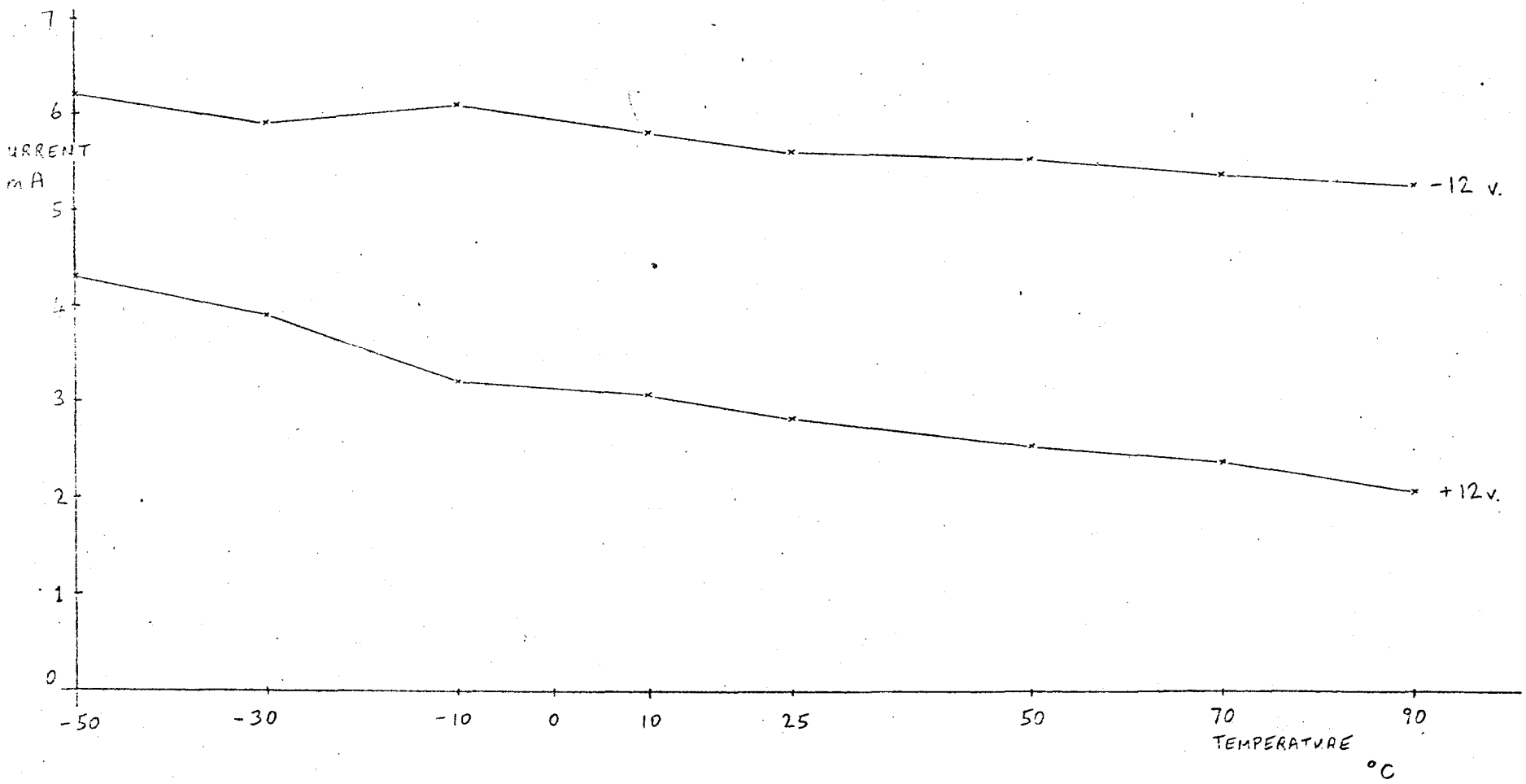
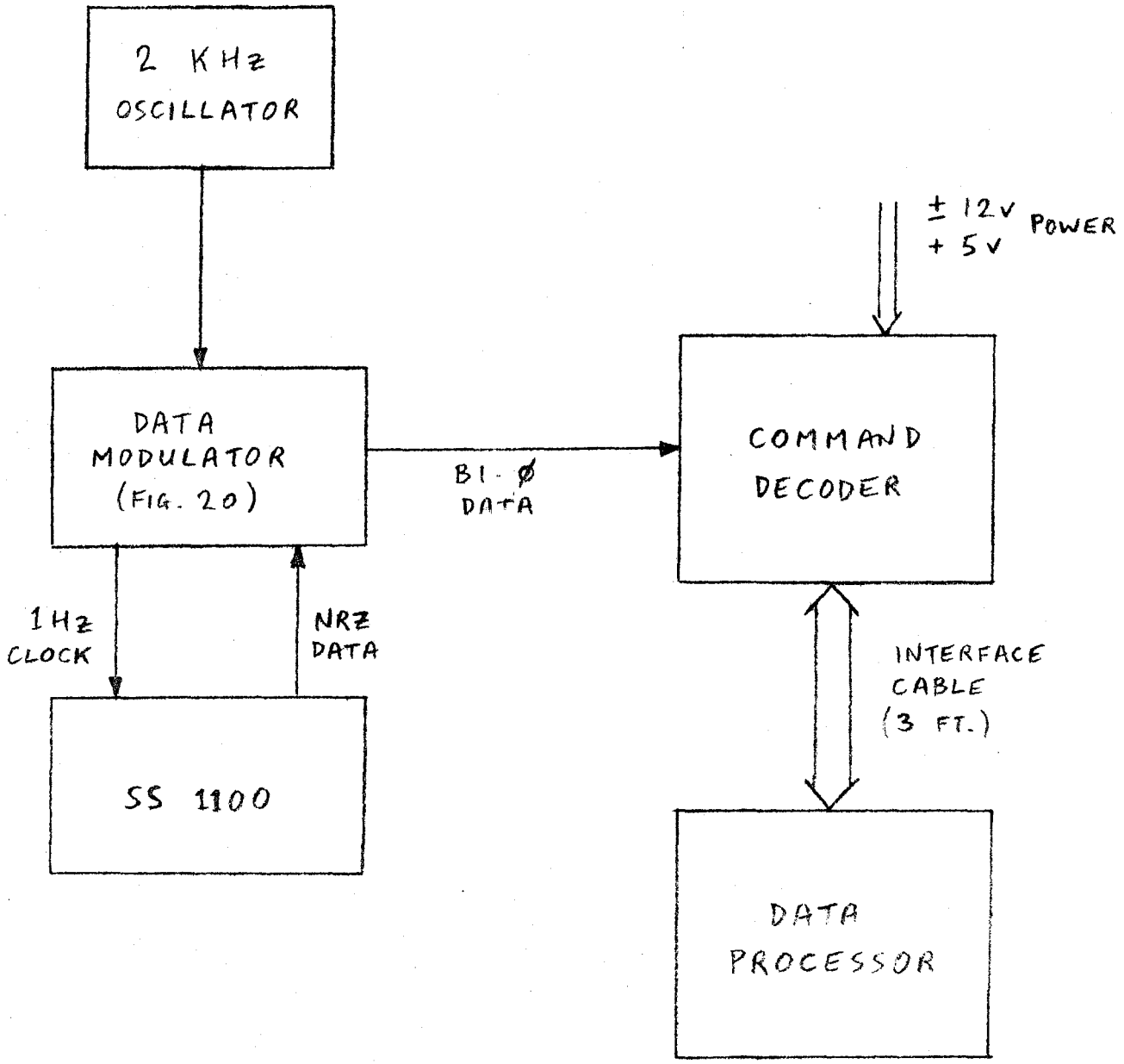


FIG. 2.8 12 VOLT SUPPLY VARIATIONS WITH TEMPERATURE

FIG. 29 DATA PROCESSOR INTERFACE TEST



G.W.A.
2-24-71