The attached unscheduled ATM covers the functional description of the Data Processor.

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1.0 INTRODUCTION

The function of the Data Processor (DP) is to collect data from several sources, including scientific experiments, and prepare the data for transmission to earth. To accomplish this the DP must generate the telemetry format, synchronizing signals, (known as control words) for use at the earth decoding station, and supply timing signals to the various experiments so that experimental data may be presented to the DP at the proper time. It is also required that the DP shall operate in three modes, so that optimum data reception is available at all times. The output from the data processor is a "split phase modulated data" signal which is presented directly to the transmitter modulation input.

The DP has been designed for additional high reliability by including a high degree of redundancy. For practical purposes there are two DP (X and Y Units) contained within the one unit with only one operating at any given moment. See Figure 1. (A more detailed block diagram is shown in attached drawing BSX 3167.)

2.0 DESCRIPTION

As may be seen in Figure 1, the DP consists of two essentially identical units either of which may accept data and deliver it to either transmitter. A more detailed block diagram is shown on the attached drawing BSX-3167.

The DP has been designed for a high degree of flexibility in terms of its ability to handle data from the various combinations of experiments while maintaining simplicity of logic and over-all function.

The following description is written as applying to one half of the DP. It also applies to the remaining half. The only item where this will not be true is the analog multiplexer, frame counter, and the DP-subsystem interface which are not duplicated. The overall data flow of the data processor is shown on the flow chart of Figure 2.

2.1 TIMING AND CONTROL CIRCUITS

The data processor is essentially a series of counters, gates and registers from which signals of succeeding time periods may be obtained. The basic clock is an oscillator of 169.6KHZ. This clock drives the master flip-flop (MFF) which divides the clock frequency down to 84.8 KHZ.

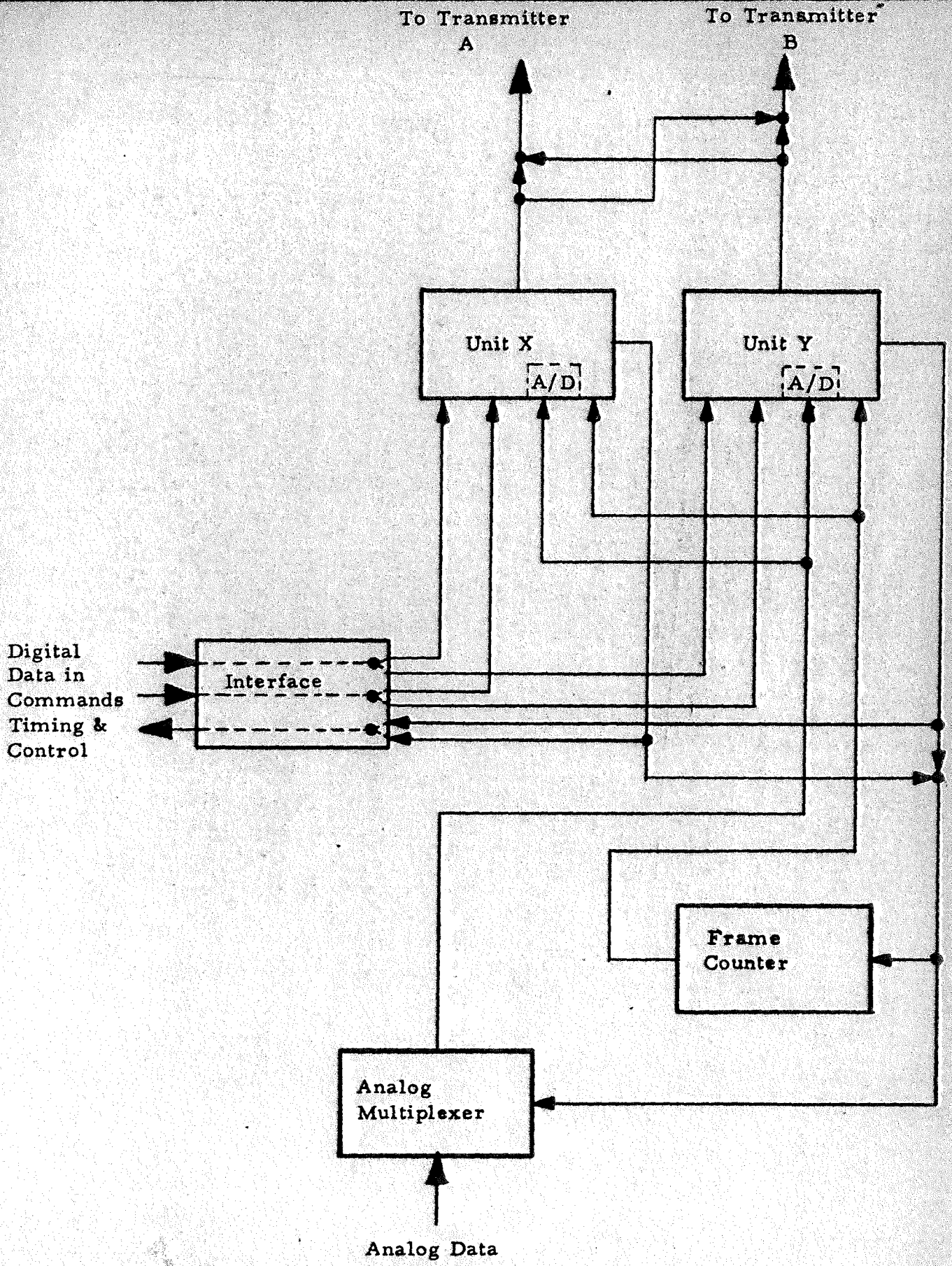
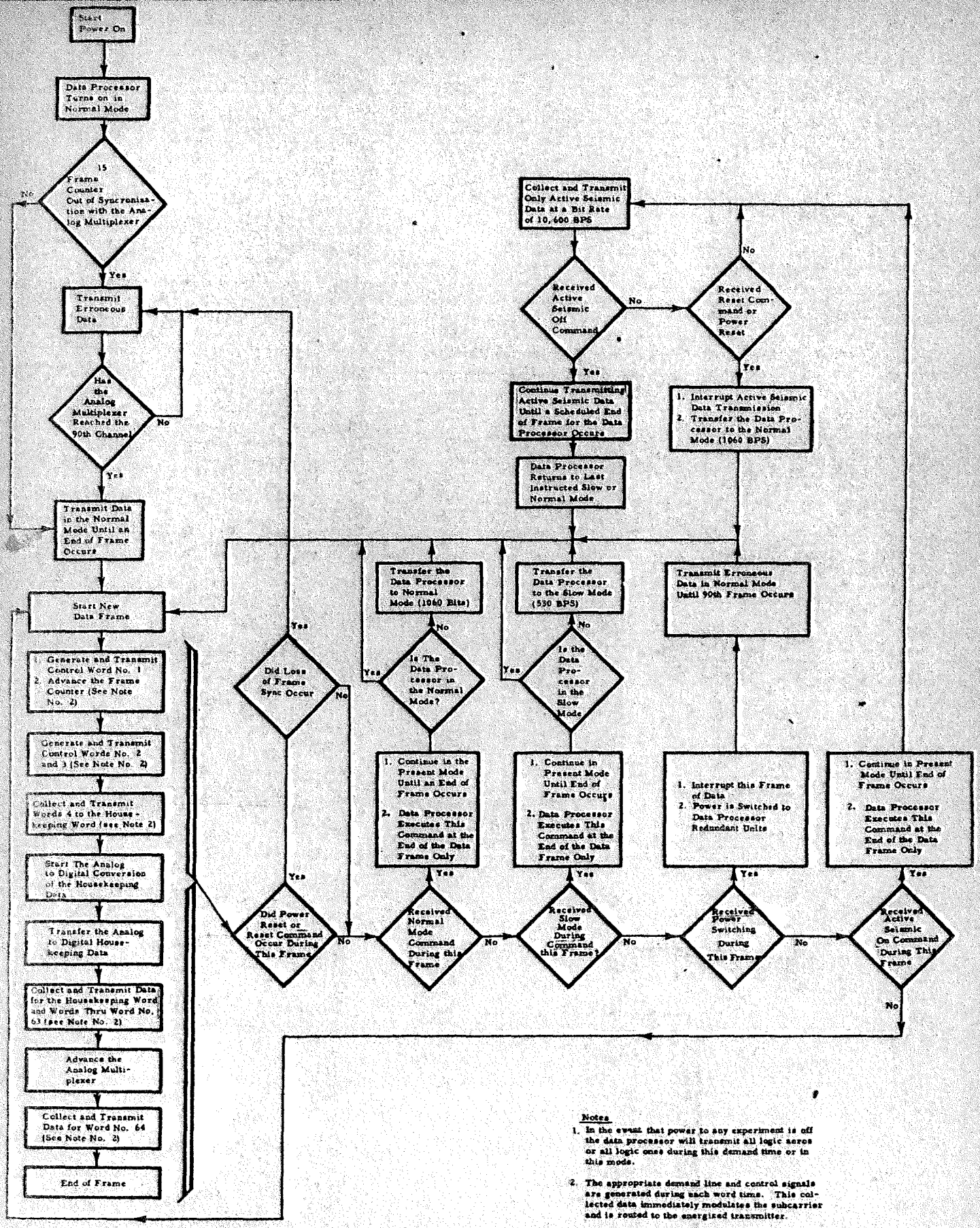

To Transmitter A
To Transmitter B
Unit X
A/D
Unit Y
A/D
Digital Data in
Commands
Timing & Control
Interface
Frame Counter
Analog Multiplexer
Analog Data

Figure 1



Notes

1. In the event that power to any experiment is off the data processor will transmit all logic zeros or all logic ones during this demand time or in this mode.
2. The appropriate demand line and control signals are generated during each word time. This collected data immediately modulates the subcarrier and is routed to the energized transmitter.

FIGURE 2

The MFF 84.8 KHZ signal drives the TM Counter which divides by eight so that a 10.6 KHZ signal is obtained. This signal is used in the "active seismic" mode to be discussed later. The signals of the TM counter with proper gating also produces a 42.4 KHZ signal to be used in the "slow data" mode.

The TT counter is a divide by ten counter driven by the 84.8 KHZ signal from the MFF or the 42.4 KHZ from the TM counter. The outputs from this counter are used to drive the sub-bit counter and the timing logic.

The sub-bit counter is a divide by eight counter with output frequencies of 1060 HZ or 530 HZ depending upon the operational mode. This output establishes the bit rate, drives the BT counter and provides timing signals for the timing logic.

The BT Counter is a divide by ten counter with an output frequency of 106 HZ or 53 HZ which establishes the word rate. Outputs of this counter are used in generating the control words and signal timing throughout the DP.

2.2 TELEMETRY FORMAT

The data processor formats the data collected from the experiments into a telemetry format as shown in Figure 3. The frame rate in the normal mode is 1 21/32 frames/sec. which means a complete frame of data is collected approximately every 0.6 sec. Each frame contains 64 words of 10 bits each giving 640 bits/frame. The basic bit rate is then 1060 bps.

In addition to the words assigned to the experiments, the first three 10 bit words are used as a 30 bit control word and a single 10 bit word is used for command verification purposes.

The bit assignments for the control word are shown in Figure 4. A 22 bit synchronization word consisting of an 11 bit Barker Code followed by the same code complemented is used. The next 7 bits provide frame identification for one thru ninty frames for correlation of analog multiplexer data. The 30th bit provides "normal" or "slow" mode information during the first two frames of the 90 frame sequence, and data processor serial number identification during the third thru fifth frames of the 90 frame sequence. For the sixth thru 90th frames the 30th bit has no information, and reads logic zero.

The multiformat commutator determines the specific assignments of each word within the telemetry format. Minor format changes are possible by simply changing jumpers in the commutator decoding assembly. Major format change would require a moderate design change in the commutator decoding assembly.

FIGURE 3

Array A Normal Configuration

	1	2	3	4	5	6	7	8
1	X	X	X	x	o	x	S	x
2	-	x	-	x	-	x	I	x
3	o	x	o	x	o	x	S	x
4	-	x	-	x	-	x	I	x
5	H	x	•	x	•	x	S	x
6	-	x	-	x	-	CV	I	x
7	o	x	o	x	o	x	S	I
8	-	x	-	x	-	x	I	x

Legend:

X = Control
x = Passive Seismic - Short period
\- = Passive Seismic - Long period seismic
• = Passive Seismic - Long period tidal and one temperature
o = Magnetometer
S = Solar Wind
I = Suprathermal Ion Detector

HF = Heat Flow
CP = Charged Particle Lunar Environment
CV = Command Verification
H = Housekeeping

Each box contains one 10 bit word
Total bits per frame = 10 x 64 = 640 bits

2.3 MULTIFORMAT COMMUTATOR AND DEMAND REGISTER

The multiformat commutator consist of two divide by eight counters in series and gates such that any of 64 consecutive periods may be gated out. The driving signal is obtained from logic made up of signals from the bit and sub-bit counters. Therefore, as the bit counter frequency is the same as the word rate, the commutator is advanced once each word.

The desired result of the commutator are signals one or more word lengths in duration so that data may be gated from the experiments and command decoder through the modulator and into the transmitter in a prescribed manner. These signals originate at the outputs of the decoder gates, and are presented to the inputs of the demand register.

The demand register provides the following functions: (1) is a memory for the demand signal while the commutator is being switched, (2) acts as a master switch turning off all demands while allowing the format generator and all control signals to function normally while in active seismic mode, and (3) act as a buffer between the demand decoder assembly eliminating any gating transients from the demand lines.

2.4 OPERATIONAL MODES

The DP is required to operate in three possible modes; normal mode, slow mode and active seismic mode. All mode to mode switching within the DP occurs at the end of the 64 word format which is in progress at the time the mode change-command is received.

2.4.1 Normal Mode

In the normal mode the data rate is 1060 bits per sec. which is 106 words per second. The demand signals to the data sources (experiments, e.c.) are one word in length, approximately 9.45 millisec. in duration. Other timing signals such as the data gate, and the various frame marks are approximately 118 μ sec. in duration.

2.4.2 Slow Mode

In the slow mode the DP operation is similar to the normal mode except that the date rate is 530 bits per second with 53 words per second. Also the demand and timing signals are changed to 18.90 millisec. and 236 μ sec., respectively.

2.4.3 Active Seismic Mode

Upon receiving the active seismic command from the command decoder the signal is stored until completion of the existing 64 word format. At the end of the 64th word the data processor switches into the active seismic mode. This may occur on either the even or odd frame, and between any analog words.

The effect of this switch is to gate off all demands to the command decoder and the various experiments and gate off any incoming serial data and control words except serial data from the active seismic experiment which is gated in by this switch. The data rate is now 10.6 KHZ rather than 1060 HZ

The data shift signal, frame mark, even frame mark and data gate signals and 90th analog frames continue to be sent to the required experiments at the normal rate.

To summarize: The data processor is switched in such a manner that only the data inputs and data rate are affected. However, no demand signals will occur.

2.5 ANALOG MULTIPLEXER

The Analog Multiplexer is a 90 channel multiplexer which samples each of the analog inputs in a sequential manner to produce a Pulse Amplitude Modulated (PAM) Signal. It is designed to accept advance pulses from the Timing and Control Circuits within the particular Data Processor Unit which is energized. Likewise, its output will be available to both the A/D Converters, one in Unit X and the other in Unit Y. Only one A/D Converter will be energized. Advance pulses occurring once per frame advance the Analog Multiplexer to a new position after each A/D conversion. A block diagram of the multiplexer/converter is shown in figure 5.

2.6 A/D CONVERTER

The Analog to Digital Converter digitizes the PAM output signal from the Analog Multiplexer. A single 8-bit conversion is made every telemetry frame during the housekeeping word time period. The Timing and Control Circuits provide the necessary signals so the conversions are made at the appropriate time. The output data is then made available to the Digital Multiplexer in parallel data form.

2.7 CONTROL WORD GENERATOR

The Control Word Generator generates the synchronization code and provides the information to the Output Register during the proper bit times of the control word. Mode, frame, and data processor serial number are stored in flip-flops. This information is also provided to the Output Register at the appropriate bit times.

ANALOG MULTIPLEXER - ANALOG TO DIGITAL CONVERTER
SIMPLIFIED BLOCK DIAGRAM

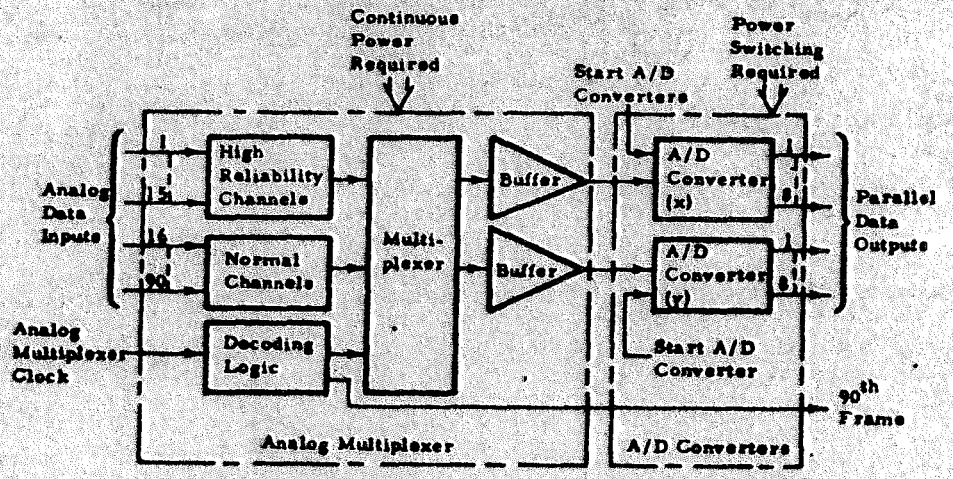


FIGURE 5.

2.8 DIGITAL MULTIPLEXER

The digital multiplexer consists of a ten bit, shift register which will accept eight parallel bits from the analog to digital converter or eight serial bits from the command decoder and shift them out serially in a 10 bit word with zeros inserted in the two most significant figures. The bits are shifted high order first.

Included in the digital multiplexer circuitry are gates which gate through serial input data directly from the experiments. The gate outputs and the 10 bit shift register outputs are 'or'd" together and presented to a two bit shift register which accepts either serial data from experiments or parallel control word coding.

2.9 OUTPUT REGISTER AND SPLIT PHASE DATA MODULATOR

The two bit shift register accepts serial experiment data and parallel control word data and presents the data in serial form to the 'split phase data modulator'. The modulator output frequency is the same as the data rate. The phase of the output is such that during a "one" bit of data a "one to zero" transition takes place and during a "zero" bit of data a "zero to one" transition takes place.

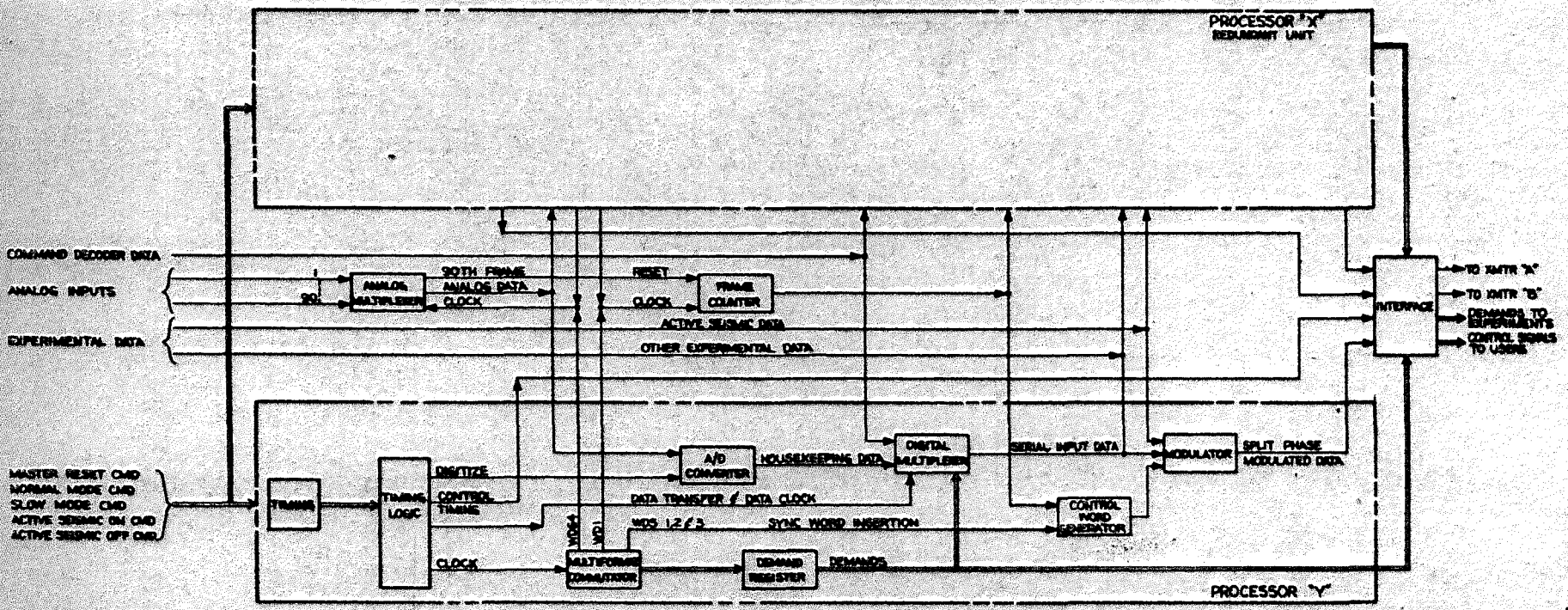
2.10 DATA PROCESSOR SYNCHRONIZATION

The design of the DP is such that all timing will be self synchronized in approximately 54 seconds after power turn on. A power reset circuit is designed into the circuits such that when power is turned on the DP starts in the "normal" mode. The 64 word format counters are fully synchronized in approximately 0.6 seconds. The analog multiplexer has no reset or initializing input, but it does have a 90th frame output. This output is used to reset the odd-even flip flop in the signal sync circuits and the frame counter, supplying frame count data to the third control word. See Figure 4.

The power reset circuit affects only the mode memory circuits and does not supply a reset to the various data processing counters which are fully self synchronus.

The power reset circuit design is such that it responds to power supply variations with durations as short as 200 nano seconds to essentially infinate duration. This is accomplished with logic devices and a voltage level detection circuit.

One consequence of this circuit is that a momentary loss of power supply voltage will result in a DP mode transfer from "slow" or "active seismic" modes to "normal" mode. However, such a power loss without the "power reset" circuit would result in an indeterment mode. The selection of the automatic return to the "normal" mode is dictated by the expectation that "normal" mode will be the primary mode of operation.



FUNCTIONAL BLOCK DIAGRAM
ALSEP DATA PROCESSOR

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