



**Aerospace
Systems Division**

Miley

Impact of Open Lines in Experiment
Cables

NO.

EATM-54

PAGE i

DATE 31 Jan

The purpose of this EATM is to answer the questions raised at the PSEP CDR regarding cutting the unused experiment cables. It is shown that there will be no impact on system performance as a result of cutting these unused cables.

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In order to convert the Data Subsystem of ALSEP Flight System 2 for use on the PSEP mission, it is planned to sever the three unused experiment cables at the locations shown in Figure 1 and the cable to the astronaut switches.

All the lines being cut are to be insulated from one another with the exception of the two lines from astronaut switch no. 1 (which are to be shorted together). It is the purpose of this memo to describe the impact of operating PSEP with these lines open. As can be seen in Figure 1, the circuits terminating in these cables can be classified in one of the following groups.

- Primary power circuits
- Digital synchronizing circuits
- Digital data circuits
- Control circuits

Note that no analog data input circuits are involved when experiments 2, 3 and 4 are deleted from ALSEP Flight Model 2. In the following paragraphs the effects on system operation of unloading each of these circuits are described.

a. Power Circuits

The power balance in the PSEP system is predicated on these lines being open-circuited. Hence, cutting these wires has no adverse effect; in fact, it is a design requirement that these lines be open-circuited. Consequently, it is important that the manner of insulating the ends of the wires in the severed cables (e.g. shrink tubing, etc.) guarantee wire-to-wire isolation under operating conditions. This is being accomplished with the shrink tubing on each wire.

b. Digital Synchronizing Circuits

The driving circuits in the Data Processor which provide the various timing and synchronizing pulses to the experiments have been designed to withstand both open-circuit and closed-circuit loading without permanent damage or functional effect. The verification of this design feature is provided by the fact



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that the timing lines to all 8 ALSEP experiments are brought to the central terminal strip and the Data Processor normally operates with 4 of the 8 experiment circuits open.

c. Digital Data Circuits

Any digital data lines which are open and not grounded will yield a digital "1" output in all bits. Although a digital "1" is normally indicative of a logic level of +2.5 to +5.5 volts at the digital data processor input, an open, ungrounded line will provide this kind of an input condition.

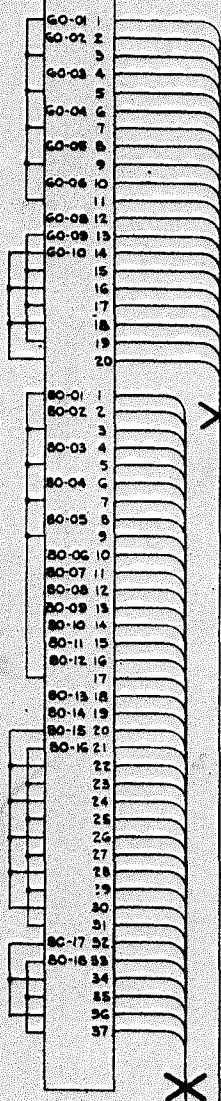
d. Control Circuits

The function of astronaut switches 2 and 3 is to simulate a specific set of commands to the Power Distribution Unit. Since the astronaut will not be performing this function on PSEP these cables can be deleted. The active state of a command is simulated by these switches by a momentary grounding of the appropriate command line(s). If these control lines from the switches are open-circuited, the function is effectively removed from the system.

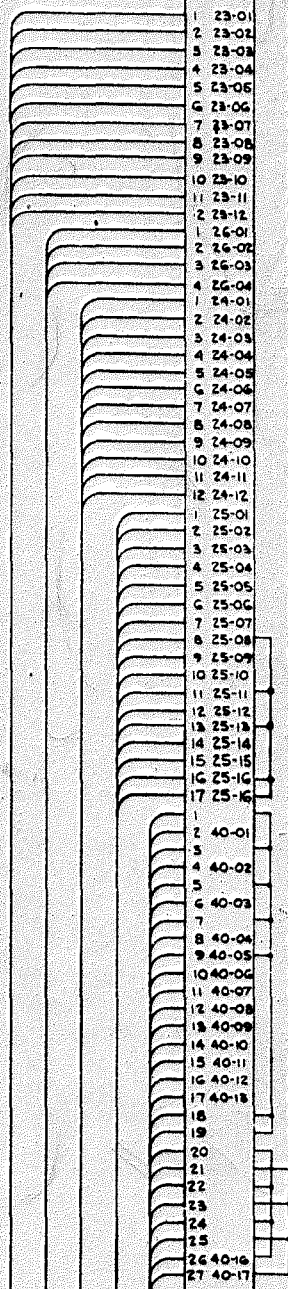
Conclusions

It is therefore evident from the above analysis that the operations of the Data Subsystem is unaffected by leaving the cables assigned to experiments 2, 3 and 4 and astronaut switches open-circuited. This conclusion has been verified many times during ALSEP system tests when the system has operated, with no adverse effects, with one or more experiments disconnected.

STANDBY
STANDBY POWER



NOTE 8
TERMINAL STRIP
NOTE 9



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PRIMARY STRUCTURE SIDE NO. 1 TEMP
PRIMARY STRUCTURE SIDE NO. 1 + SIG
PRIMARY STRUCTURE SIDE NO. 1 - SIG
PRIMARY STRUCTURE SIDE NO. 2 TEMP
PRIMARY STRUCTURE SIDE NO. 2 + SIG
PRIMARY STRUCTURE SIDE NO. 2 - SIG
PRIMARY STRUCTURE BOTTOM NO. 1 TEMP
PRIMARY STRUCTURE BOTTOM NO. 1 + SIG
PRIMARY STRUCTURE BOTTOM NO. 1 - SIG
PRIMARY STRUCTURE FRONT NO. 1 TEMP
PRIMARY STRUCTURE FRONT NO. 1 + SIG
PRIMARY STRUCTURE FRONT NO. 1 - SIG
INNER MULTILAYER INSULATION + SIG
INNER MULTILAYER INSULATION - SIG
OUTER MULTILAYER INSULATION + SIG
OUTER MULTILAYER INSULATION - SIG
SHUNT REGULATOR NO. 1
SHUNT REGULATOR NO. 1
SHUNT REGULATOR NO. 1 RETURN
SHUNT REGULATOR NO. 1 RETURN
SHUNT REGULATOR NO. 2
SHUNT REGULATOR NO. 2
SHUNT REGULATOR NO. 2 RETURN
SHUNT REGULATOR NO. 2 RETURN
POWER DISSIPATION LOAD NO. 1
PDM LOAD NO. 1 AND NO. 2 RETURN
POWER DISSIPATION LOAD NO. 2
MAGNETOMETER DUMMY LOAD (3 WATTS)
PHOTO CELL VOLTAGE NO. 1 + SIG
PHOTO CELL VOLTAGE NO. 1 - SIG
PHOTO CELL VOLTAGE NO. 2 + SIG
PHOTO CELL VOLTAGE NO. 2 - SIG
PHOTO CELL VOLTAGE NO. 3 + SIG
PHOTO CELL VOLTAGE NO. 3 - SIG
DUST DETECTOR NO. 1 TEMP
DUST DETECTOR NO. 1 RETURN
DUST DETECTOR CHASSIS GROUND
SUN SHIELD NO. 1 + SIG TOP SIDE
SUN SHIELD NO. 1 - SIG TOP SIDE
SUN SHIELD NO. 2 + SIG BOTTOM SIDE
SUN SHIELD NO. 2 - SIG BOTTOM SIDE
DUST DETECTOR TEMP NO. 2
DUST DETECTOR TEMP NO. 3
DUST DETECTOR TEMP NO. 3 RTN
DUST DETECTOR TEMP NO. 2 RTN
SHIELD
DIGITAL DATA
SHIELD
FRAME MARK
SHIELD
SHIFT
SHIELD
DEMAND
SHIELD RETURN
COMMAND NO. 83
COMMAND NO. 84
COMMAND NO. 85
COMMAND NO. 87
COMMAND NO. 89
COMMAND NO. 90
COMMAND NO. 91
COMMAND NO. 92
SHIELD
SHIELD

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NOTE 9

TERMINAL STRIP

MAGNETOMETER	J40
DUST DETECTOR AND SUN SHIELD	
17 LINES	J25
POWER DISSIPATION MODULE	
12 LINES	J24
THERMAL BAG	
4 LINES	J26
PRIMARY STRUCTURE	
12 LINES	J23
SOLAR WIND	
20 LINES	J60
SUPRATHINEL	ION DETECTOR
37 LINES	J48

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