This ATM summarizes the evaluation and conclusions on the false command verification word anomaly, octal 177 with parity, discovered during MSFN testing at KSC with the Qual SA (MSFN Test Model), EASEP, and ALSEP-1.

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DISCUSSION

1. The false CV word, octal 177 with parity, which represents eight 1's in the decoder output register, was observed following readout of a good CV word when MSFN was transmitting filler 1's between commands.

2. The anomaly was never observed during tests with the STS using filler 0's, and was not observed during a test with MSFN transmitting filler 0's. It was duplicated when the STS was modified to transmit filler 1's.

3. The use of an alternating bit pattern (0101) between commands from the STS produced 7 false CV's of octal 52 with parity, and 7 of octal 125 without parity. Monitoring of HK-14 showed no execution of the 052 commands.

4. Tests show that the false CV-177 occurs between 7 and 16 percent of the time at normal bit rate, and never occurs at low bit rate.

5. Analysis of circuit schematics indicates the problem to be a random action of the Data End Reset pulse at the end of readout of a normal command verification word. The duration of this pulse is so short that on occasion it is unable to clear the reset control. The logic is then set to generate a second CV word in the next downlink frame. The data in this second CV word will be the value of the uplink at the time the true CV word was shifted out, i.e., the filler bits.

6. The anomaly appears only following a good Command Verification and does not result in a faulty execution; therefore, it is not a potential operational hazard.

Enclosures:

A. Command Decoder - Reset Logic Operation.
B. Command Summary - MSFN Interface and Troubleshooting Tests at KSC.
C. Summary Results of Troubleshooting at BxA.

ENCLOSURE A

COMMAND DECODER - RESET LOGIC OPERATION

1. Overall Operation of the Command Decoder

The normal operation of the command decoder, i.e., with a good uplink and normal downlink data rate, can be considered as a sequence in which the logic cycles through four operating modes. These are:

a. Address search
b. Command execution
c. CV word read-out
d. Reset

The principal features of the logic operation in each of these modes will be described in brief below. During the address search, the uplink data is being clocked through a shift register, and the shift register contents are continuously tested by address recognition gates. Recognition of the address sets the Address Memory flip flop, and initiates the command execution mode.

A bit counter is enabled, at a preset count of 29. The counter permits the seven bit command complement and then the seven bit command to be clocked into the shift register, with the parity check logic testing the command. At a count of 29 + 14 = 43 shifting-in is stopped, the Command Execute line is enabled, and remains enabled for a further 20 incoming bits. If correct parity has been detected, the shift register contents, i.e., the command, is executed via decode gates. Note, however, that it is necessary for the count to be between 43 and 63, and that the Command Execute cannot be enabled under any other condition.

Detection of the count of 63 is used to set a flip flop to generate the Command Verification Enable. The counter continues to count uplink bits, and shifting remains disabled. Subsequently, at a time determined by the downlink, the data processor clocks the command data out of the shift register for downlink transmission. Data processor signals signifying the end of CV word read-out are used to generate Data End Reset.

The Data End Reset resets the command decoder by clearing the various flip flops which have been set during the address search, command execution, and CV word read-out modes, and also presets the uplink bit counter to 29.

The purpose of this memo is to provide a detailed description of the logic operation at reset, including an anomalous condition which permits a second CV word to be inserted into the downlink.

2. Command Decoder Reset

In the following description, gates and signals are identified by the nomenclature used on the BxA Command Decoder Logic Schematic Drawing Number 2332973. Particular reference should be made to sheets 2 and 3, Control Logic A and Decoder Programmer A. The four flip flops which are cleared on reset are:

D. P. Shift Pulses Enable A, G12 9B and G13 9A, sheet 2.
Reset Control A, G21 21B and G22 21A, sheet 2.
Command Verification Enable A, G4 13B and G5 13A, Sheet 2.
Address Memory A, FF 1, sheet 3.

The B side of the command decoder contains logic identical to the A side, so the description below is also applicable to the B side.

The first reset operation is clearing the D. P. Shift Pulses Enable A flip flop. The clear signal is Data End Reset, i.e. the output of G17 10A. To generate the clear signal at, and only at, the end of the CV word, the inputs to the G17 10A and gate are:

Data Gate - DG1ZP
Data Demand - DD1ZP and D. P. Shift Pulses Enable.

The Data End Reset is one of the inputs to an OR gate used to clear the Reset Control A flip flop. The output of the Reset Control A flip flop is in turn used to clear both the Command Verification Enable A and the Address Memory A flip flops, and to preset the counter to 29. This completes the reset of the command decoder logic to the address search mode.

3. The Second CV Word Reset Anomaly

There is a practical difficulty in implementing the reset actions described above, and this is to obtain a satisfactory waveform of the Data End Reset pulse.

As described above, in order to inhibit this signal unless the D. P. Shift Pulses Enable flip flop has been previously set, the output of the flip flop is used as one input to the G17 10A gate, and it is the output of the gate which is used to clear the flip flop. The result is that immediately following the end of the CV word, Data End Reset goes low to clear the flip flop, but as soon as the flip flop has cleared, i.e., D. P. Shift Pulses Enable goes low, then the G17 10A gate recloses and Data End Reset returns to a high level.

The result is that Data End Reset is low only for the transition time of the flip flop. Our interpretation of the generation of the second CV word, which has been recently observed and investigated, is that the Data End Reset pulse is so short that on occasion it is unable to clear the Reset Control Flip Flop. In this case the command decoder will be operating with the Command Verification Enable A and Address Memory A flip flops set, with the logic set to generate a second CV word in the next downlink frame.

The data in the second CV word will depend on value of the uplink present as the first, or true, CV word was shifted out. If the uplink trailer is all zeroes, then the shift register will be clear during the second CV word and there will be no way to detect its presence in the downlink. If the uplink trailer is all ones, then the 2nd CV will be 177_8 + parity. In practice, the uplink and downlink bit rates are so nearly the same that the eight bits of the downlink, (i.e., 7 bits + parity) will contain the uplink trailer, as has been verified by test using a one-zero pattern.

COMMAND SUMMARY - MSFN INTERFACE AND TROUBLESHOOTING TESTS AT KSC

Test / Summary	. April 10 . MSFN Interface . Qual SA-MILA	. May 2 . RF Test . Qual SA-MILA	. May 5 . RF Phase and CV 177 T/S test . Qual SA-MILA	. May 7 . MSFN Interface . EASEP-MILA
No. of GMIL Commands	46	12	118	59
No. of Command Verifications	15	4	110	51
No. of CV 177 Anomalies	1 *	1	16	3
No. of Rejects		2 S/C		
Comments	*. CV 177 normal- due to sync loss during switch-over . GMIL 20 DB RF loss	. GMIL RF phasing . CV177 anomaly . CMD test matrix . DR #0100	. CMD test matrix . CV 177 anomaly	CMD test matrix . CV177 anomaly . Test successful

ENCLOSURE B

ENCLOSURE B (continued)

COMMAND SUMMARY - MSFN INTERFACE AND TROUBLESHOOTING TESTS AT KSC

Test / Summary	. May 7 . CV 177 T. S. Test . Qual SA-MILA	. May 9 . MSFN Interface . ALSEP-1 - MILA	. May 10 . CV177 T. S. Test . Qual SA - MILA
No. of GMIL Commands	81	81	53
No. of Command Verifications	67	53	50
No. of CV 177 Anomalies	7	16	
No. of Rejects	2	2 S/C 1 ground (Re-transmit O. K.)	
Comments	. CMD test Matrix . CV177 anomaly . GMIL Malfunction	. CMD test Matrix . CV177 anomaly . Rejects no concern . Test successful	. CMD test Matrix . GMIL CMD with trailing 0's . No anomalies

ENCLOSURE C

SUMMARY RESULTS OF TROUBLESHOOTING AT BXA

Test	Date	False/Total	%	CMD	False CV	Trailer	Data Rate	Synch	Address	Data Proc.
1	5/19	7/50	14	174	177	ones	Normal	yes	25-2A 25-2B	20-X 30-Y
2	5/20	12/126	10	Test	177	ones	Normal	yes	2B	Y
3	5/20	14/100	14	174	7-052* 7-125	1010	Normal	yes	2B	Y
4**	5/20									
5	5/20	0/126	0	Test	None	ones	Low	yes	2B	Y
6	5/20	7/100	7	174	177	ones	Normal	No	2B	Y
7-	5/20	16/126	13	Test	177	ones	Normal	yes	2A	Y
8	5/20	17/126	14	Test	177	ones	Normal	yes	2B	Y
9	5/20	14/126	11	Test	177	ones	Normal	yes	2B	X
10	5/20	15/126	12	Test	177	ones	Normal	yes	2A	X

* The octal 052 false CV's were not executed; Verified via HK-14

** Test 4 was run with various modulation values to verify the specifications for MSFN