



**Aerospace  
Systems Division**

Reliability Failure Mode,  
Effects and Criticality Analysis  
Addendum 3 ASE

NO.	ATM 501	REV. NO.	B-3
PAGE <u>1</u>		OF <u>3</u>	
DATE <u>8/6/71</u>			

This addendum updates ATM 501-B ASE by:

1. Replacement of the old 16 Channel MUX FMECA work sheets, pages 3.9.49;50; and 51 (3 pages) with nine new FMECA work sheets. This change is a result of change to a new BxA supplied MUX. See Attachment I. The new MUX FMECA is also called out in ATM 912 dated 8/20/70.
2. Addition of four (4) FMECA work sheets to Section 3.9 to cover EMI modifications. These sheets are also found in ATM 840 dated 11/5/69. See Attachment II.
3. Addition of one FMECA work sheet to Section 3.9 to cover changes in the Central Station. See Attachment III.

The FMECA work sheet in Attachments I, II, and II are to be added to ATM 501-B as indicated.

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## 1.1 INTRODUCTION

This analysis is detailed at the Active Seismic Experiment electronic modification level for Array D as a supplement to the ALSEP Failure Mode, Effects, and Criticality Analysis, ATM 501B. ATM 501B includes the ASE Failure Mode, Effects and Criticality Analysis at the experiment and sub-system level. Each potential failure is considered in light of the probability of occurrence, failure mode distribution and its effect on experiment success.

## 1.2 PURPOSE

The purpose of this supplement is to update the failure mode, effects, and criticality analysis of modifications made to the ASE/CSE for Array D.

## 1.3 ASE/CSE MODIFICATIONS

The following ASE/CSE modifications have been incorporated into the Active Seismic Experiment for Array D.

- A. Use of BxA 16 Channel Mux and A/D converter (see enclosure 1).
- B. The 16 channel EMI modification included the following:
  - (1) Added capacitor C10 (.01 $\mu$ F) to A/D converter board No. 1 for filtering.
  - (2) Changed R1 (2.7 $\Omega$ /4w) to L1 (100  $\mu$ hy) choke to reduce ripple on A/D converter board No. 2.
  - (3) Added capacitor C11 (470 pfd) to A/D Converter Analog Assy for filtering.
- C. The ASE/CSE Thumper RTE Initial Revel Modification included the following:
  - (1) Removal of capacitor C102 (22 pfd) used to preset flip flop.
  - (2) Added blocking diodes CR 102 and CR 103 (SM1N914).
- D. The EMI modifications specified in (enclosure 2) were made to the ASE prior to Array A-2.



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## 2.0 FAILURE MODES, EFFECTS & CRITICALITY ANALYSIS

The failure mode and effects analysis for the active Seismic Experiment modifications to Array D on a piece part level are documented in enclosure 3. The criticality ranking for those modifications contained in enclosure 3 are as follows:

### Criticality Ranking

I Loss of Experiment

II Degradation of Experiment

## 3.0 SINGLE POINT FAILURE SUMMARY

Five components have been added to the Array D ASE which would constitute loss of either the Thumper or ASE in the event of failure in the particular mode as specified in enclosure 1. Weight, power, and space constraints have ruled out the possibility of making these elements redundant. The probability of any of these devices failing in a single point failure mode is relatively insignificant when compared to the total number of single point failures already in the ASE.

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Attachment I

Remove from ATM 501-B the following FMECA work sheets:

Page 3.9.49  
3.9.50  
3.9.51

Replace with the attached new FMECA work sheets:

Page 3.9.49.1  
3.9.49.2  
3.9.49.3  
3.9.50.1  
3.9.50.2  
3.9.50.3  
3.9.51.1  
3.9.51.2  
3.9.51.3

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# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM	ALSEP	PREPARED BY	R. J. Dallaire	NO.	ATM501	REV.	B-3
END ITEM	ASE/CE	DWG NO.	2346700	PAGE	3.9.45.1		
ASSY	16 Ch. MUX	DWG NO.	2346711	DATE	8/20/70		

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
			END ITEM	SYSTEM		
1.0 First Tier Channel Encoder	1.0 Failure as Shown Below	1.0 Electrical Failure	1.0 ASE MUX Affected as Shown	1.0 Output Affected as Shown	.00300	3
	1.1 One First Tier MOS FET Gate in Each of the Four MOS-FET Chips is Always "On".	1.1 Output of SN54L20 Fails High	1.1 (3 of 4 Channels of each First Tier MOS FET Chip will be Lost	1.1 Loss of 12 Channels		
	1.2 One First Tier MOS FET Gate in Each of the Four MOS-FET Chips is Always "Off".	1.2 Output of SN54L20 Fails Low	1.2 One Channel From each First Tier MOS Chip Lost	1.2 Loss of 4 Channels		
	1.3 First Tier MOS FET Gate Always "Off".	1.3 Input Fails Open or Short	1.3 One Channel From each First Tier MOS Chip Lost	1.3 Loss of 4 Channels		
2.0 Second Tier Channel Encoder	2.0 Failure as Shown Below	2.0 Electrical Failure	2.0 ASE MUX Affected as Shown	2.0 Output Affected as Shown	.00300	3
	2.1 Second Tier MOS FET Gate Always "On"	2.1 Output of SN54L20 Fails High	2.1 3 of 4 First Tier MOS Chip Lost	2.1 Loss of 12 Channels		
	2.2 Second Tier MOS FET Gate Always "Off"	2.2 Output of SN54L20 Fails Low	2.2 One First Tier MOS Chip Lost	2.2 Loss of 4 Channels		
	2.3 Second Tier MOS FET Gate Always "Off"	2.3 Input Fails Open or Short	2.3 One First Tier MOS Chip Lost	2.3 Loss of 4 Channels		
3.0 First Tier MOS FET Gate Drivers	3.0 Failure as Shown Below	3.0 Electrical Failure	3.0 ASE MUX Affected as Shown	3.0 Output Affected as Shown	.00240	5
	3.1 Driven MOS FET Always "Off"	3.1 Driver Output Fails High	3.1 One Channel From each First Tier Chip Lost	3.1 Loss of 4 Channels		
	3.2 Driven MOS FET Always "On"	3.2 Driver Output Fails Low	3.2 3 of 4 Channels From Each First Tier Chip Lost	3.2 Loss of 12 Channels		

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM	ALSEP	PREPARED BY	R. J. Dallaire	N.	ATM501	REV.	B-3
END ITEM	ASE/CE	DWG NO.	2346700	PAGE	3.9.49.2		
ASSY	16 Ch. MUX	DWG NO.	2346711	DATE	8 20/70		

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
			END ITEM	SYSTEM		
4.0 Second Tier MOS FET Gate Drivers	4.0 Failure as Shown Below	4.0 Electrical Failure	4.0 MUX Affected as Shown	4.0 Output Affected as Shown	.00240	5
	4.1 Driven MOS FET Always "Off"	4.1 Driver Output Fails High	4.1 One First Tier MOS Chip Lost	4.1 Loss of 4 Channels		
	4.2 Driven MOS FET Always "On"	4.2 Driver Output Fails Low	4.2 3 of 4 First Tier Chips Lost	4.2 Loss of 12 Channels		
5.0 First Tier FET	5.0 Failure as Shown	5.0 Electrical Failure	5.0 MUX Affected as Shown	5.0 Output Affected as Shown	.00600	1
	5.1 Loss of a Gate on Chip	5.1 Short Source-Gate or Any Open	5.1 Loss of 1 Channel	5.1 Loss of 1 Channel		
	5.2 Loss of MX02D Chip	5.2 Short Drain-Substrate, Source-Substrate, Drain-Gate, or Gate-Substrate	5.2 Loss of 4 consecutive Channels	5.2 Loss of 4 Channels		
	5.3 Loss of Other Gates on Chip	5.3 Short Drain-Source	5.3 Loss of 3 Consecutive Channels	5.3 Loss of 3 Channels		
	5.4 Loss of MX02D Chip	5.4 Short Drain-Substrate of Used Gates	5.4 Loss of 4 Consecutive Channels	5.4 Loss of 4 Channels		
6.0 Second Tier FET	6.0 Failure as Shown	6.0 Electrical Failure	6.0 MUX Affected as Shown	6.0 Output Affected as Shown	.00600	1
	6.1 Loss of Gate on Chip	6.1 Short Source - Gate or Any Open	6.1 Loss of every 4th channel	6.1 Loss of 4 Channels		
	6.2 Loss of MX02D Chip	6.2 Short Drain-Substrate, Source-Substrate, Drain Gate, or Gate-Substrate	6.2 Loss of all channels	6.2 Loss of all Channels		
	6.3 Loss of Other Gates on Chip	6.3 Short Drain-Source	6.3 Loss of All Channels	6.3 Loss of 12 Channels		
	6.4 Loss of MX02D Chip	6.4 Short Drain-Substrate of Unused Gates	6.4 Loss of All Channels	6.4 Loss of all Channels		

TABLE II

## FAILURE MODE, EFFECT &amp; CRITICALITY ANALYSIS

SYSTEM AISEP	PREPARED BY R. J. Dallaire	N. ATM501	REV. B-3
END ITEM ASE/CE	DWG NO. 2346700	PAGE 3.9.49.3	
ASSY A/D Conv.-Analog Brd	DWG NO. 2346710	DATE 8/20/70	

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^{-5}$	CRITIC- ALITY
			END ITEM	SYSTEM		
1.0 Oscillator- Clock	1.0 Oscillator Fails as Shown	1.0 Failure of Discrete Parts or Integrated Circuits	1.0 Clock Affected as Shown	1.0 Output Affected as Shown	.007313	2
	1.1 Oscillator Fails to Provide Output	1.1 Short or Open R1, R2, R3, R4 R5, C1, C2, Y1, or Failure of NG1A, NG1B, NG1C	1.1 Loss of Clock to Counters	1.1 Output will be Frozen		
	1.2 Oscillator Frequency Drift	1.2 Crystal (Y1) Parameter Drift	1.2 Counters Will Count at Wrong Speed	1.1 Output Slightly High or Low		
2.0 Input Buffer	2.0 Buffer Fails as Shown	2.0 Failure of I. C. or Capacitor as Shown	2.0 Analog Input Affected	2.0 Output Affected as Shown	.004507	4
	2.1 Loss of Input to Comparator	2.1 Short C4, Failed Output of LM102	2.1 Analog Input Appears High or Low	2.1 Output all 1's or 0's		
	2.2 Offset Input to Comparator	2.2 Input Offset Drift of LM102	2.2 Offset Input Voltage	2.2 Slight Error in Output		
	2.3 Noise to Input of Comparator	2.3 Open C4	2.3 Chance of Small Errors in Conversion	2.3 Occasional Error in Output		
3.0 Comparator (Compares Ramp Vol- tage to Analog Input Voltage)	3.0 Comparator Fails as Shown	3.0 Failure of Discrete Parts or I. C.'s	3.0 Ramp Comparison Affected	3.0 Output Affected as Shown	.004833	3
	3.1 Loss of Command Latch Signal	3.1 Open R5, R13, or short R6, C7, or failure of LM111, X5.	3.1 Counters Will Count Erron- eously	3.1 Output will be Random or All Zeros		
	3.2 Comparator Will Switch too Soon or too Late	3.2 LM111 Input Offset Drift	3.2 Count Will be Slightly too High or too Low	3.2 Output will be Slightly High or Low		
	3.3 Noise in Comparator	3.3 Open C5 or short R12	3.3 Chance Count Will be Low	3.3 Occasional Slightly Low Output		

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SYSTEM	ALSEP	PREPARED BY	R. J. Dallaire	NO	ATM501	REV.	B-3
END ITEM	ASE/CE	DWG NO.	2346700	PAGE	349.50.1		
ASSY	A/D Conv. - Analog Brd	DWG NO.	2346719	DATE	8/20/70		

## FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
			END ITEM	SYSTEM		
4.0 Ramp Generator	4.0 Ramp Generator Fails as Shown	4.0 Failure of Discrete Devices or I. C.	4.0 Ramp Generator Affected as Shown	4.0 Output Affected as Shown	.017864	1
	4.1 Ramp Generator Will Cease to Function	4.1 Open or Short R8, R9, R10, R11, R14, R15, C3, CR2, Q1 Open R7, or LM107 Failure	4.1 Counter Will Not Turn Off	4.1 Output Will Be Random		
	4.2 Incorrect Ramp Slope	4.2 Drift of CR2, R8, R9, R10, R11, C3, or Input Offset Drift of LM107	4.2 Counter Turned Off too Soon or too Late	4.2 Output Slightly High or Low		
	4.3 Excess Current in Zener CR1	4.3 Short R7	4.3 -12V Supply May Be Shorted	4.3 Possible Loss of A/D Converter (Will Cause PDU to Switch to Redundant A/D Converter)		
5.0 Power Supply Noise Suppression	5.0 On-Board Supplies Affected as Shown	5.0 Failure of Capacitors as Shown	5.0 On-Board Supplies Affected As Shown	5.0 Output Affected as Shown	.000804	5
	5.1 Loss of -12V or +5V Lines	5.1 Short C8 or C9	5.1 Loss of One MUX - A/D Conv.	5.1 Loss of One A/D Converter		
	5.2 Noise on +12V, -12, or 5V Lines	5.2 Open C6, C7, C8, or C9	5.2 Chance Erroneous Count	5.2 Occasional Output Error		
	5.3 Loss of +12V Line Capacitor	5.3 Short C6 or C7	5.3 No Effect Due to Redundant Capacitors	5.3 No Effect		
6.0 Thermistor Network	6.0 Thermistor Affected as Shown	6.0 Resistor Failures as Shown	6.0 Thermistor Readings Affected as Shown	6.0 A/D Converter Operation not Affected	.000335	6
	6.1 Improper Voltage Supplied to Thermistors	6.1 Open or Short R16, R7	6.1 Thermistor Readings Offscale High or Low	6.1 Thermistor Offscale High or Low		
	6.2 Drift in Voltage Supplied to Thermistors	6.2 Drift R16, R17	6.2 Thermistor Readings Slightly High or Low	6.2 Thermistor Slightly High or Low		



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END ITEM	ASE/CE	DWG NO.	2346719	PAGE	3.9.50.2		
ASSY	A/D Conv. - Digital Bnd	DWG NO.	2346722	DATE	8/20/70		

## FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
			END ITEM	SYSTEM		
1.0 Counter Control Circuitry	1.0 Counter Controls Fail as Shown	1.0 I.C. Failure	1.0 Counter Control Affected as Shown	1.0 Output Affected as Shown	.005900	2
	1.1 Counters Will Not Change States	1.1 Failure of NG1, NG2, H1A, H2A, H2B, H1C, X2	1.1 Loss of Control to Counters	1.1 Output Will be Random		
2.0 Counter Circuitry and Output Buffers	2.0 Counters or Buffers Fail As Shown	2.0 I.C. Failure	2.0 Counters and Buffers Affected as Shown	2.0 Output Affected as Shown	.009600	1
	2.1 Higher Order Stages Will Not Change States	2.1 Failure of X4 or X5	2.1 Higher Order Bits Frozen	2.1 Higher Order Bits Frozen		
	2.2 Counter "Over Count" When Analog Input is Over 5V	2.2 Failure of X6 High	2.2 When Analog Input is Over 5V Counters Will Recycle	2.2 An Analog Input of Greater than 5V will Digitally Read Less Than 5V, Analog Inputs Under 5V Will be Unaffected		
	2.3 Counters Stop Counting	2.3 Failure of X6 Low	2.3 Counters Will Stay at Zero After Reset	2.3 Output Always Read Zeros		
	2.4 One Output Bit Always High or Low	2.4 Failure of Buffer Gate High or Low	2.4 One Bit Erroneous, Other 7 Will Be Okay	2.4 One Bit Erroneous		
3.0 Voltage Supply Noise Suppression	3.0 Noise Suppressor Fails as Shown	3.0 Discrete Parts Failure	3.0 Digital Circuitry Affected as Shown	3.0 Output Affected as Shown	.005210	3
	3.1 Loss of +5V to Board	3.1 Open R1 or Short C1	3.1 Digital Circuitry Will Cease to Function	3.1 Outputs Will Appear to be All Ones		
	3.2 Noise on +5V Line	3.2 Open C1 or Short R1	3.2 Chance Erroneous Count	3.2 Output Occasionally Erroneous		

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SYSTEM	ALSEP	PREPARED BY	R. J. Dallaire	NO.	ATM501	REV.	B-3
END ITEM	ASE/CE	DWG NO.	2346700	PAGE	3.9.50.3		
ASSY	16 Ch. Multiplexer	DWG NO.	2346711	DATE	8/20/70		

## FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

PART/COMPONENT SYMBOL	FAILURE MODE (Q)	EFFECT OF FAILURE		FAILURE PROBABILITY Q x 10 <sup>3</sup>	CRITICALITY
		ASSEMBLY	END ITEM		
1.0 First Tier Channel Encoders (SN54L20)	1.1 Output of SN54L20 Fails High (.400)	1.1 One First Tier MOS FET Gate in Each of the Four MOS-FET Chips is Always "On".	1.1 Loss of 12 Channels, (3 of 4 Channels of each First Tier MOS FET Chip will be Lost)	.0012	1**
	1.2 Output of SN54L20 Fails Low (.400)	1.2 One First Tier MOS FET Gate in Each of the Four MOS-FET Chips is Always "Off".	1.2 Loss of 4 Channels, (One Channel From Each First Tier MOS Chip)	.0012	1
	1.3 Input Fails Open or Short (.200)	1.3 First Tier MOS FET Gate Always "Off".	1.3 Loss of 4 Channels (One Channel From Each First Tier MOS Chip)	.0006	2
2.0 Second Tier Channel Encoders (SN54L20)	2.1 Output of SN54L20 Fails High (.400)	2.1 Second Tier MOS FET Gate Always "On"	2.1 Loss of 12 Channels (3 of 4 First Tier MOS Chips)	.0012	1**
	2.2 Output of SN54L20 Fails Low (.400)	2.2 Second Tier MOS FET Gate Always "Off"	2.2 Loss of 4 Channels (One First Tier MOS Chip)	.0012	1
	2.3 Input Fails Open or Short (.200)	2.3 Second Tier MOS FET Gate Always "Off"	2.3 Loss of 4 Channels (One First Tier MOS Chip)	.0006	2
3.0 First Tier MOS FET Gate Drivers (DM 7800)	3.1 Output Fails High (.500)	3.1 Driven MOS FET Always "Off"	3.1 Loss of 4 Channels (One Channel From Each First Tier Chip)	.0012	1
	3.2 Output Fails Low (.500)	3.2 Driver MOS FET Always "On"	3.2 Loss of 12 Channels (3 of 4 Channels From Each First Tier Chip)	.0012	1**
4.0 Second Tier MOS FET Gate Drivers (DM7800)	4.1 Output Fails High (.500)	4.1 Driver MOS FET Always "Off"	4.1 Loss of 4 Channels (One First Tier MOS Chip)	.0012	1
	4.2 Output Fails Low (.500)	4.2 Driver MOS FET Always "On"	4.2 Loss of 12 Channels (3 of 4 First Tier Chips)	.0012	1**

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

SYSTEM	ALSEP	PREPARED BY	R. J. Dallaire	NO	ATM501	REV	B-3
END ITEM	ASE/CE	DWG NO.	2346700	PAGE	3.9.51.1		
ASSY	16 Ch. MUX	DWG NO.	2346711	DATE	8/20/70		

PART/COMPONENT SYMBOL	FAILURE MODE ( $\alpha$ )	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^5$	CRITIC- ALITY
		ASSEMBLY	END ITEM		
5.0 First Tier MOS FET (MX02D)	5.1 Short Source-Gate or Any Open (.373)	5.1 Loss of a Gate on Chip	5.1 Loss of 1 Channel	.00317	1
	5.2 Short Drain-Substrate, Source - Substrate, Drain-Gate, or Gate- Substrate (.213)	5.2 Loss of MX02D Chip	5.2 Loss of 4 Channels	.00181	2
	5.3 Short Drain-Source (.080)	5.3 Loss of Other Gates on Chip	5.3 Loss of 3 Channels	.00068	3
	5.4 Short Drain-Substrate of Unused Gates (.040)	5.4 Loss of MX02D Chip	5.4 Loss of 4 Channels	.00034	4
6.0 Second Tier MOS FET (MX02D)	6.1 Short Source - Gate or Any Open(.373)	6.1 Loss of Gate on Chip	6.1 Loss of 4 Channels	.00317	1
	6.2 Short Drain-Substrate, Source- Substrate, Drain-Gate, Drain- Gate, or Gate-Substrate (.213)	6.2 Loss of MX02D Chip	6.2 Loss of All Channels	.00181	2*
	6.3 Short Drain-Souce (.080)	6.3 Loss of Other Gates on Chip	6.3 Loss of 12 Channels	.00068	3**
	6.4 Short Drain-Substrate of Unused Gates (.040)	6.4 Loss of MX02D Chip	6.4 Loss of All Channels	.00034	4*
		<p>* Single Asterisk Denotes Loss of All 16 Channels.</p> <p>** Double Asterisk Denotes Loss 12 Channels Which Implies the Loss of More than One Geophone Channel.</p> <p>Only Criticality Numbers Having Asterisks are Termed "Serious Failure Modes".</p>			

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END ITEM	ASE/CE	DWG NO.	2346700	PAGE	3-9-51-2		
ASSY	A/D Conv. Analog Brd	DWG NO.	2346719	DATE	8/20/70		

## FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

PART/COMPONENT SYMBOL	FAILURE MODE ( $\alpha$ )	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^3$	CRITICALITY
		ASSEMBLY	END ITEM		
1.0 Oscillator Clock: R1, R2, R3, R4, R5, C1, C2, Y1, NG1A, NG1B, NG1C	1.1 Short or Open R1, R2, R3, R4, R5, C1, C2, Y1, or Failure of NG1A, NG1B, NG1C (.533)	1.1 Oscillator Will Fail to Provide Output	1.1 Loss of Clock to Counters	.004313	1
	1.2 Crystal (Y1) Drift (.371)	1.2 Oscillator Frequency Drift	1.2 Counters Will Count at Wrong Speed	.003000	2
2.0 Input Buffer: LM102, C4	2.1 Short C4, Output LM102 (.776)	2.1 Loss of Input to Comparator	2.1 Analog Input Appears High or Low	.003503	1
	2.2 Input Offset Drift (.193)	2.2 Offset Input to Comparator	2.2 Offset Input Voltage	.000870	2
	2.3 Open C4 (.030)	2.3 Noise to Input of Comparator	2.3 Chance of Small Errors in Conversion	.000134	3
3.0 Comparator: R12, R13, C5, LM111, X5	3.1 Open R12, R13, Short R13, C5; Failure of LM111, X5 (.798)	3.1 Loss of Command Latch Signal	3.1 Counters Will Count Erroneously	.004020	1
	3.2 LM111 Input Offset Drift (.140)	3.2 Comparator Will Switch too Soon or too Late	3.2 Count Will be Slightly too High or too Low	.000810	2
	3.3 Open C5, Short R12 (.002)	3.3 Noise in Comparator	3.3 Chance Count Will be Low	.000003	3
4.0 Ramp Generator: R7, R8, R9, R10, R11, R14, R15, C3, C12, Q1, LM107	4.1 Open or Short R8, R9, R10, R11, R14, R15, C3, CR2, Q1, Open R7, or Output Failure of LM107 (.442)	4.1 Ramp Generator Will Cease to Function	4.1 Counter Will Not Turn Off	.009248	1
	4.2 Drift of CR2, R8, R9, R10, R11 (.413)	4.2 Incorrect Ramp Slope	4.2 Counter Turned Off too Soon or too Late	.008631	2
	4.3 Short R7 (.001)	4.3 Excess Current in Zener CR1	4.3 -12V Supply May Be Shorted	.00003	3
5.0 Supply Noise Suppression C6, C7, C8, C9	5.1 Short C8, C9 (.070)	5.1 Loss of -12V or +5V	5.1 Loss of One MUX-A/D Converter	.000060	2
	5.2 Open C6, C7, C8, C9 (.798)	5.2 Noise on +12, -12, & +5V Lines	5.2 Chance of Erroneous Count	.000684	1
	5.3 Short C6, or C7 (.070)	5.3 No Effect Due to Redundant Capacitors	5.3 No Effect	.000060	2
6.0 Thermistor Network: R16, R17	6.1 Open or Short R16, R17 (.817)	6.1 Thermistors Not Supplied Proper Voltages	6.1 Incorrect Thermistor Outputs	.000274	1
	6.2 Drift R16, R17 (.183)	6.2 Thermistors Not Supplied Exact Voltages	6.2 Slight Error in Thermistor Outputs	.000061	2

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SYSTEM	ALSEP	PREPARED BY	R. J. Dallaire	NO.	ATM501	REV.	B-3
END ITEM	ASE/CE	DWG NO.	2338900	PAGE	3	9.51.3	
ASSY	A/D Conv. Digital Brd.	DWG NO.	2346722	DATE	8/20/70		

# FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

PART/COMPONENT SYMBOL	FAILURE MODE ( $\alpha$ )	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^5$	CRITIC- ALITY
		ASSEMBLY	END ITEM		
1.0 Counter Control Circuitry: NG1, NG2, H1A, H2B, H1C, X2	1.1 Any Failure of Digital Circuitry (1.00)	1.1 Loss of Control to Counters	1.1 Counters Will Not Change State	.005400	1
2.0 Counter Circuitry and Output Buffers: H2, H1E, H1F, X4, X5, X6	2.1 Failure of Any Stage in Counters (631)	2.1 Higher Order Stages Will Not Change States	2.1 Higher Order Bits Erroneous	.004800	1
	2.2 Failure of X6 High (.095)	2.2 Overvoltage Analog Input Will Allow Counters to Overcount	2.2 All Analog Inputs Over 5V Will Digitally Read Less Than 5V All Others Are OK	.000720	3
	2.3 Failure of X6 Low (.063)	2.3 Counters Will Stop Counting	2.3 Counters Will Stay At Zero After Reset	.000480	4
	2.4 Failure of Output Buffer Gate (.211)	2.4 One Bit Will Always Be High or Low	2.4 One Bit Will Be Erroneous All Others Will Be OK	.003600	2
3.0 Supply Decoupling: R1, C1	3.1 Open R1, Short C1 (.729)	3.1 Loss of +5V to Board	3.1 Outputs Will Appear to be All Ones	.000381	1
	3.2 Open C1, Short R1 (.267)	3.2 Noise on -15V Line	3.2 Chance Erroneous Count	.000140	2



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Reliability Failure Mode,  
Effects and Criticality Analysis  
Addendum 3 ASE

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Attachment II

Add to ATM 501-B the following new FMECA work sheets:

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3.9.88

FAILURE MODE, EFFECTS, AND CRITICALITY ANALYSIS WORKSHEET

NO. ATM501 REV. NO. B-3  
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ASSY FAILURE DESCRIPTION		RELIABILITY GOAL	SUPPLIER NAME	MISSION PHASE(S)	ASSY DWG OR SK REFERENCE		ORIGINATOR	DATE INITIAL REVISION	SUBSYSTEM NAME	ASSEMBLY NAME	
			Berry Electronics		P301-S F		P. McGinnis		Active Seismic Experiment	EMI Modifications	
PART, COMPONENT, UNIT, CIRCUIT ITEM, SET OR BOX DESCRIPTION	STATEMENT OF THE ASSUMED FAILURE	FAILURE MODE		EFFECT ON ASSEMBLY	SYSTEM EFFECT NUMBER (E)	FAILURE PROBABILITY $\times 10^5$ (Q)	DESIGN COMPENSATION TO ELIMINATE THE FAILURE MODE	PROBABILITY CRITICALITY PRODUCT $(\alpha) \times (E) \times (Q) \times 10^5$	RANK FOR ASSY	RELIABILITY MODEL CODE IDENTIFICATION	
Receiver sensitivity Limiting circuitry	Loss of series diode D6	Open	(0.300)	Degraded mortar impact data	0.010	4.900		0.01470	17		
		Short	(0.700)	Degraded mortar impact data	0.010	4.900		0.03430	15		
	Loss of parallel diode D7	Open	(0.300)	No effect	0.000	4.900		0.00000	21		
		Short	(0.700)	Loss of mortar impact data	0.046	4.900		0.15778	6		
	Loss of parallel capacitor C049	Open	(0.040)	Degraded mortar impact data	0.010	8.590		0.03436	14		
		Short	(0.960)	Loss of mortar impact data	0.046	8.590		0.35420	1		
Receiver Bandwidth Tracking Limiting Circuitry	Loss of diode D8	Open	(0.300)	Loss of one side of Bandwidth Limiting	0.010	4.900		0.01470	17		
		Short	(0.700)	Loss of mortar impact data	0.046	4.900		0.15778	6		
	Loss of resistor R20	Open	(0.090)	Loss of mortar impact data	0.046	9.500		0.03933	12		
		Short	(0.100)	Loss of one side of bandwidth limiting	0.010	9.500		0.00950	19		









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## FAILURE MODE, EFFECTS, AND CRITICALITY ANALYSIS WORKSHEET

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ASSY FAILURE DESCRIPTION	RELIABILITY GOAL	SUPPLIER NAME BxA	MISSION PHASE(S)	ASSY DWG OR SK REFERENCE 2334468J	ORIGINATOR	DATE INITIAL REVISION	SUBSYSTEM NAME	ASSEMBLY NAME	
PART, COMPONENT, UNIT, CIRCUIT ITEM, SET OR BOX DESCRIPTION	STATEMENT OF THE ASSUMED FAILURE	FAILURE MODE (a)	EFFECT ON ASSEMBLY	SYSTEM EFFECT NUMBER (E)	FAILURE PROBABILITY $\times 10^5$ (Q)	DESIGN COMPENSATION TO ELIMINATE THE FAILURE MODE	PROBABILITY CRITICALITY PRODUCT $(a) \times (E) \times (Q) \times 10^5$	RANK FOR ASSY	RELIABILITY MODEL CODE IDENTIFICATION
A/D Converter Output chokes	Loss of one of 8 output chokes	Open (0.563) Short (to gnd) (0.433)	Degraded data Loss of experiment	0.023 0.067	1.000 1.000		0.01295 0.03290	18 16	



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Attachment III

Add to ATM 501-B the following new FMECA work sheet:

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SYSTEM ALSEP Array D	PREPARED BY L. S. Moskowitz	NO. ATM501	REV. B-3
END ITEM ACTIVE Seismic	DWG NO.	PAGE 3. 9. 89 89	
ASSY Central Station	DWG NO.	DATE 7-27-71	

## FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

PART/COMPONENT SYMBOL	FAILURE MODE ( $\alpha$ )	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^5$	CRITIC- ALITY
		ASSEMBLY	END ITEM		
1.0 A/D Converter board No. 1					
C10	Open .10	Small increase in EMI noise	Degradation of ASE	.000000157	II
C10	Short .90	Pulls +5 volt line to ground	Loss of ASE	.00000141	I
2.0 A/D Converter board No. 2					
L1	Open .50	Loss of +5 volt line	Loss of ASE	.00000175	I
L1	Short .50	Small increase in EMI noise	Degradation of ASE	.00000175	II
3.0 A/D Converter analog assy					
C11	Open .10	Small increase in EMI noise	Degradation of ASE	.000000157	II
C11	Short .90	Pulls +5 volt line to ground	Loss of ASE	.00000141	I
4.0 ASE/CSE board A4					
CR102	Open .40	Could not reset F/F 19	Loss of thumper	.0000080	I
CR102	Short .60	Capacitor C5 would charge too quickly	Possible loss of thumper	.0000120	I
CR103	Open .40	Could not insure preset of F/F 19	Possible loss of thumper	.0000080	I
CR103	Short .60	Could result in excess current being sunk by 9041 gate	Probably no effect on experiment	.0000120	II