Bendix
Aerospace Systems Division

Dual A/D Converter Reliability Prediction And Failure Mode, Effects & Criticality Analysis	NO. ATM 905	REV. NO.
	PAGE 1 OF 13	
	DATE 7/23/70	

This ATM documents the Reliability Prediction and Failure Modes Effects & Criticality Analysis of the Bendix designed Dual A/D Converter. The analysis reflects the final flight configuration for the Array D ALSEP System.

Prepared by Rodney J. Dallaire
Rodney J. Dallaire
ALSEP Reliability Dept.

Approved by F. C. Fourbre for
S. J. Ellison
ALSEP Reliability Manager

1.0 INTRODUCTION

The results of the Reliability Prediction and the Failure Mode, Effects, & Criticality Analysis for the ALSEP Array D A/D Converter portion of the 90 Channel Multiplexer are documented in this report. This A/D Converter represents the Bendix Designed unit which makes extensive use of SSI and MSI integrated circuits. The A/D Converter was integrated with the Bendix Designed Dual 90 Channel Multiplexer.

The reliability prediction for a Single A/D Converter is 0.99622, which exceeds the specified goal of 0.9450. The resulting reliability prediction for the combined Dual 90 Channel Multiplexer and A/D Converter is 0.9987 for one year of lunar operation, which exceeds the specified design goal of .9956.

2.0 CIRCUIT DESCRIPTION

Figure 1 presents a Functional Block Diagram of the A/D Converter. This diagram is included to clarify the terms and discriptions given in the Failure Mode, Effects, & Criticality Analysis portion of this ATM (Tables II & III). The numbers in each box correspond to the Circuit/Function Item Number listed in the FMECA. Thus a clear picture may be obtained of the inter-relationships between Circuit Functions and Failure Mode Effects.

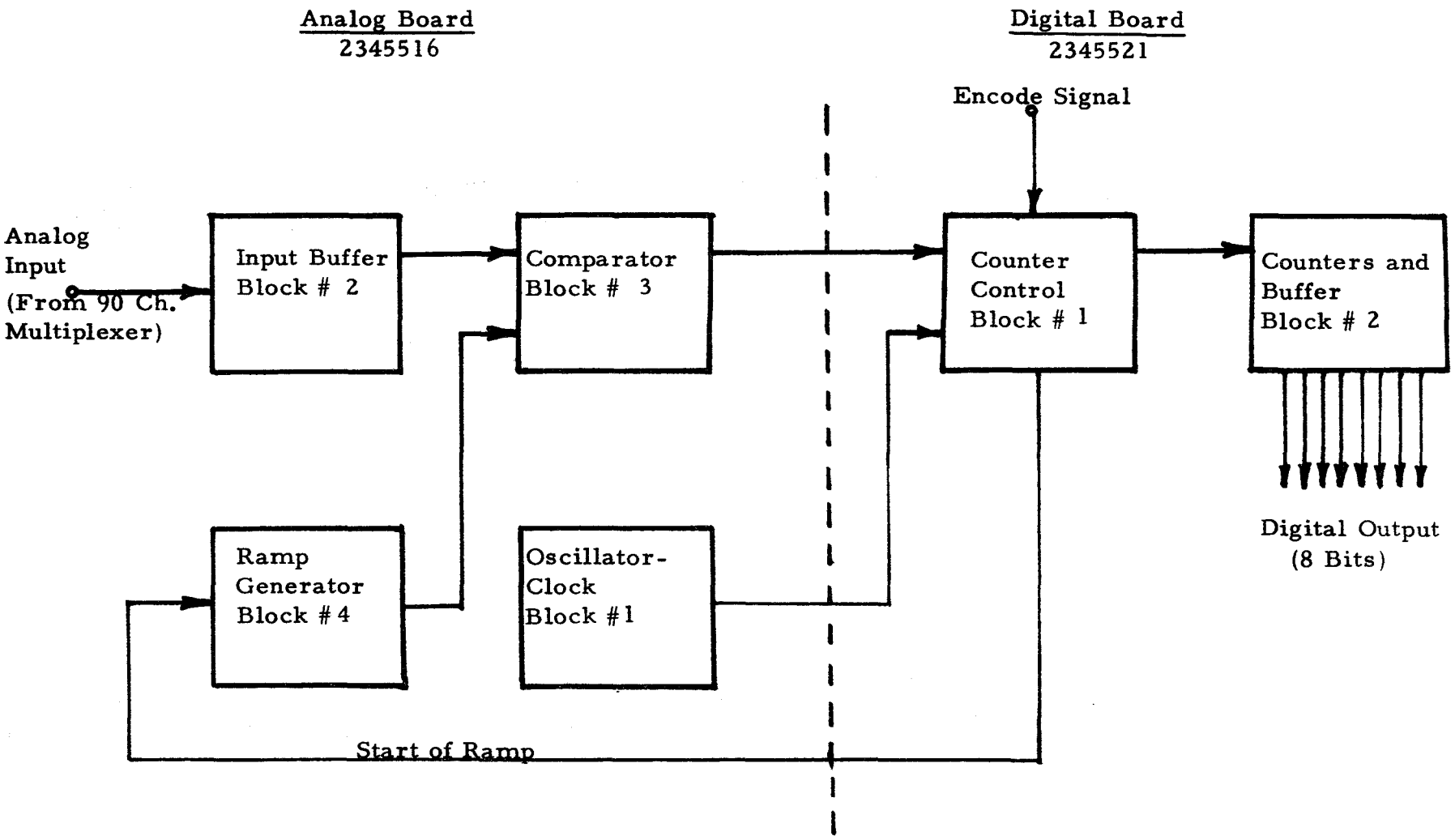
Briefly, the A/D Converter receives one of the 90 Housekeeping Data Channels from the 90 Channel Multiplexer in the form of an analog voltage. The buffer (Block 2) acts as a high impedance input for the purposes of non-loading the channel source and minimizing channel cross-talk. At the "Start of Conversion" signal, which is supplied by the data processor, a voltage ramp (Block 4) and a binary counter (Block 2, digital board) is started simultaneously by the counter control (Block 1, digital board). When the ramp voltage equals the analog input voltage, the comparator (Block 3, analog board) sends two signals, one to the counter control to stop the clock puslses to the counter, and the other to discharge the ramp. The binary output of the counters,then, is the digtial equivalent of the Housekeeping Channel voltage. This process is repeated for each new channel selected by the multiplexer.

3.0 RELIABILITY PREDICTION

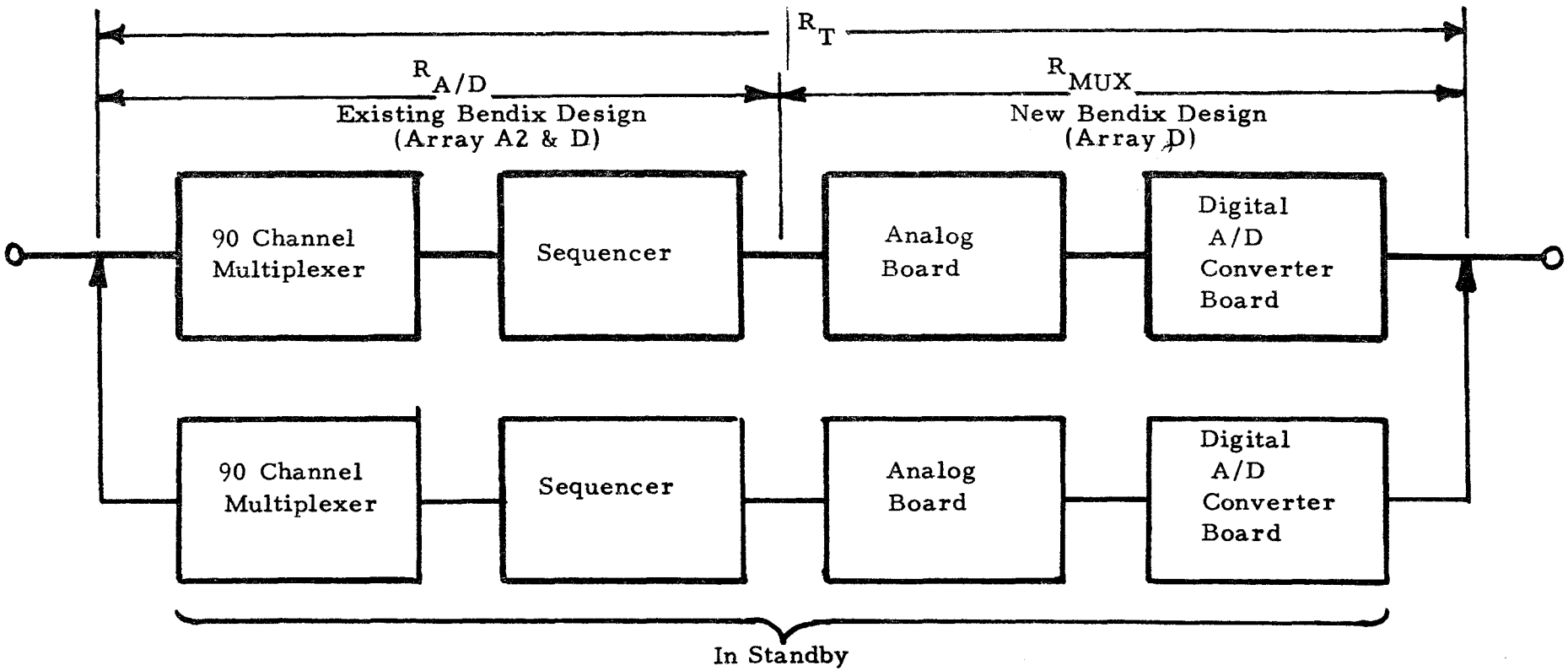
The reliability prediction for the Dual 90 Channel Multiplexer and A/D Converter, operating in standby redundant configuration is calculated to be 0.9987183 for launch, deployment, and one year of lunar operation. The predicted reliability exceeds the specified goal of 0.9956.

Figure 2 defines the Reliability Block Diagram and Mathematical Model for the Multiplexer and A/D Converter. The standby elements are activated by earth command. Functionally, the system operates in conjunction with the Data Processor. However, the Data Processor is was not included as part of this analysis.

The failure rates for each functional component identified in Figure 2 are tabulated in Table I. The failure rates shown represent composite totals derived from the part application stress ratios of each electronic piece part. The application reflects the anticipated "use" environment.



A/D Converter Block Diagram



Active System

$$R_{MUX} = \varepsilon^{-(\lambda 1 + \lambda 2)\, t}$$

$$R_{A/D} = \varepsilon^{-(\lambda_3 + \lambda_4)\, t}$$

$$R_A = R_{MUX} \cdot R_{A/D}$$

Complete System

$$R_T = 1 - \frac{\lambda a \lambda s t^2}{2} - \frac{\lambda a^2 \lambda t^2}{2}$$

DUAL 90 CHANNEL MULTIPLEXER & A/D CONVERTER
RELIABILITY BLOCK DIAGRAM & MATHEMATICAL MODEL

FIGURE 2

TABLE I

FAILURE RATE SUMMARY

Assembly	λi	ai (%/1000 Hrs.) Operating	si (%/1000 Hrs.) Standby	Failure Rate Source
90 Ch. Multiplexer				
90 Ch. MOS FET's	1	0.144500	0.0001445	ATM 860A
Sequencer	2	0.387611	0.0003876	ATM 860A
A/D Converter				
Analog Board	3	0.041753	0.0048953	ATM 904
Digital Board	4	0.001342	0.0000013	ATM 904
Totals	$\Sigma\lambda i$	0.575206	0.0054287	

Reliability Calculation

$$R_{MUX} = \epsilon^{-(0.53211 \times 10^{-5})(8760.52)} = \epsilon^{-0.046616} = 0.9544691$$

$$R_{A/D} = \epsilon^{-(0.043905 \times 10^{-5})(8760.52)} = \epsilon^{-0.037753} = 0.9962202$$

$$R_A = R_{MUX} \cdot R_{A/D} = (0.9544691\ (0.9962202) = 0.950861 \text{ (Active System)}$$

$$R_T = 1 - \frac{(0.575206)\ (0.0054287)\ (0.0876052)^2}{2} - \frac{[(0.575206)\ (0.0876052)]^2}{2}$$

$$R_T = 1 - \frac{(0.00002397)}{2} - \frac{(0.0025393)}{2} = 1 - 0.001198 - 0.0012697$$

$R_T = 0.9987183$ = Total MUX-Converter System Reliability Prediction

4.0 FAILURE MODES, EFFECTS & CRITICALITY ANALYSIS

The failure mode and effects analysis for the A/D Converter are documented in Tables II and III. Table II describes the functional failure modes and the resultant effects on the end item and system level. Table II delineates the failure modes at the piece part level. Each identified failure is numerically itemized for cross reference between Tables II and III, and Figure 1.

The failure probabilities reflect the identified line item. The criticality ranking lists by order of magnitude, the highest down to the lowest failure probabilities. Table II lists criticalities by circuit/function, while Table III lists the criticality sub-ranking within each circuit/function item. With this method, the highest order criticalities are easily identified both by circuit/function levels and by discrete part levels.

The format of Tables II and III is designed to provide the reader with a narrative description of the varying types of failures that could occur, combined with the resultant performance characteristics. This information is useful to system support in performing fault isolation should any anomally occur.

There are no ALSEP single point failures in either the 90 Channel Multiplexer or the A/D Converter. Careful parts selection and circuit design coupled with the switching of most supply voltages in the redundant units has enabled the Bendix design to have zero single point failures. Two single point failures were identified early in the design stage of the A/D Converter. These consisted of +12V noise suppression capacitors which, if failed shorted, would take the ALSEP +12 Volt supply down. These single point failures were eliminated in the finial design by removing one of the capacitors, and substituting a pair in series for the other.

There are also no single thread failure modes in the A/D Converter design. Complete functional ability may be restored by switching to the redundant unit. The two A/D Converters are completely independent.

The failure probability figures were derived using the data contained in ATM 904, the A/D Converter Parts Application Analysis. ATM 243 was used to derive the component α's (open, short, dirft, etc. apportionments). Some failure modes, such as drift of a resistor in a digital circuit, do not affect the operation. The failure modes which do not affect the operation are not included in the FMECA. For this reason the sum of α's for some circuit/function items do not equal one. However, all A/D Converter piece-part failure modes which do affect the operation of the A/D Converter or any other unit in ALSEP are included in the FMECA (Tables II and III).

Not all failure modes are serious. Where the effect of failure on the system is termed "output slightly erroneous", the digital value received on the ground can be adjusted to the correct value. This can be done by observing how the failure or drift has affected the calibration signals.

5.0 RELIABILITY ASSESSMENT

The purpose of performing a reliability prediction and failure modes analysis is to identify inherent design weaknesses. From the results of these analyses it has been concluded the reliability and design objectives have been fully satisfied.

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	R. J. Dallaire	ATM 905	
END ITEM	DWG NO.	PAGE	
90 C. MUX-A/D Conv.	2338900	9 of 13	
ASS'Y	DWG NO.	DATE	
A/D Conv.-Analog Brd	2345516	7/23/70	

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
			END ITEM	SYSTEM		
1.0 Oscillator-Clock	1.0 Oscillator Fails as Shown	1.0 Failure of Discrete Parts or Integrated Circuits	1.0 Clock Affected as Shown	1.0 Output Affected as Shown	.007313	2
	1.1 Oscillator Fails to Provide Output	1.1 Short or Open R1, R2, R3, R4, R5, C1, C2, Y1, or Failure of NG1A, NG1B, NG1C	1.1 Loss of Clock to Counters	1.1 Output will be Frozen		
	1.2 Oscillator Frequency Drift	1.2 Crystal (Y1) Parameter Drift	1.2 Counters Will Count at Wrong Speed	1.1 Output Slightly High or Low		
2.0 Input Buffer	2.0 Buffer Fails as Shown	2.0 Failure of I.C. or Capacitor as Shown	2.0 Analog Input Affected	2.0 Output Affected as Shown	.004507	4
	2.1 Loss of Input to Comparator	2.1 Short C4, Failed Output of LM102	2.1 Analog Input Appears High or Low	2.1 Output all 1's or 0's		
	2.2 Offset Input to Comparator	2.2 Input Offset Drift of LM102	2.2 Offset Input Voltage	2.2 Slight Error in Output		
	2.3 Noise to Input of Comparator	2.3 Open C4	2.3 Chance of Small Errors in Conversion	2.3 Occassional Error in Output		
3.0 Comparator (Compares Ramp Voltage to Analog Input Voltage)	3.0 Comparator Fails as Shown	3.0 Failure of Discrete Parts or I.C.'s	3.0 Ramp Comparison Affected	3.0 Output Affected as Shown	.004833	3
	3.1 Loss of Command Latch Signal	3.1 Open R5, R13, or short R6, C7, or failure of LM111, x 5.	3.1 Counters Will Count Erroneously	3.1 Output will be Random or All Zeros		
	3.2 Comparator Will Switch too Soon or too Late	3.2 LM111 Input Offset Drift	3.2 Count Will be Slightly too High or too Low	3.2 Output will be Slightly High or Low		
	3.3 Noise in Comparator	3.3 Open C5 or short R12	3.3 Chance Count Will be Low	3.3 Occasional Slightly Low Output		

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM	PREPARED BY	NO.	REV.
AILSEP	R. J. Dallaire	ATM905	
END ITEM: 90 C. MUX - A/D Conv.	DWG NO. 2338900	PAGE 10 of 13	
ASS'Y: A/D Conv. - Analog Brd	DWG NO. 2345516	DATE 7/23/70	

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
			END ITEM	SYSTEM		
4.0 Ramp Generator	4.0 Ramp Generator Fails as Shown	4.0 Failure of Discrete Devices or I.C.	4.0 Ramp Generator Affected as Shown	4.0 Output Affected as Shown	.017864	1
	4.1 Ramp Generator Will Cease to Function	4.1 Open or Short R8, R9, R10, R11, R14, R15, C3, CR2, Q1 Open R7, or LM107 Failure	4.1 Counter Will Not Turn Off	4.1 Output Will Be Random		
	4.2 Incorrect Ramp Slope	4.2 Drift of CR2, R8, R9, R10, R11, C3, or Input Offset Drift of LM107	4.2 Counter Turned Off too Soon or too Late	4.2 Output Slightly High or Low		
	4.3 Excess Current in Zener CR1	4.3 Short R7	4.3 -12V Supply May Be Shorted	4.3 Possible Loss of A/D Converter (Will Cause PDU to Switch to Redundant A/D Converter)		
5.0 Power Supply Noise Suppression	5.0 On-Board Supplies Affected as Shown	5.0 Failure of Capacitors as Shown	5.0 On-Board Supplies Affected As Shown	5.0 Output Affected as Shown	.000804	5
	5.1 Loss of -12V or +5V Lines	5.1 Short C8 or C9	5.1 Loss of One MUX - A/D Conv.	5.1 Loss of One A/D Converter		
	5.2 Noise on +12V, -12, or 5V Lines	5.2 Open C6, C7, C8, or C9	5.2 Chance Erroneous Count	5.2 Occasional Output Error		
	5.3 Loss of +12V Line Capacitor	5.3 Short C6 or C7	5.3 No Effect Due to Redundant Capacitors	5.3 No Effect		
6.0 Thermistor Network	6.0 Thermistor Affected as Shown	6.0 Resistor Failures as Shown	6.0 Thermistor Readings Affected as Shown	6.0 A/D Converter Operation not Affected	.000335	6
	6.1 Improper Voltage Supplied to Thermistors	6.1 Open or Short R16, R7	6.1 Thermistor Readings Offscale High or Low	6.1 Thermistor Offscale High or Low		
	6.2 Drift in Voltage Supplied to Thermistors	6.2 Drift R16, R17	6.2 Thermistor Readings Slightly High or Low	6.2 Thermistor Slightly High or Low		

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	R. J. Dallaire	ATM 905	
END ITEM: 90 Ch. MUX-A/D Conv.	DWG NO. 2338900	PAGE 11 of 13	
ASS'Y: A/D Conv.-Digital Brd	DWG NO. 2345521	DATE 7/23/70	

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE		FAILURE PROBABILITY Q x IC^{-5}	CRITICALITY
			END ITEM	SYSTEM		
1.0 Counter Control Circuitry	1.0 Counter Controls Fail as Shown	1.0 I.C. Failure	1.0 Counter Control Affected as Shown	1.0 Output Affected as Shown	.005900	2
	1.1 Counters Will Not Change States	1.1 Failure of NG1, NG2, H1A, H2A, H2B, H1C, X2	1.1 Loss of Control to Counters	1.1 Output Will be Random		
2.0 Counter Circuitry and Output Buffers	2.0 Counters or Buffers Fail As Shown	2.0 I.C. Failure	2.0 Counters and Buffers Affected as Shown	2.0 Output Affected as Shown	.007600	1
	2.1 Higher Order Stages Will Not Change States	2.1 Failure of X4 or X5	2.1 Higher Order Bits Frozen	2.1 Higher Order Bits Frozen		
	2.2 Counter "Over Count" When Analog Input is Over 5V	2.2 Failure of X6 High	2.2 When Analog Input is Over 5V Counters Will Recycle	2.2 An Analog Input of Greater than 5V will Digitally Read Less Than 5V, Analog Inputs Under 5V Will be Unaffected		
	2.3 Counters Stop Counting	2.3 Failure of X6 Low	2.3 Counters Will Stay at Zero After Reset	2.3 Output Always Read Zeros		
	2.4 One Output Bit Always High or Low	2.4 Failure of Buffer Gate High or Low	2.4 One Bit Erroneous, Other 7 Will Be Okay	2.4 One Bit Erroneous		
3.0 Voltage Supply Noise Suppression	3.0 Noise Suppressor Fails as Shown	3.0 Discrete Parts Failure	3.0 Digital Circuitry Affected as Shown	3.0 Output Affected as Shown	.00521	3
	3.1 Loss of +5V to Board	3.1 Open R1 or Short C1	3.1 Digital Circuitry Will Cease to Function	3.1 Outputs Will Appear to be All Ones		
	3.2 Noise on +5V Line	3.2 Open C1 or Short R1	3.2 Chance Erroneous Count	3.2 Output Occasionally Erroneous		

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	R. J. Dallaire	ATM 905	
END ITEM: 90 Ch. MUX-A/D Conv	DWG NO. 2338900	PAGE 12 of 13	
ASS'Y: A/D Conv. Analog Brd	DWG NO. 2345516	DATE 7/23/70	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-3}	CRITICALITY
1.0 Oscillator Clock: R1, R2, R3, R4, R5, C1, C2, Y1, NG1A, NG1B, NG1C	1.1 Short or Open R1, R2, R3, R4, R5, C1, C2, Y1, or Failure of NG1A, NG1B, NG1C (.533)	1.1 Oscilaltor Will Fail to Provide Output	1.1 Loss of Clock to Counters	.004313	1
	1.2 Crystal (Y1) Drift (.371)	1.2 Oscillator Frequency Drift	1.2 Counters Will Count at Wrong Speed	.003000	2
2.0 Input Buffer: LM102, C4	2.1 Short C4, Output LM102 (.776)	2.1 Loss of Input to Comparator	2.1 Analog Input Appears High or Low	.003503	1
	2.2 Input Offset Drift (.193)	2.2 Offset Input to Comparator	2.2 Offset Input Voltage	.000870	2
	2.3 Open C4 (.030)	2.3 Noise to Input of Comparator	2.3 Chance of Small Errors in Conversion	.000134	3
3.0 Comparator: R12, R13, C5, LM111, X5	3.1 Open R12, R13, Short R13, C5; Failure of LM111, X5 (.798)	3.1 Loss of Command Latch Signal	3.1 Counters Will Count Erroneously	.004020	1
	3.2 LM111 Input Offset Drift (.140)	3.2 Comparator Will Switch too Soon or too Late	3.2 Count Will be Slightly too High or too Low	.000810	2
	3.3 Open C5, Short R12 (.002)	3.3 Noise in Comparator	3.3 Chance Count Will be Low	.000003	3
4.0 Ramp Generatpr: R7, R8, R9, R10 R11, R14, R15, C3, C12, Q1, LM107	4.1 Open or Short R8, R9, R10, R11, R14, R15, C3, CR2, Q1, Open R7, or Output Failure of LM107 (.442)	4.1 Ramp Generator Will Cease to Function	4.1 Counter Will Not Turn Off	.009248	1
	4.2 Drift of CR2, R8, R9, R10, R11 (.413)	4.2 Incorrect Ramp Slope	4.2 Counter Turned Off too Soon or too Late	.008631	2
	4.3 Short R7 (.001)	4.3 Excess Current in Zener CR1	4.3 -12V Supply May Be Shorted	.00003	3
5.0 Supply Noise Suppression C6, C7, C8, C9	5.1 Short C8, C9 (.070)	5.1 Loss of -12V or +5V	5.1 Loss of One MUX-A/D Converter	.000060	2
	5.2 Open C6, C7, C8, C9 (.798)	5.2 Noise on +12, -12, & +5V Lines	5.2 Chance of Erroneous Count	.000684	1
	5.3 Short C6, or C7 (.070)	5.3 No Effect Due to Redundant Capacitors	5.3 No Effect	.000060	2
6.0 Thermistor Network: R16, R17	6.1 Open or Short R16, R17 (.817)	6.1 Thermistors Not Supplied Proper Voltages	6.1 Incorrect Thermistor Outputs	.000274	1
	6.2 Drift R16, R17 (.183)	6.2 Thermistors Not Supplied Exact Voltages	6.2 Slight Error in Thermistor Outputs	.000061	2

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

SYSTEM: ALSEP	PREPARED BY: R. J. Dallaire	NO.: ATM905	REV.
END ITEM: 90 Ch. MUX-A/D Conv.	DWG NO.: 2338900	PAGE 13 of 13	
ASSY: A/D Conv. Digital Brd.	DWG NO.: 2345521	DATE: 7/23/70	

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
1.0 Counter Control Circuitry: NG1, NG2, H1A, H2B, H1C, X2	1.1 Any Failure of Digital Circuitry	(1.00)	1.1 Loss of Control to Counters	1.1 Counters Will Not Change State	.005400	1
2.0 Counter Circuitry and Output Buffers: H2, H1E, H1F, X4, X5, X6	2.1 Failure of Any Stage in Counters	(.631)	2.1 Higher Order Stages Will Not Change States	2.1 Higher Order Bits Erroneous	.004800	1
	2.2 Failure of X6 High	(.095)	2.2 Overvoltage Analog Input Will Allow Counters to Overcount	2.2 All Analog Inputs Over 5V Will Digitally Read Less Than 5V All Others Are OK	.000720	3
	2.3 Failure of X6 Low	(.063)	2.3 Counters Will Stop Counting	2.3 Counters Will Stay At Zero After Reset	.000480	4
	2.4 Failure of Output Buffer Gate	(.211)	2.4 One Bit Will Always Be High or Low	2.4 One Bit Will Be Erroneous All Others Will Be OK	.001600	
3.0 Supply Decoupling: R1, C1	3.1 Open R1, Short C1	(.729)	3.1 Loss of +5V to Board	3.1 Outputs Will Appear to be All Ones	.000381	1
	3.2 Open C1, Short R1	(.267)	3.2 Noise on -15V Line	3.2 Chance Erroneous Count	.000140	2