Bendix
Aerospace Systems Division

NO.	REV. NO.
ATM-990	

Array E - LEAM Digital Interface
(54L Vs Amelco Logic)

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DATE 3/11/71

This ATM is in response to Array E Action Item 147 which requests BxA to examine 54L TTL-Amelco interface.

Prepared by: R. B. Wallace
R. B. Wallace

Approved by: D. Fithian
D. Fithian

SUMMARY

An analysis of the Array E Central Station-LEAM digital interface was made. Areas of concern noted, included:

a. The calculated worst case logical "0" noise margin for the 54L-Amelco TTL logic interface was 223 mv vs 340 mv for the 54L-54L interface.

b. A 1K ohm series resistor with a shunt zener diode was employed on each digital interface to protect the interface from overvoltage. The resistor reduces noise margin by 8% for the 54L-Amelco interface and would reduce noise margin by greater than 50% if employed in the 54L-54L interface.

c. Fan out of the shift clock line to a second Amelco 525 gate is allowed which reduces noise margin for this function to 196 mv for the logical "0" condition.

RECOMMENDATION

It is recommended that the LEAM interface be changed to provide the full margins of compatibility as that described in the ICS. Since the existing interface currently does meet the requirements of the ICS it is recommended that program impact be assessed prior to hardware implementation of this recommendation. The change is recommended because this interface is degraded by the necessity to employ experiment flat cables. These cables, because of their physical characteristics, couple more capacitive noise between signal lines than the normal ALSEP/experiment internal signal conductors. Every effort should therefore be taken to maximize noise margin. The interface changes requested include:

a. Use 54L04 hex inverters on all ALSEP digital interfaces including timing, control and command interfaces. This logic element is currently being employed elsewhere in the LEAM electronics and is the gate being used to interface with the 90th frame mark pulse in present design.

b. Remove the 1K ohm series impedance which reduces noise in propprtion to current demand on the logic line.

c. Restrict fanout as required in the ICS to one to minimize reduction in noise margin.

DETAILS

A summary of the Amelco and 54L logic levels, current requirements and noise margins are presented in Tables 1 thru 3. The main differences are:

a. The Amelco logic specifies limits in more detail than the 54L line. The Amelco logic has an apparent advantage in noise margin because of this. A review of the typical noise margins presented in Table 3 for the 54L line indicates however that the 54L logic vendors have been more conservative. The maximum noise margin for the 54L line of 400 mv is limited by the +125°C characteristic which indicates typically 650 mv exists. For other temperatures the 54L line typically improves by approximately a factor of 2 or better. Comparing the 125°C logic "0" noise limit with the Amelco logic limit of 350 mv shows the 54L line has a 50 mv advantage.

b. The Amelco logic consumes less power which achieves a power advantage over 54L. Voltage drops across series elements in the signal lines therefore are less of a factor for the Amelco interfaces.

c. The V_{INL} characteristic at 125°C for Amelco is specified at 550 mv compared to the 54L limit of 700 mv. Use of this limit is conservative since operation will typically not exceed 70°C. This parameter however reduces noise margin when 54L is used to interface with Amelco logic.

Figure 1 depicts the typical simplified schematic of the C/S-experiment interface. In the current LEAM design, all digital interfaces, including command lines are depicted as shown with the exception of the 90th frame mark timing signal and the digital data output line. Both of these signals use 54L logic elements to interface with the C/S and, the 1K ohm and zener are not employed on the digital output line. The manganin wire and flat cable losses are small and do not affect the interface characteristics significantly. The 330 ohm and 1K ohm resistors do affect the noise margin at the interfaces and are calculated in Table 4. The voltage V_1 represents logic levels which would be inputed to the LEAM interface in the event the 1K ohm resistor were removed as recommended. Using the worst case temperatures of -55° to +125°C noise margins were calculated. Noise margins for the typical 54L-54L interface was 340 mv minimum vs 223 mv for the 54L-Amelco interface. Noise margins for the shift clock lines would be reduced an additional 27 mv because of the fanout to an additional gate.

TABLE 1

AMELCO, 54L TTL AND ALSEP C/S LOGIC LEVELS

AMELCO	-55°C	+25°C	+125°C	Units
V_{OL}	250	200	200	mv
V_{INL}	800	800	550	mv
V_{OH}	2.4	2.7	2.5	v
V_{INH}	2.0	1.7	1.6	v
54L (TI or Nat'l)		-55° to +125°C		
V_{OL}	*	300	*	mv
V_{INL}	*	700	*	mv
V_{OH}	*	2.4	*	v
V_{INH}	*	2.0	*	v
Central Station Logic Levels				
V_{OL}	NA	400 Max	NA	mv
V_{IN}	NA	400 Max	NA	mv
V_{OH}	NA	2.4 Min	NA	v
V_{INH}	NA	2.4 Min	NA	v

*Not explicitly specified by 54L vendors.

TABLE 2

AMELCO AND 54L TTL CURRENT LIMITS

AMELCO	-55°C	+25°C	+125°C	Units
I_{INL}	37	26	20	μA
I_{INH}	6	4	6	μA
I_{OL}	300	260	160	μA
I_{OH}	60	60	100	μA
54L				
I_{INL}	*	180	*	μA
I_{INH}	*	100	*	μA
I_{OL}	*	2000	*	μA
I_{OH}	*	100	*	μA

*Not explicitly specified between extremes.

TABLE 3

AMELCO VS 54L TTL LOGIC NOISE MARGIN

AMELCO	-55°C	+25°C	+125°C	Units
Logical "0"	550	600	350	mv
Logical "1"	400	1000	900	mv
54L (TI or Nat'l) Guarantee		-55° to +125°C		
Logical "0"	*	400	*	mv
Logical "1"	*	400	*	mv
Typical 54L** Temp. Characteristics				
Logical "0"	1500	1200	650	mv
Logical "1"	1800	2400	3350	mv

*Not explicitly specified between extremes.
**Ref. TI Catalog CC201.

TABLE 4

CALCULATED NOISE MARGIN
54L-54L Vs 54L-Amelco

	54L-54L Interface	54L-Amelco Interface	Noise Margin 54L-54L	Noise Margin 54L-Amelco
Logical "1"				
V_1	2.367V	2.398	367 mv	398 mv
V_2 (With 1K)	2.267V	2.364	267 mv	364 mv
Logical "0"				
V_1	.360	.307	340 mv	243 mv
V_2 (With 1K)	.540	.327	160 mv	223 mv

Logical "1" input to LEAM = $V_2 = V_1 - I_{INH} R_2$

where $V_1 = 214 - I_{INH} R_1$

Logical "0" input to LEAM = $V_2 = V_1 + I_{INL} R_2$

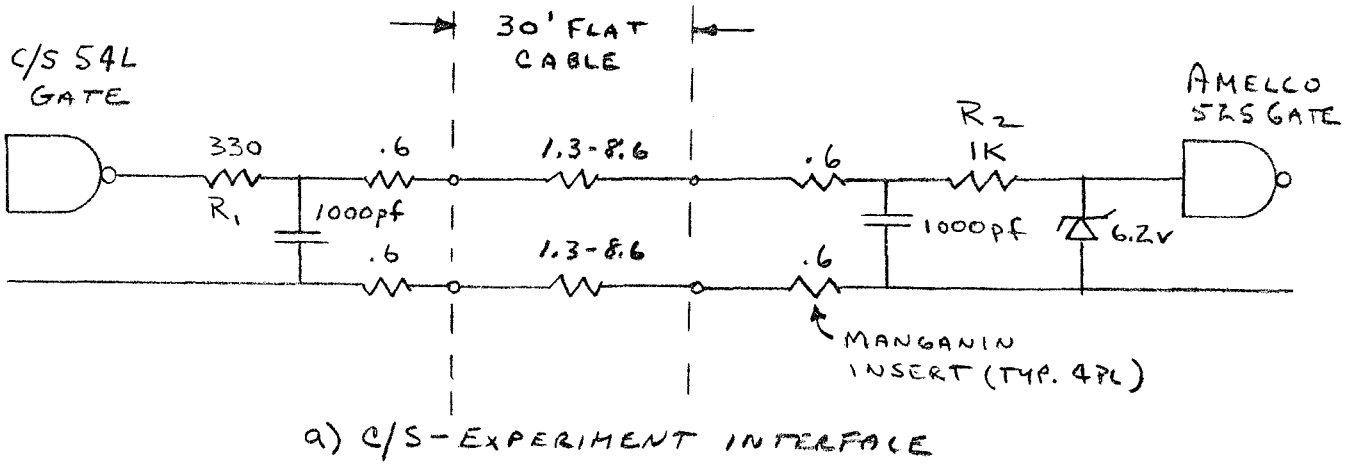
where $V_1 = 300 \text{ mv} + I_{INL} R_1$

Logic "1" Noise Margin = V_1 or V_2 - 2.0 V

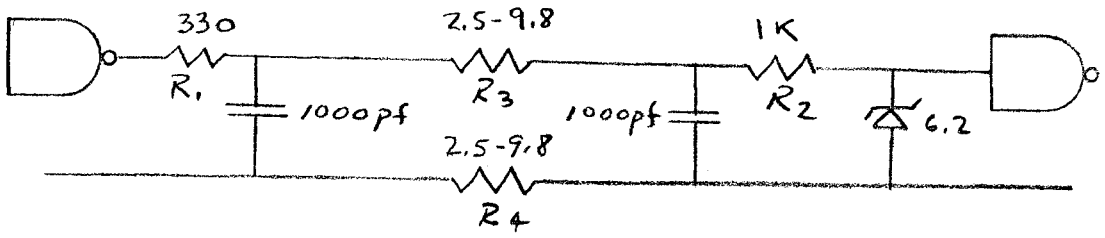
Logic "0" Noise Margin = 0.7V -(V_1 or V_2) for 54L-54L

= 0.55 - (V_1 or V_2) for 54L-Amelco

Note: V_1 = Input to LEAM without R_2, 1K ohm series resistance.



a) C/S - EXPERIMENT INTERFACE



b.) SIMPLIFIED INTERFACE

$R_3 + R_4 << R_1 + R_2$

Figure 1. Array E C/S - LEAM Digital Interface