ATM-618

JANUARY ENGINEERING MODEL TEST

PROGRESS REPORT

31 January 1967

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ILLUSTRATIONS.

TABLES

1.0 PROGRESS SUMMARY

This is the third monthly progress report on the ALSEP Engineering Model Systems Tests which covers the activities during the time period 1 January through 31 January 1967.

Category #2 tests have been completed on all the Array "A" experiments available (EM of SWE and PSE Central Station Electronics, and breadboards of LSM and SIDE/CCGE) and Category #2 tests are underway on CPLEE and ASE at the end of this report period. STS #1 was integrated with EM Central Station and operated successfully. RTG Mod 14 was integrated with the EM Central Station and operated well for 14 hours under varing load conditions.

The Central Station digital equipments continue to operate well. No significant faults have occurred in the command decoder or data processor. The power subsystem and PDU has also exhibited faultless operation during the report period. However, the RF equipment continues to operated in a degraded fashion. The receiver local oscillator "B" is intermittent and transmitter "B" is undermodulated. It has been difficult to obtain confidence in the Central Station RF equipments because these faults have been complicated by continuing inoperation of the GSE RF receiver. Improved Central Station and GSE RF components became available at the end of the report period so that long term RF operation should be achieved during February.

Category #2 tests have proceeded well on all Array "A" experiments received. The experiment's functional operation has been proper in that all command and timing and control signals have been received and executed properly. A common problem encountered with all the experiments is noise spikes induced on interface lines due to switching transients in the experiments power converters. In experiments having only digital interfaces these spikes appear to have little or no effect on the experiment or the Central Station. The full significance of these noise interactions with other experiments will not be determined until Category #3 tests. However, in experiments such as PSE where low level signals are being amplified and digitized this power converter noise results in introduction of high noise levels into the science data.

The Category #2 tests performed on CPLEE to date have not uncovered any significant interface incompatibilities. ASE subsystem tests have been performed to verify mortar and thumper operation time break, transmitter-receiver, and Central Station electronics operation.

The EM tests are proceeding as per schedule given in ATM 604. The content of this month's Engineering Model Test Progress Report varies from previous reports in that in addition to summarizing systems level test data, it also briefly summarizes experiments [illegible] tests.

2.0 ACCOMPLISHMENTS

The accomplishments of this month's Engineering Model Tests are:

1. Completion of Category #2 tests on all Array "A" experiments received.
2. Initiation of CPLEE Category #2 tests.
3. Initiation of ASE Category #2 tests.
4. Completion of Mod 14 RTG integration tests with EM Central Station.
5. STS #1 compatibility tests with EM Central Station.
6. Completion and check out of Data Output Monitor Equipment.
7. Integration of the Dust Detector Engineering Model.

3.0 TEST RESULTS

3.1 ENGINEERING MODEL TEST CONFIGURATION

The basic arrangement of the Engineering Model Central Station and experiments is shown in Figure 3-1. Table 3-1 indicates the status of all equipments on line during the month.

3.2 CENTRAL STATION STATUS

3.2.1 Data Subsystem

The Data Subsystem digital units have continued to excell through January. The only fault which has occurred with these units during the whole of the engineering model tests is that on one occasion during January the response of the command decoder became intermittent. After investigation it was concluded that poor connection in the demodulator board connector was responsible. This type of connector is only used in the Data Subsystem development models. In the prototype and subsequent models the PC component boards are hardwired to a mother board.

The operation of the RF units has been restricted by the lack of the downlink GSE receiver and by the poor performance of the local oscillators in the ALSEP uplink receiver. The RF uplink has been employed for about 50% of the total testing time during the period covered by this report, and the opportunity was taken to record the degradation in receiver noise level as the local oscillator performance deteriorated after several hours of operation.

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TABLE 3-1

STATUS OF ENGINEERING MODEL HARDWARE ON LINE

Month Ending 31 January 1967

Prime Equipments

Subsystem/Component	Breadboard	Modified Brassboard	Engineering Model	Remarks & Status
Data Subsystem				
Data Processor		X		
Multiplexer - A/D Converter			X	
Diplexer			X	
Diplexer Switch			X	
Transmitter "A"			X	
Transmitter "B"		X		Undermodulated
Receiver		X		Lo B intermittent
Command Decoder		X		
PDU			X	
Wire Harness			X	
Terminal Strip			X	
Power Subsystem				
RTG Simulator (BxA)			X	
RTG Generator (GE)			X	On line 26 and 27 Jan.
PCU			X	
PDM			X	
Structural/Thermal				
Base Plate			X	
Dust Detector			X	
Experiments				
Passive Seismic			X	
Solar Wind			X	
Magnetometer				Breadboard returned 12/7
SIDE/CCIG				Breadboard returned 20/2
CPLEE			X	
ASE			X	
Heat Flow				

TABLE 3-1 (CONT.)

STATUS OF ENGINEERING MODEL HARDWARE ON LINE

Month Ending 31 January 1967

GSE

Subsystem/Component	On Line	Operation: Satisfactory	Operation: Unsatisfactory	Remarks
Signal Breakout Boxes				
Passive Seismic #1	X	X		
#2				
Solar Wind	X	X		
Magnetometer	X	X		
SIDE/CCIG	X	X		
CPLEE	X	X		
ASE	X	X		
Heat Flow				
Data SS Test Set				
DDS 1000	X	X		
Uplink	X	X		
Downlink	X	X		
Experiment Simulators				Not used.
RF Test Set	X	X		Receiver inoperative
STS #1				On line 6, 7, and 9 January.
Experiment Test Sets				
Passive Seismic	X	X		
Solar Wind	X	X		
Magnetometer				Returned 12/7
SIDE/CCIG				Returned 12/22
CPLEE	X	X		
ASE	X	X		
Heat Flow				

Transmitter "B" produced a modulation on the +29 VDC line. The input current of this transmitter varies with its data modulation resulting in a differentiated data modulation waveform on the 29 v supply line of 300 mv peak-to-peak amplitude. The transmitter design specification has now been amended to control the variation of transmitter input current with data modulation.

A modified GSE receiver and the prototype ALSEP receiver and transmitter were received at the end of January. It is anticipated that some useful operation of the RF links will be possible during February.

3.2.2 Power Subsystem RTG Integration

The Mod 14 RTG which utilizes an electrically powered heater was successfully integrated with the ALSEP Central Station on 1/26/67 and 1/27/67, after initial leak testing and power mapping tests had been completed on the RTG. The RTG is shown together with the RTG monitoring console and temperature control units in Figures 3.2-1 and 3.2-2.

The preliminary RTG tests indicated that outputs up to 68 w could be obtained. Thus the integration test plan called for two series of tests, one with specification minimum of 56 w available to ALSEP and the other with the maximum achievable input power, i.e. between 65 w and 70 w. In practice it was established that the combination of impedance mismatching between the Mod 14 RTG at full output and of connecting cable losses limited the available power to ALSEP to 60.4 w. The integration tests were restricted to operation with reduced RTG input, adjusted to provide 56 w output power to ALSEP.

The tests which were performed were similar to the Category #1 Central Station tests with the RTG simulator, with the emphasis on power system performance evaluation.

Records of the turn-on and turn-off transients are shown in Figures 3.2-3 and 3.2-4. The main effects which control the slope of these transients are as follows. Initially, the large PCU converter input capacitor is discharged, and on turn-on this restricts the rate of rise of input voltage to the PCU, so that the voltage rises with a time constant of about 4 ms towards the open circuit output voltage of the RTG. When the input rises to 7 to 8 v, PCU #1, or 5 to 6 v, PCU #2 the power converter oscillator starts and the subsequent rise of the line voltages in limited both by the charging of the PCU input capacitor and by the charging of the PCU output filter capacitors. The reason for the difference between the output voltages transients of the two PCU's from about 3 ms onwards is not understood, but it is believed that the ripple which can be observed on the records is associated with unbalanced operation of the converter transformer, probably associated with core saturation. The stabilization of the input and output voltages when the regulator becomes operative can be seen on the traces.

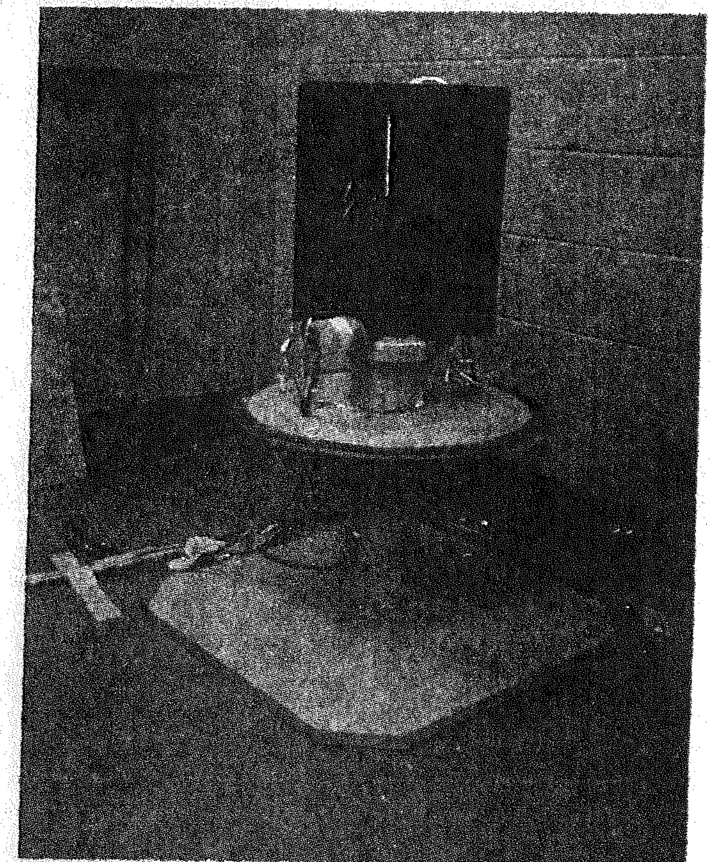


Figure 3.2-1 Mod 14 RTG Without Shroud

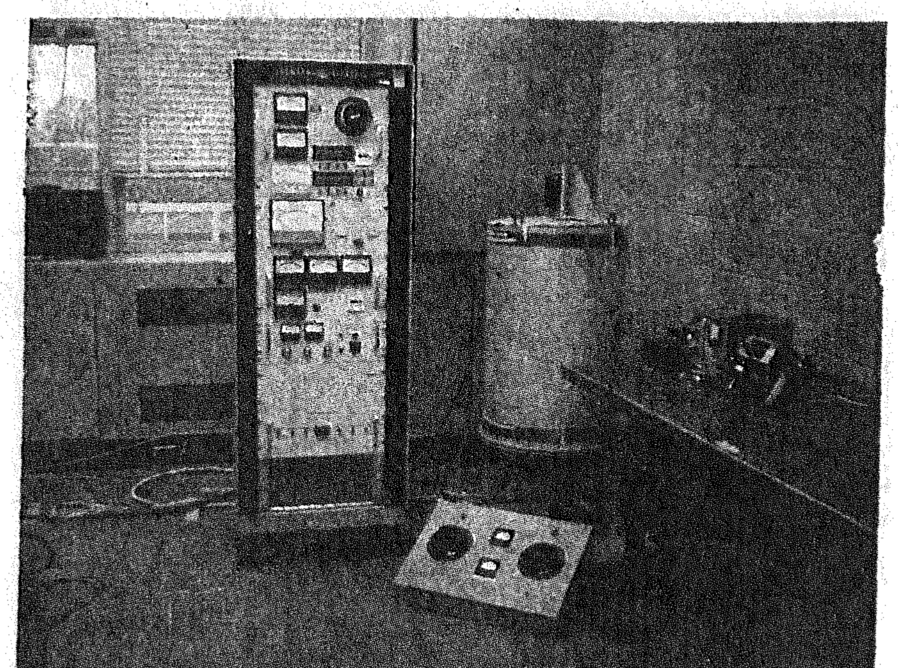


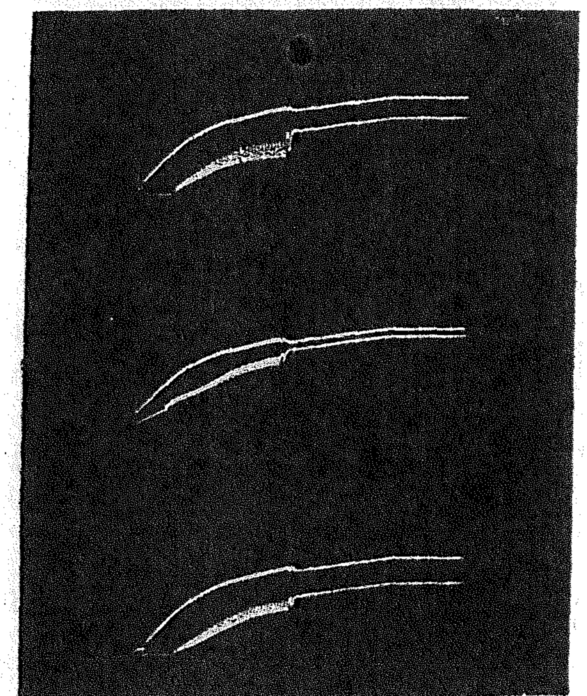
Figure 3.2-2 RTG in Shroud, RTG Test Console

Figure 3.2-3 PCU Turn On Transients

Turn on by removing short circuit from input line to PCU from RTG.
56 w input, 12 w reserve (steady state):

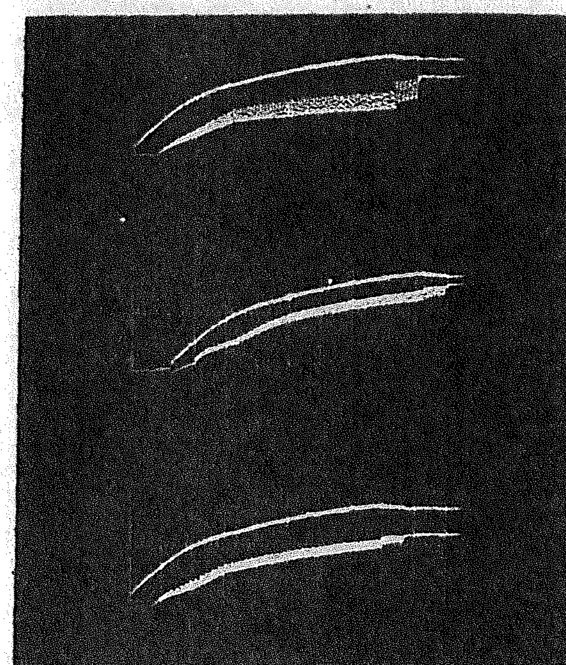
All records 1ms/cm

(a) PCU #1



Top Trace	+16v	5v/cm
Bottom Trace	+ 5v	2v/cm
Top	+16v	5v/cm
Bottom	+29v	10v/cm
Top	+16v	5v/cm
Bottom	+29v	5v/cm

(b) PCU #2



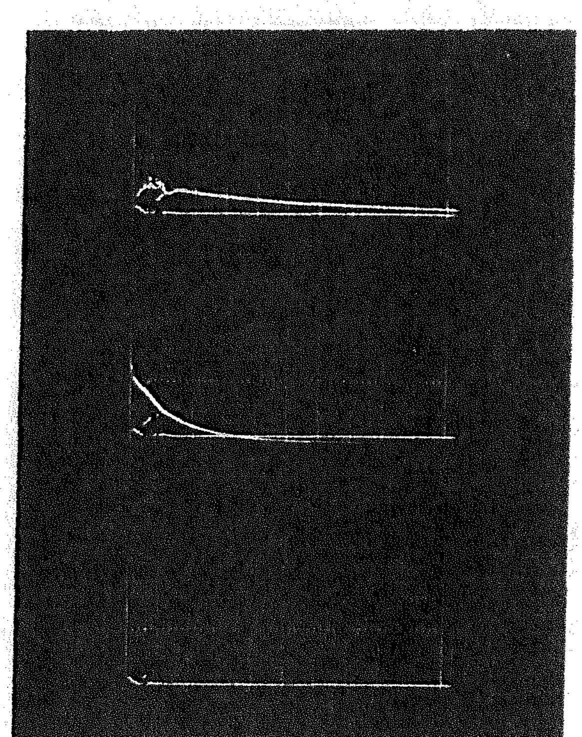
Top Trace	+16v	5v/cm
Bottom Trace	+ 5v	2v/cm
Top	+16v	5v/cm
Bottom	+29v	10v/cm
Top	+16v	5v/cm
Bottom	+12v	5v/cm

Note: Initiation time, removal of short circuit, is uncertain with respect to scope trigger point.

Figure 3.2-4 PCU Turn Off Transients

Turn off by applying short circuit to input line to PCU from RTG 56 w input, 12 w reserve initially.

All Records 1 ms/cm



Top Trace	+5v	2v/cm
Bottom Trace	+16v	5v/cm
Top	+29v	10v/cm
Bottom	+16v	5v/cm
	+16v	5v/cm

Note: Initiation time, application of short circuit, is uncertain with respect to scope trigger point.

The difference in character of the transients of +29 output line the other output lines is due to the +29 v circuit being auto coupled to the input, whereas the other lines are derived from isolated transformer windings in the PCU.

The noise on all the PCU output lines was investigated, the records for PCU #2 are shown in Figure 3.2-5. Similar records for PCU #1 are available at BxA. No ringing transient spikes could be detected, and with the exception of the +29 v line the noise amplitudes are less than 100 mv peak-to-peak The +29 v line noise is compounded from two components, one arising from PCU unbalance which produces about 60 mv peak-to-peak ripple, the other is the modulation due to the transmitter serial number 1, which as previously described in this report approaches 300 mv peak-to-peak with a differentiated data stream waveform.

The performance of the power relief sequencer with overloads stepped onto the PCU +29 v output to initiate power relief sequences operation was investigated. The results are shown in Figure 3.2-6. Various values of overload were used to obtain the various combinations of experiments ripple off. The records are considered to be self-explanatory, but the difference between the voltage transients when a marginal overload, which results in only Experiment #4 being rippled off, and more severe overloads should be noted.

Records of 29 v line transients during operation of the experiment circuit breaker were obtained, both for a marginal overload and for a 900 mA step overload on a nominal 170 mA experiment base load. The results for this latter condition are shown in Figure 3.2-7. On the originals, the marginal performance of the Babcock relays in clearing a 1 amp current can be detected. This was a known limitation of these relays, and a more satisfactory type will be used in the prototype and subsequent models of the PDU. No interactions between the power protection circuits for the experiments, or with the power relief sequencer, were detected during this series of tests.

PCU changeovers were performed and the resulting voltage transients on the PCU input line and all the PCU output lines were recorded, as shown in Figure 3.2-8 and Figure 3.2-9. No voltage levels which are considered to be detrimental to ALSEP performance were detected.

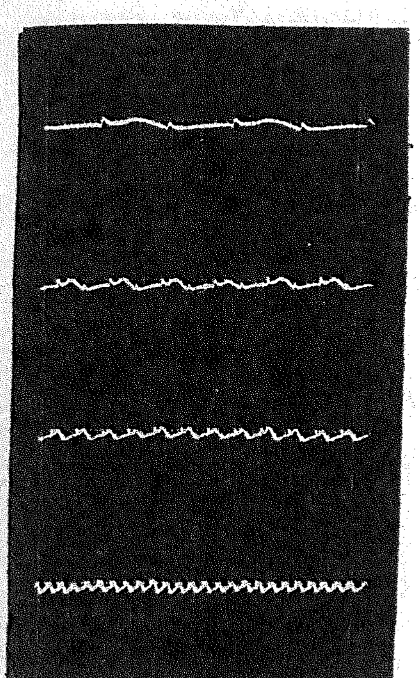
During this sequence of tests the downlink was operated satisfactorily and no errors in reading the Central Station data were observed. Also a complete command response test of the Central Station was performed satisfactorily, and no command interactions were detected.

The performance of the PCU's with limiting output loading conditions and 56 w RTG output was also explored. No performance anomalies were detected when the PCU's load were reduced to provide the regulator with more reserve power, the PCU's regulation holding the voltages correctly up to the point of regulator saturation. However, when the station load was increased, to reduce the reserve power below 1.6 w, the regulators lost control of the output voltages, and

Figure 3.2-5 Power Line Noise, Station Power Supplied by RTG

All records 200 mv/cm
56 watt input, 11 watt reserve

PCU #2



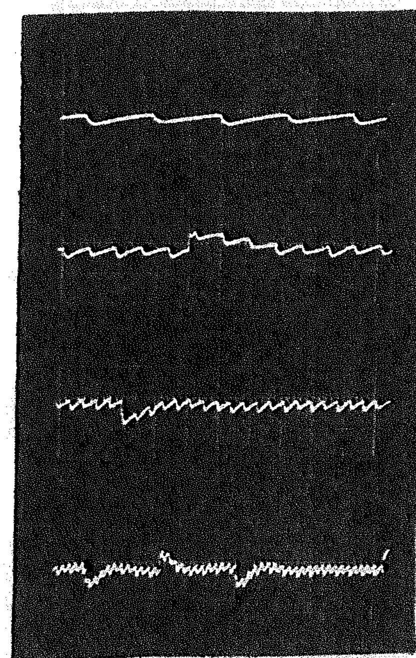
(a) +16v Input

20 μs/cm

50 μs/cm

100 μs/cm

200 μs/cm



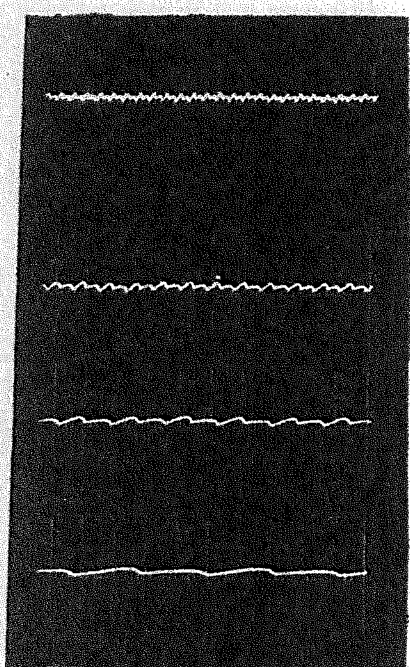
(b) +29v Line

20 μs/cm

50 μs/cm

100 μs/cm

200 μs/cm



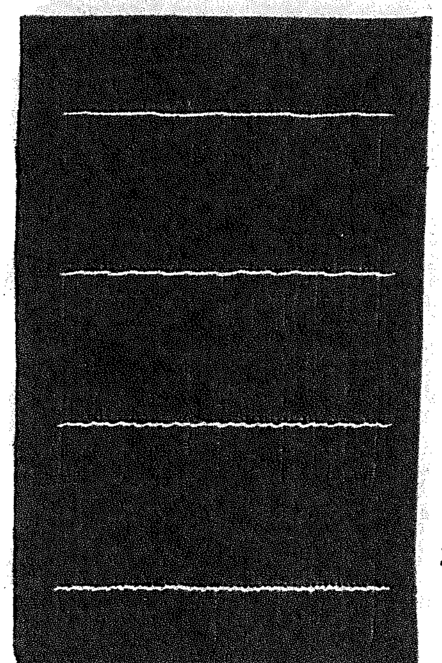
(c) +12v Line

20 μs/cm

50 μs/cm

100 μs/cm

200 μs/cm



(d) +5v Line

20 μs/cm

50 μs/cm

100 μs/cm

200 μs/cm

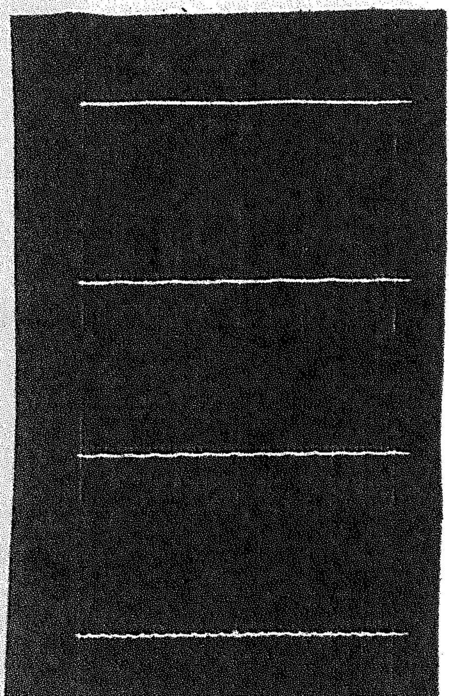
Note: All records are single shot, non-synchronous.

Figure 3.2-5 (Cont.)
Power Line Noise, Station Power
Supplied by RTG

All records 200 mv/cm
56 watt input, 11 watt reserve

PCU #2

(e) +15v Line



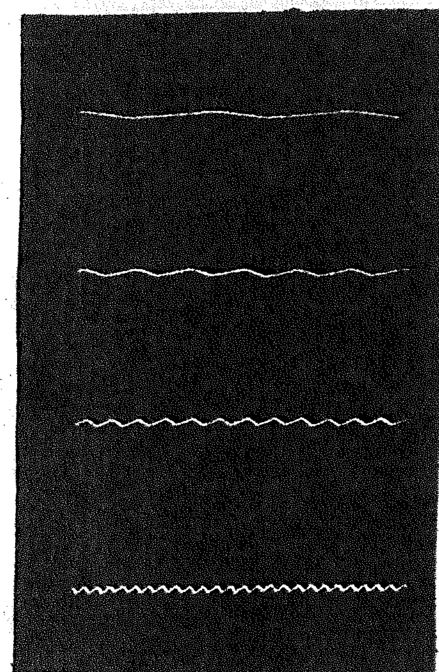
20μs/cm

50μs/cm

100μs/cm

200μs/cm

(f) -6v Line



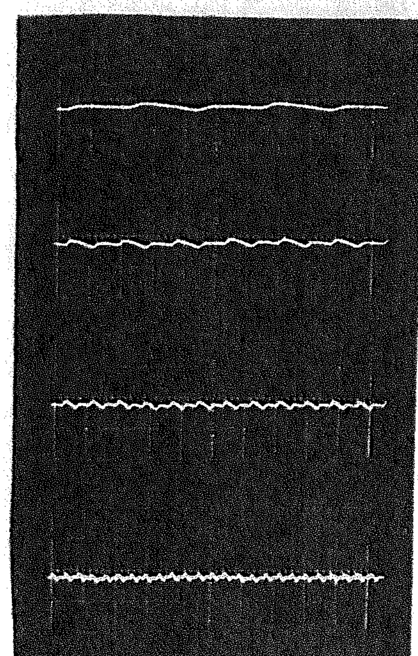
20μs/cm

50μs/cm

100μs/cm

200μs/cm

(g) - 12 v Line



20μs/cm

50μs/cm

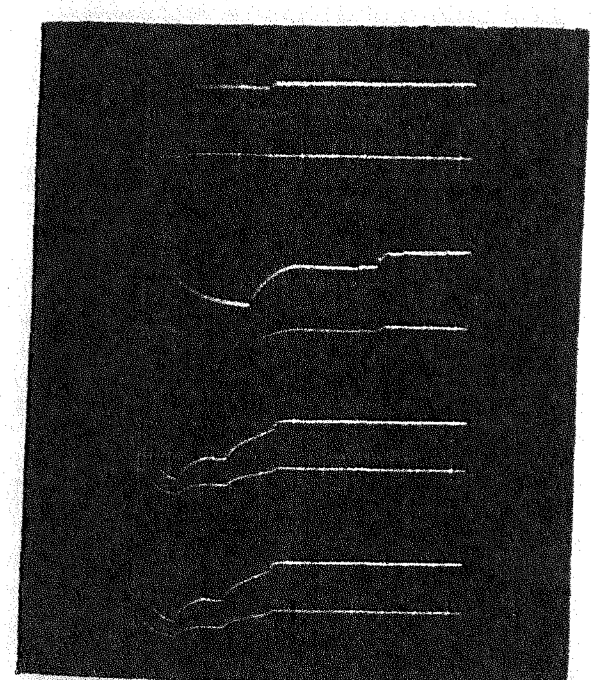
100μs/cm

200μs/cm

Note: All records are single shot, non-synchronous.

Figure 3.2-6 Line Transients During Operation of Power Relief Sequencer

All records +29v at PCU, Top Trace
+16v at PCU, Bottom Trace



(a) PCU #1

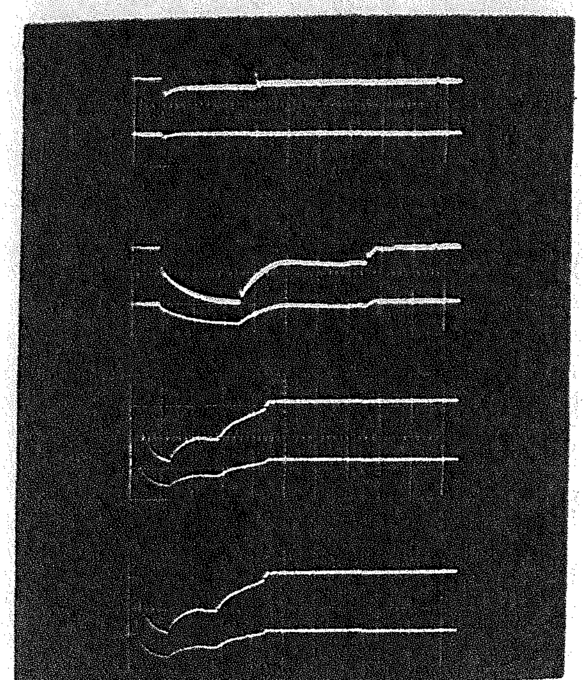
Experiment #4 OFF

500 mv/cm

Experiments #4 and #3 OFF 2 ms/cm

Experiments #4, #3 and #1 OFF

1 v/cm
5 ms/cm



(b) PCU #2

Experiment #4 OFF

500 mv/cm

Experiments #4 and #3 OFF 2 ms/cm

Experiments #4, #3 and #1 OFF

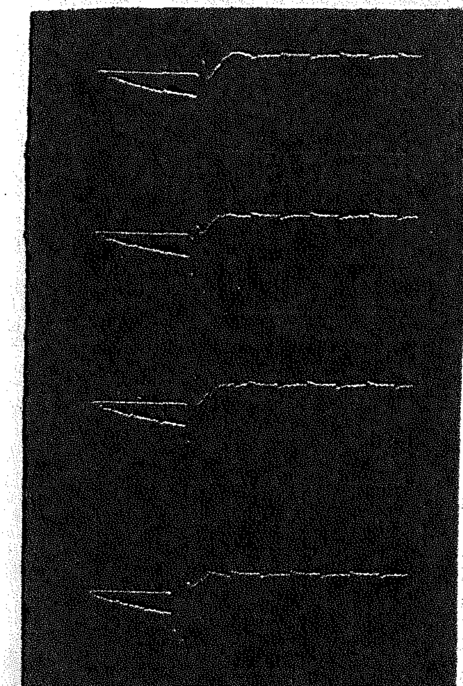
1 v/cm
5 ms/cm

Station power supplied by RTG.

All experiments simulated by 170 mA dummy resistive loads. Overload stepped onto PCU +29v output to initiate power relief sequencer. operation.

Figure 3.2-7 Line Transients During Operation of Experiment Overload Protection Circuits

Station power supplied by RTG.
All records +29v at PCU, Top Trace, 1 v/cm 0.5 ms/cm
+29v at Expt., Bottom Trace, 10v/cm



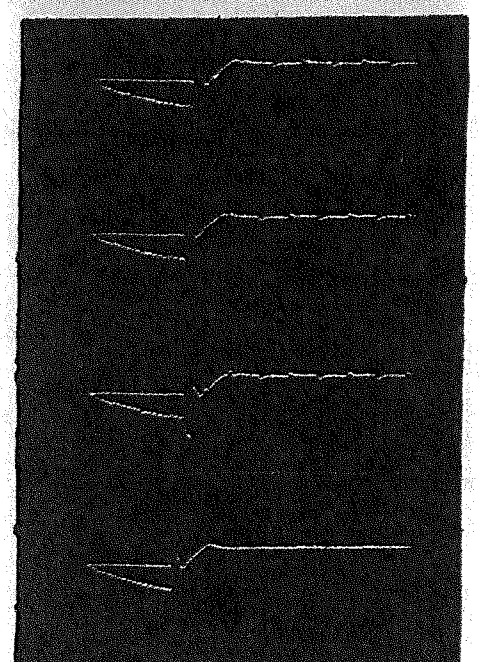
(a) PCU #1

Expt. #4

Expt. #3

Expt. #2

Expt. #1



(b) PCU #2

Expt. #4

Expt. #3

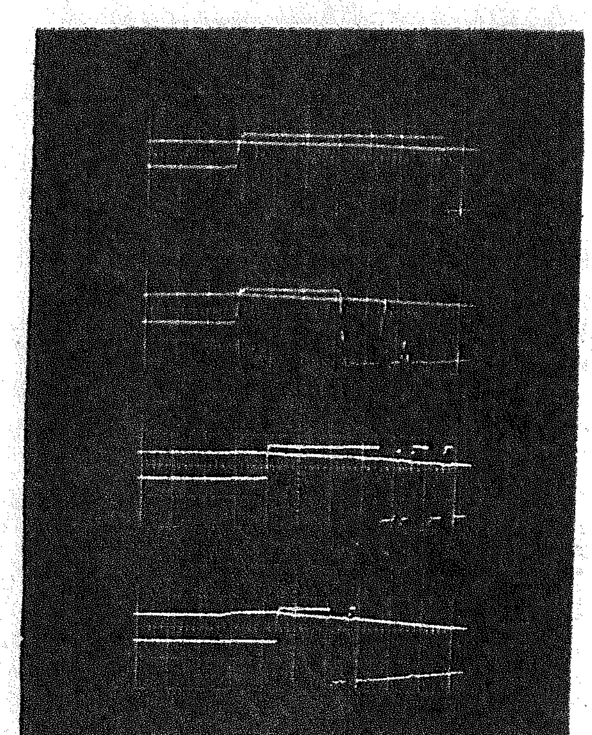
Expt. #2

Expt. #1

All experiments simulated by 170 A resistive loads.
Power reserve approximately 11 watt.
Operation initiated by step resistive load, of 900 mA.

Figure 3.2-8 PCU Changeovers, Station Power Supplied by RTG

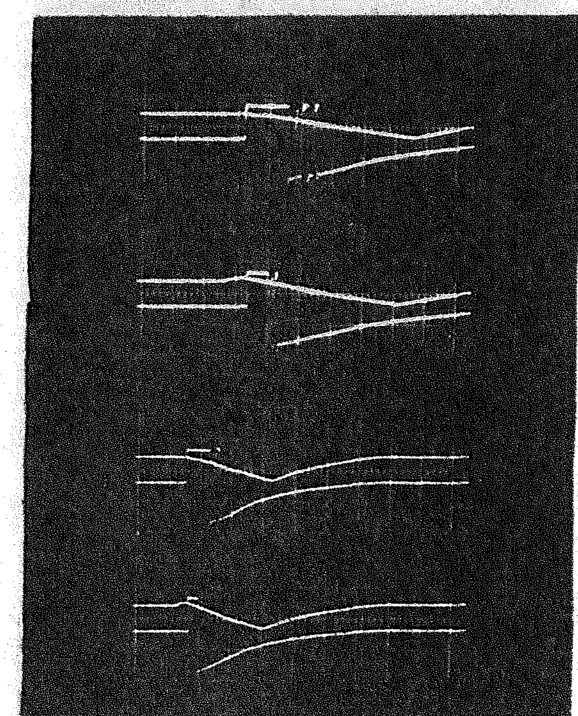
All Records Top Trace +12 Line 5v/cm
Bottom Trace +16v Input 10v/cm



(a) 100 μs/cm and 200 μs/cm

PCU #2 → #1
100 μs/cm
PCU #1 → #2

PCU #2 → #1
200 μs/cm
PCU #1 → #2

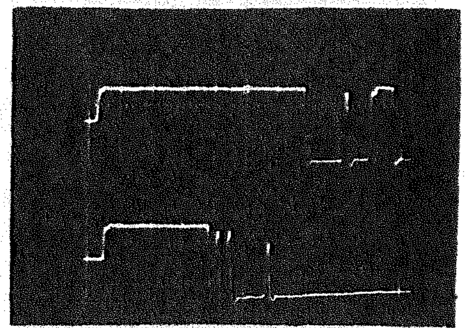


(b) 500 μs/cm and 1 ms/cm

PCU #2 → #1
500 μs/cm
PCU #1 → #2

PCU #2 → #1
1 ms/cm
PCU #1 → #2

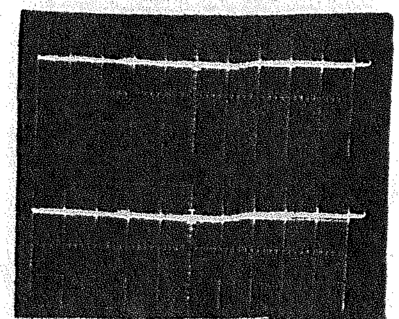
Figure 3.2-9 PCU Changeovers Station Power Supplied by RTG



(a) <u>+16v Line</u> 10v/cm

PCU #2 → #1
100 μs/cm
PCU #1 → #2

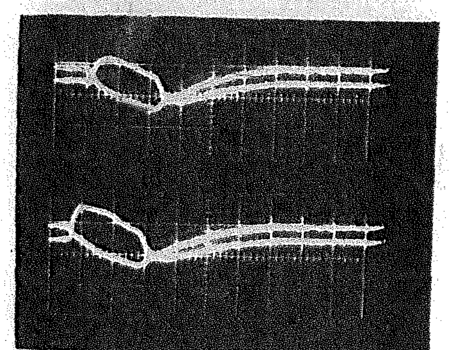
All records below at 1 ms/cm



(b) <u>+15v Line</u> 5v/cm

PCU #2 → #1

PCU #1 → #2

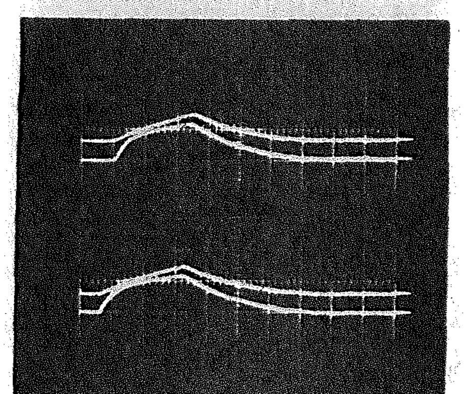


(c) <u>Top Trace +29v Line</u> 10v/cm

<u>Bottom Trace +5v Line</u> 2v/cm

PCU #2 → #1

PCU #1 → #2



(d) <u>Top Trace -12v Line</u> 5v/cm

<u>Bottom Trace -6v Line</u> 2v/cm

PCU #2 → #1

PCU #1 → #2

noise outputs of up to 90 mv peak-to-peak on the +12 v line and 250 mv peak-to-peak on the +29 v line were recorded. The noise waveform was complex, and was primarily composed of odd harmonies of 29 Hz. This phenomena will be further investigated.

3.2.3 Engineering Model Power Budget, Central Station and Experiments

The measured power consumption of the Central Station is shown in Table 3.2-1, for the experiments in Table 3.2-2. The load fluctuations in the Central Station, apart from the transmitter previously discussed, are small and have little effect on ALSEP performance, the variations of experiment loads are summarized in Table 3.2-2. Some of the records from which the experiment input power data shown in the table was derived are snown in Figures 3.2-10 through Figure 3.2-15.

Those cases where the experiment power consumption is at variance with the ICS requirements, are referred to in the discrepancy tables for the individual experiments which are contained in Section 3.3 of this report.

3.3 CATEGORY #2 TESTS

3.3.1 Passive Seismic Experiment

Category #2 tests on the PSE were completed on the 23 of January 1967. Table 3.3.1-1 lists the discrepancies noted during the tests. This list of discrepancies applies only to the tests conducted which were limited due to the use of the PSE Central Station Electronics without sensor.

A summary of results of these tests is given below.

Power - The PSE generated noise on the 29 volt line due to the switching action of its DC-DC converter. Frequency of the converter was approximately 27 KHz. Figure 3.3.1-1 depicts the 1.5 v ringing transient at the 18.5 μsec repetition rate.

A 29 v turn-off transient of 160 v peak-to-peak and ringing at 200 KHz was observed and is shown in Figure 3.3.1-2. Several transients occurred during each turn off as the Central Station relay bounce opened and closed the circuit. Figure 3.3.1-3 depicts the turn off with experiment and with a resistive load of 220 mA at SBOB.

A turn on power transient of 11.8 watts was recorded. Figure 3.3.1-4 shows the turn on waveform along with its corresponding transient on the +29 v line. The amplitude of the 29 v transient is approximately 400 mv, which is what would be expected during the 400 mA surge.

Commands - The PSE response to commands was satisfactory. Absence of realistic loads associated with the executive of the commands prohibited and investigation of power transients. These included the auto leveling, leveling speed and thermal control.

TABLE 3.2-1

MEASURED CENTRAL STATION POWER CONSUMPTION

Component	+29v	+15v	+12v	+5v	-6v	-12v	Totals	Units
Data Subsystem Digital Components	1,188	67.5	698	2,320	233	361	4,867.5	mw
Receiver	———	———	561	———	———	———	561	mw
Transmitter	9,610	———	216	———	———	———	4,826	
Totals	10,798	67.5	1,475	2,320	233	361	15,254.5	mw
Diplexer (estimated)	———	———	150 mw (with Transmitter B only)	———	———	———	150	mw
Measured PCU #1 Output Voltage	29.31	15.32	12.06	5.192	-6.408	-12.36		v
Measured PCU #2 Output Voltage	29.60	15.39	12.06	5.238	-6.464	-12.40		v

TABLE 3.2-2

RECORDED EXPERIMENT POWER CONSUMPTION

Experiment	Normal Mean	Operation Fluctuation	Turn On Peak	Heater Mean	Load Peak	Operating Peak	Condition at Operating Peak
PSE	6.3 w	0.2 w peak-to peak ripple	11.8 w Recovers to 7.0 w in 40 ms	Heater not fitted		6.8 w actual peak 12.5 w actual peak	Stabilization after expt. turn ON. Simulated motor load turn ON.
LSM	5.1 w	1.7 w peak to peak ripple	11.2 w with 50 ohm limiting resistor	1.0 w	Not Recorded	10.5 w actual peak 11.9 w actual peak	Motor ON Motor turn ON.
SWS	About 3.6 w	From 2.6 w min to 5.2 w max.	10.7 w Recovers to 5.0 w in 60 ms	3.0 w	Not Recorded	6.2 w Actual peak	Voltage selector relay transient (Dust cover removed could not be tested)
SIDE	4.6 w	From 4.4 w min to 4.9 w max. including ripple	7.4 w with 50 ohm limiting resistor	Heater not fitted		1.7 w peak transient	Channeltron R H. V. supply ON transient (Dust cover removed could not be tested)
CPLEE (Low voltage supplies only ON)	2.3 w		6.2 w for <10 ms recovers to 3.0 w at 40 ms	2.0 w	2.6 w peak transient for 20 ms	1.0 w peak transient for 20 ms	Dust cover removed logic.

Note: All figures derived from current traces from strip chart recorder with a bandwidth of 140 Hz. Fast current peaks, e.g. associated with power converter operation, are not included.

TABLE 3.3.1-1

ENGINEERING MODEL TEST DISCREPANCIES - PSE

Problem Requiring Modification	ICS Paragraph	ICS Value	Acceptable Value to Bendix	Remarks
1. ETS Single Point Ground	3.2.5.1	1 megohm isolation between grounds.	ICS value	Single point ground violated in ETS via sensor input to electronics.
2. Power Line Noise	3.2.3	———	Acceptable value dependent on outcome of Category #3 tests.	1.5 v peak-to-peak due to power converter. See Figure 3.3.1-1
3. ETS loading of ETS Buffered Control Signals i.e. Shift Pulse and Data Gate	3.2.6.3.1	———	ICS Value	Expected to be modified for prototype tests.
4. No Provision for External Frame Mark on ETS	———	———	———	To be included in ETS for prototype tests.
5. No Connection to Survival Power in PSE Connector	3.2.3.2	———	———	Under investigation expected to be included in prototype PSE.
6. Apparent Absence of 29 v Isolation Diodes	———	———	———	Isolation diodes shown on PSE schematic missing. Expected to be included in prototype PSE.
7. Turn-on Power Transient	3.2.3.1	10.5 w	10.5 w	11.8 watt transient recorded during experiment turn on.

TABLE 3.3.1-1 (Cont.)

Problem Requiring Modification	ICS Paragraph	ICS Value	Acceptable Value to Bendix	Remarks
8. Turn-off Voltage Transient	3.2.3.5	———	Between 110 v and -50 v. 200 mh max. inductance in series with load.	150 v peak-to-peak with ringing at 200 KHz. See Figure 3.3.1-2.
9. 29 v Noise Due to Level Power Switch On	3.2.3.5	20 mv	150 mv	Refer to Figure 3.3.1.6. Noise due to X level power turn on 2.5 v peak-to peak on 29 v line.
10. Power Converter Noise on Timing Control, and Command Lines	3.2.2.7	100 mv	100 mv	Noise measured at greater than 500 mv.
11. Power Converter Noise On Analog Lines	———	———	Dependent on measuring accuracy required on these lines.	Noise measured at greater than 400 mv.
12. Power Converter Noise on Science Data Input	———	———	See AL 270000 Specification	Noise on data input resulted in jitter of 5 LSB on downlink printed.

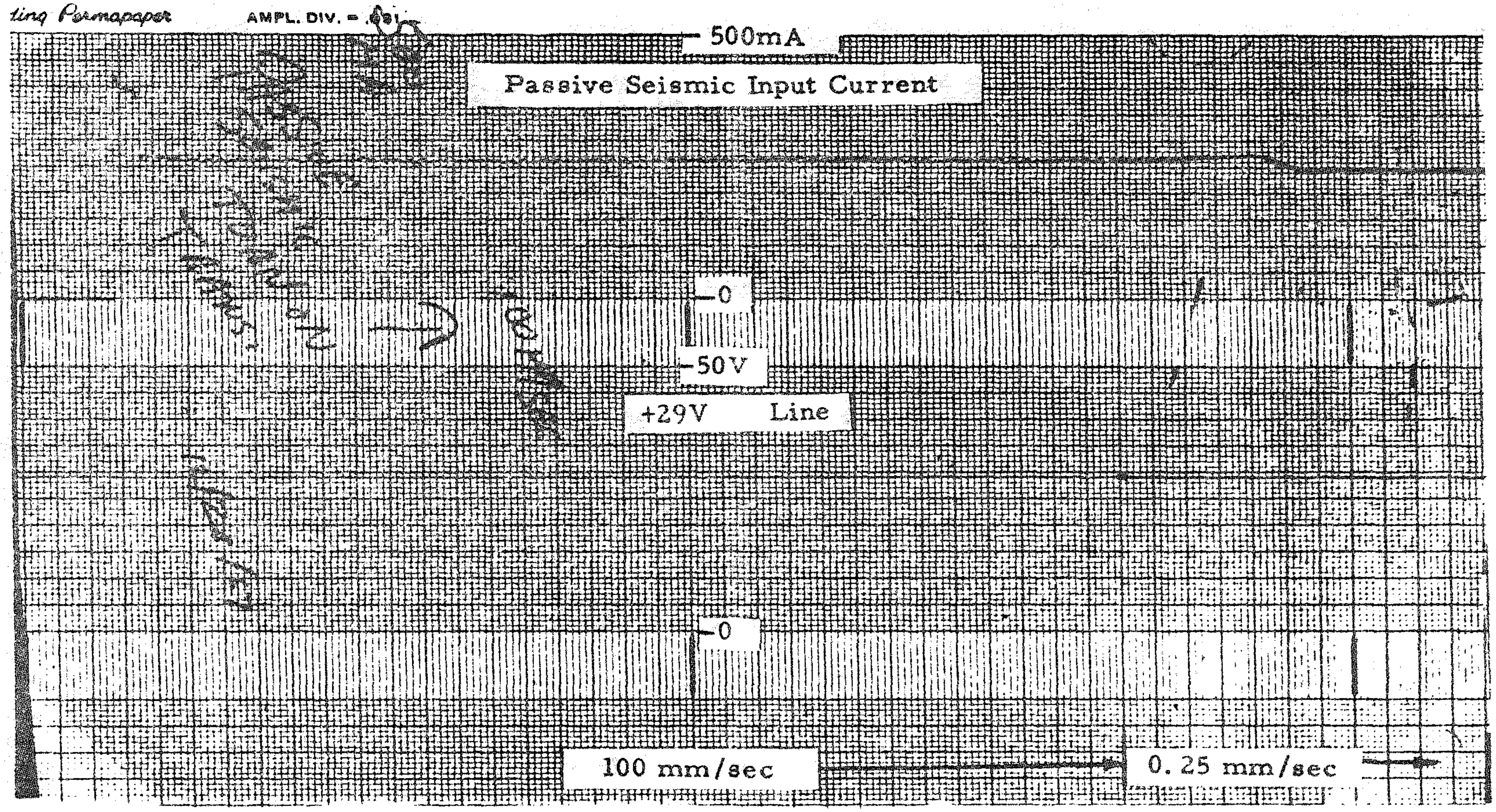


Figure 3.2-10 PSE Turn On Transient

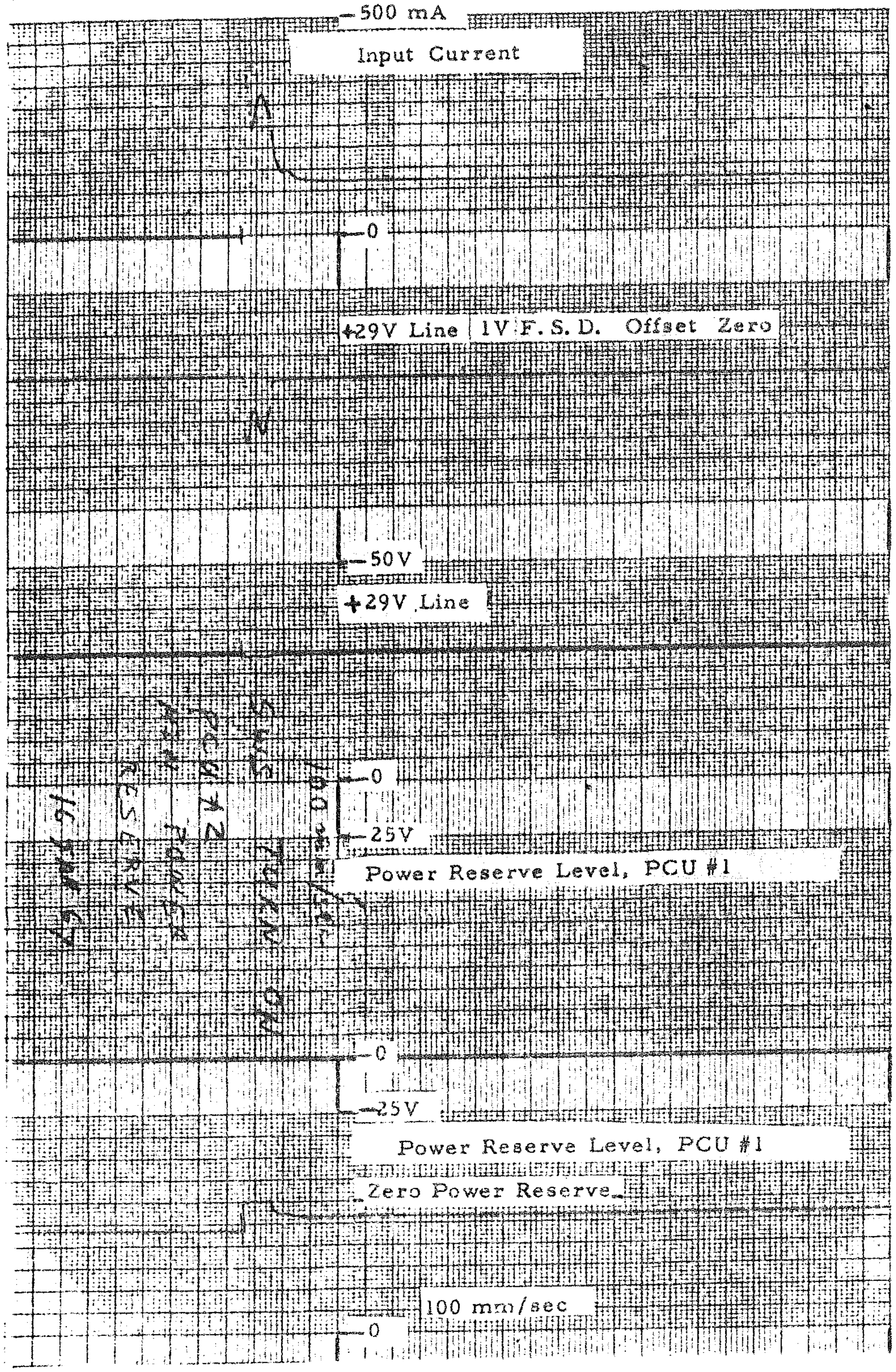


Figure 3.2-11 SWS Turn On Transients

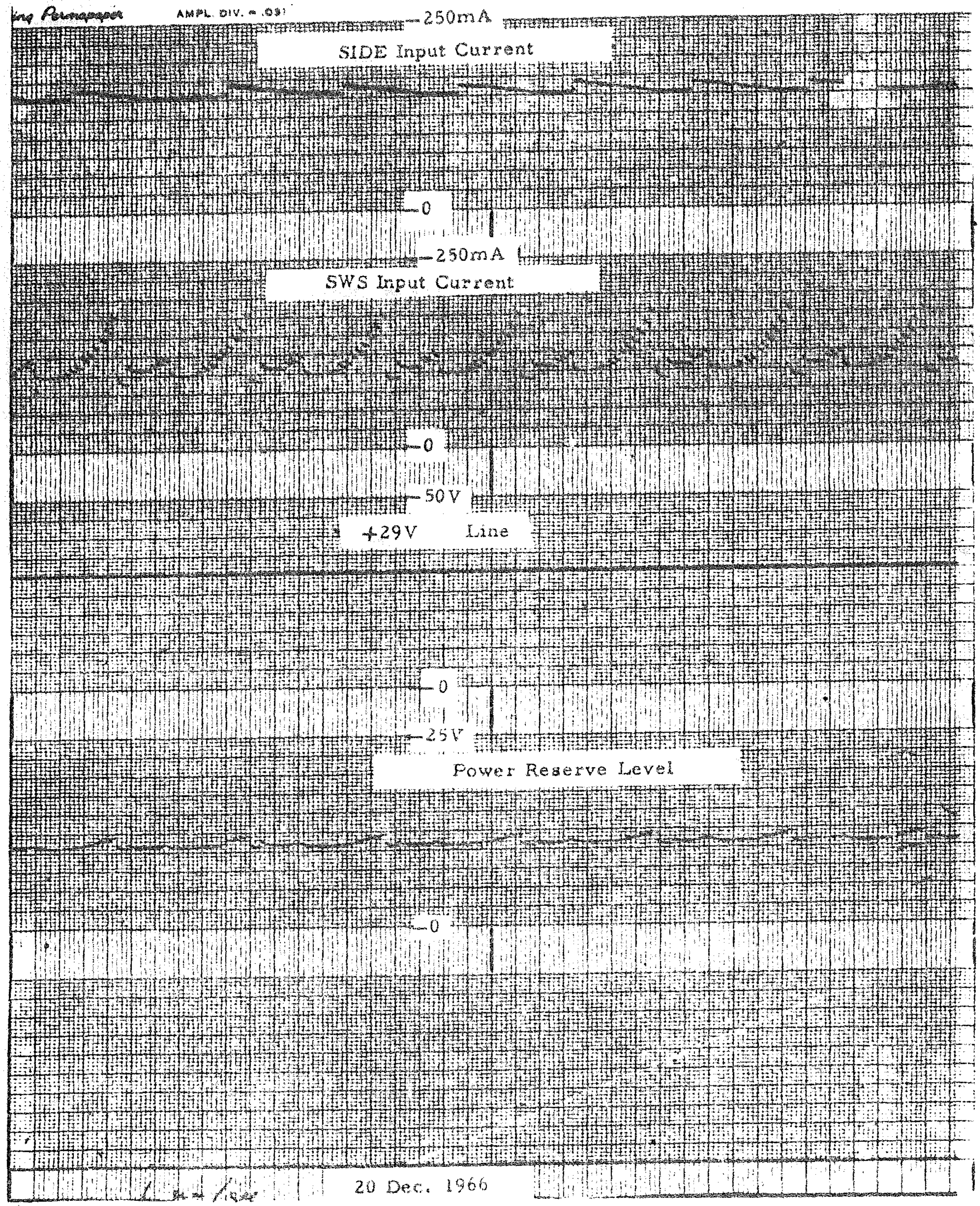


Figure 3.2-12 SIDE and SWS Current Profiles

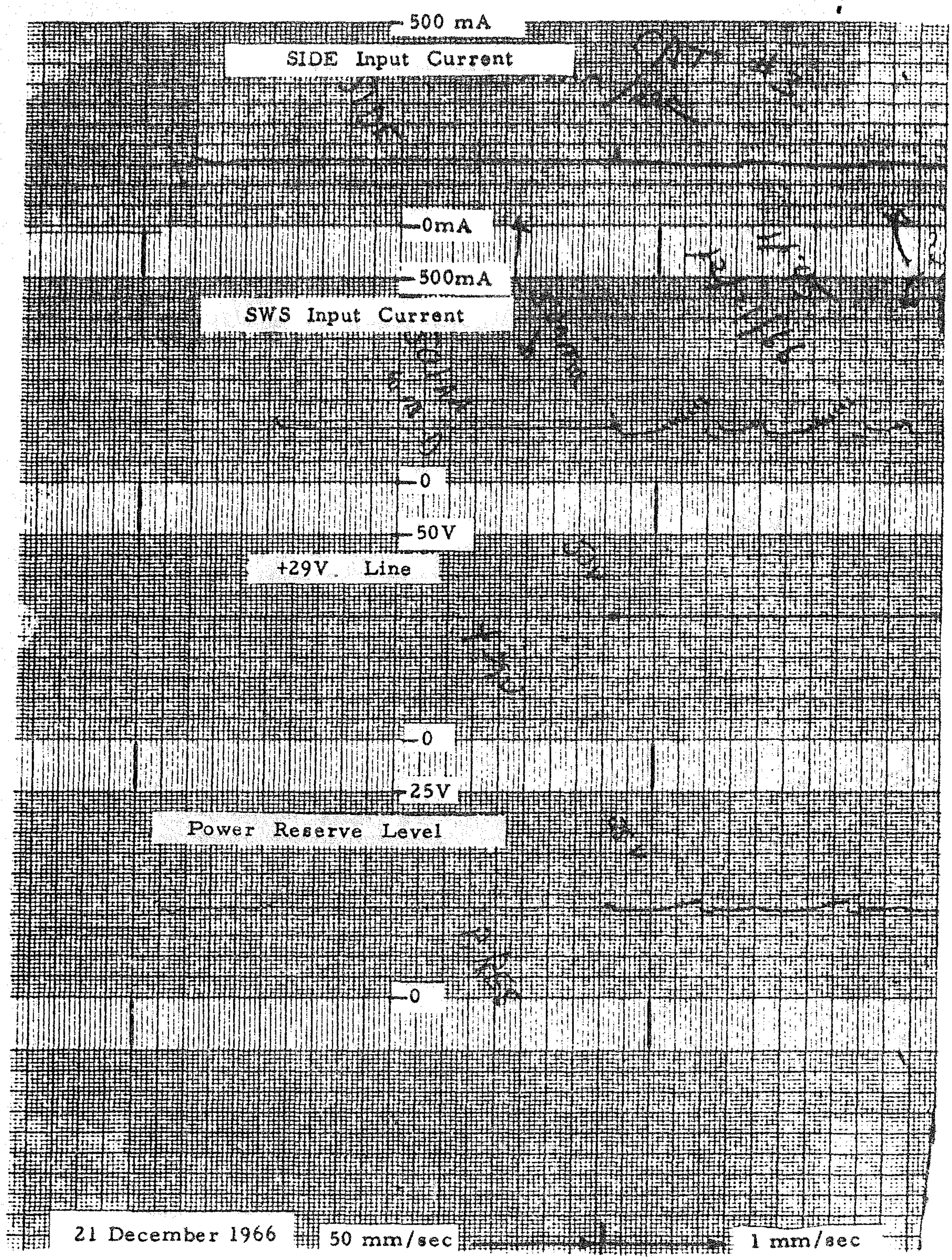


Figure 3.2-13 SIDE Turn On Transients, with SWS on Line

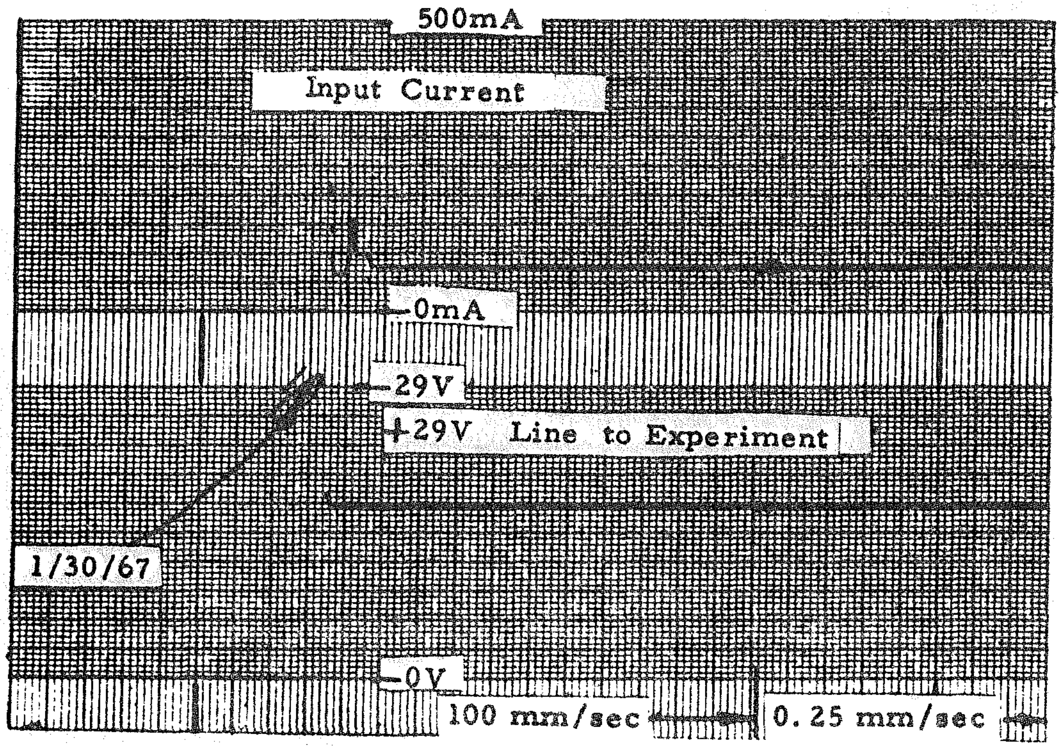


Figure 3.2-14 CPLEE Turn On Transients Low Voltage Supplies only on in Experiment

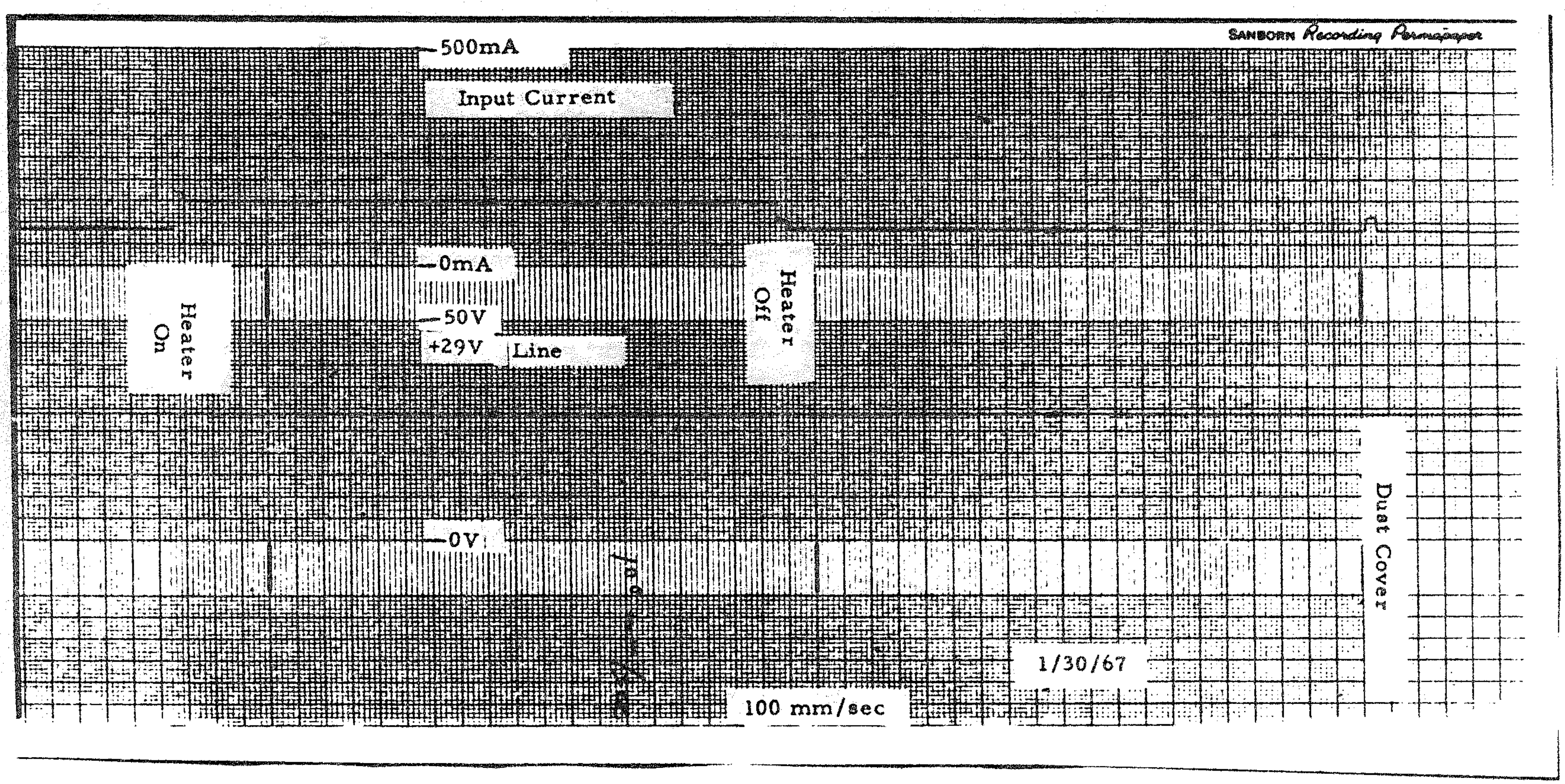


Figure 3.2-15 CPLEE Current Profile During Command Response

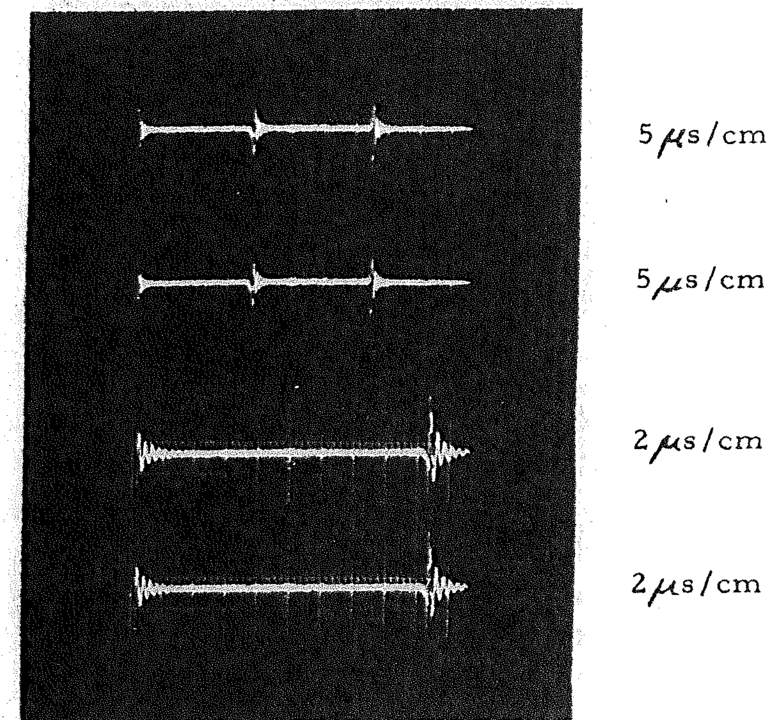
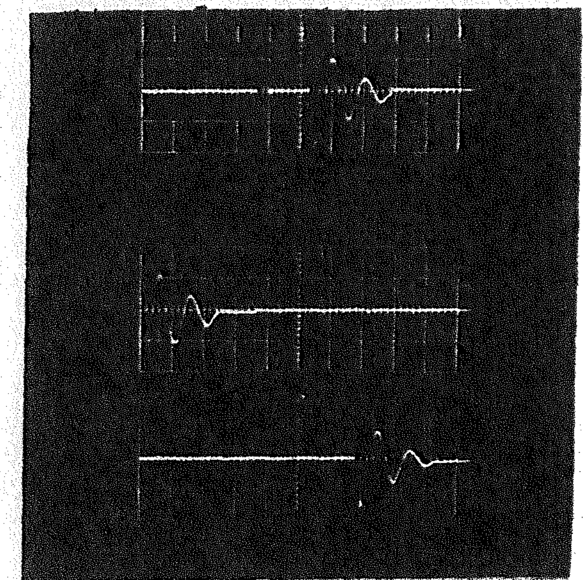


Figure 3.3.1-1 +29v Power Converter Noise 500 mv/cm

Note: These are multiple sweep exposures. Non-synchronous noise is present but not recorded.

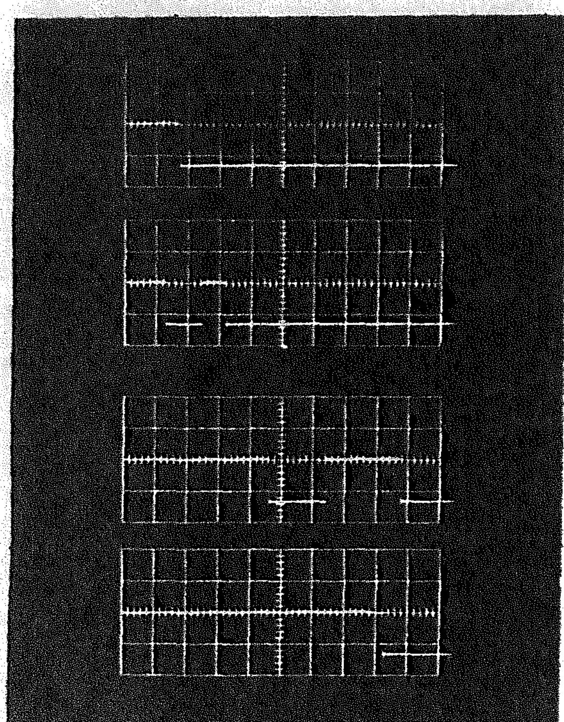


50μ/cm

50 v/cm

5μs/cm

Figure 3.3.1-2 Passive Seismic Turn-off Transient



20 v/cm

100μs/cm

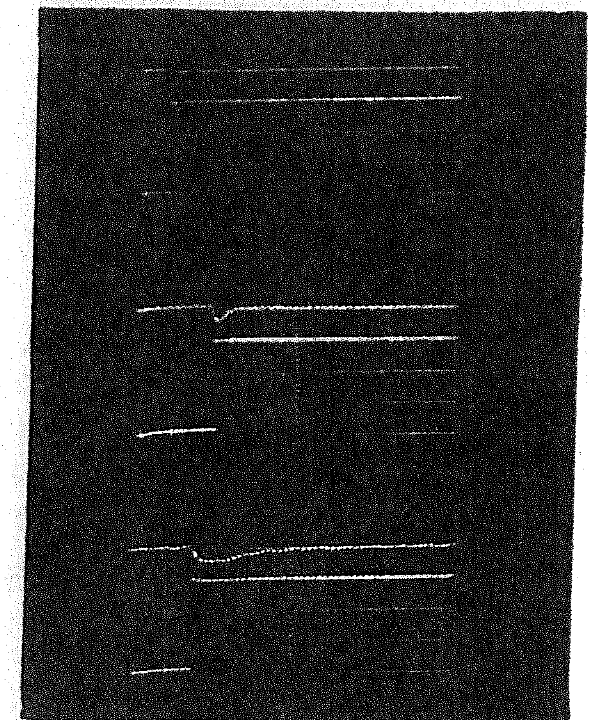
50μs/cm

20μs/cm

10 μs/cm

+29 at center of grid.

Figure 3.3.1-3 Passive Seismic Turn-off Transient, 220 mA Dummy Load



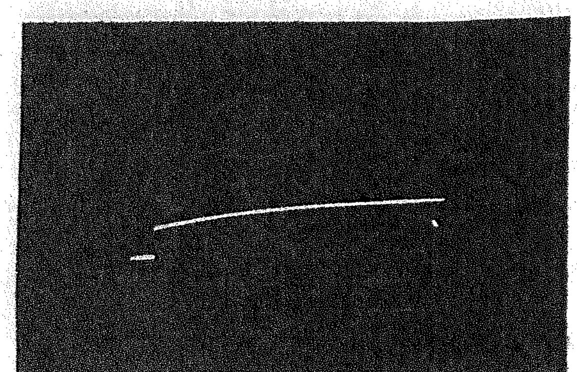
500 μs/cm

200 μs/cm

50 μs/cm

Top Trace +29 v at PCU, 1 v/cm
Bottom Trace +29 v at SBOB, 10 v/cm

Figure 3.3.1-4 Passive Seismic On Transient



2 v/cm
100 μs/cm

Figure 3.3.1-5 Passive Seismic Uncage Command, Trailing Edge

The PSE uncage command was abnormal. The fall time of the leading edge of the command was recorded at approximately 400 nanoseconds. The trailing edge of the uncage command broke at the 2 v level and required 1 ms to recover to the 4 v quiescent level. Figure 3.3.1-5 depicts the uncage command signal.

Transients on the +29 v line were induced when the level motors were switched on by command. Dummy loads were employed in the experiment and a transient of 2.5 v was present. Figure 3.3.1-6 shows the complex waveform. The 2.5 peak amplitude occurs at the beginning of the ringing and may not be visible because of degradation of the photograph during reporduction.

DC-DC converter noise was present on the command lines. Amplitude of the coupled noise was on the order of 200 mv.

Timing and Data Signal Waveforms - the timing, control and date waveforms were satisfactory. Fall time of all signals approached the minimum of 2μsec.

Science Data - Noise in the science output was investigated by grounding the science data input at the ETS and monitoring the DDS-1000 print out. Jitter of the science data was observed as high as 5 bits, i.e., first 5 LSB on the short period channel. Photographs of the analog science data channels were taken via the special analog test connector on the PSE electronics. Figure 3.3.1-7 shows the 270 KHz 460 mv noise which was attributed to crosstalk from the PSE A-D converter oscillator. The modulation on the SP lines is synchronized with the data demand line; the high amplitude noise portion corresponding to the absence of the demand pulse. This operation is being investigated with Teledyne.

Figure 3.3.1-8 shows the noise on the short period, tidal, and long period inputs to the PSE A-D converter observed during subsystem testing. The noise crosstalk on tidal is about 350 mv peak-to-peak at a low duty cycle and 40 mv peak-to-peak continuous, LP seismic is about 420 mv peak-to-peak at low duty cycle and 120 mv peak-to-peak continuous, and short period seismic has 460 mv and 150 mv peak-to-peak components.

3.3.2 Solar Wind

The remainder of the Category #2 tests for SWS were completed on 19 January, 1967. No significant interface problems were encountered throughout these tests. A list of out-of-specification conditions is given in Table 3.3.2-1.

A summary of test results is given below.

Power - A photograph of the 29 v noise cause by SWS stepping through it sequence is shown in Figure 3.3.2-1. The 1.2 second steps are caused by the experiment stepping through various particle energy levels. Superimposed is the 10 KHz, 80 millivolt noise characteristic of the Central Station PCU.

TABLE 3.3.2-1

SOLAR WIND ENGINEERING MODEL TEST DISCREPANCIES

Problem Requiring Modification	ICS Paragraph	ICS Value	Acceptable Value to Bendix	Remarks
1. 5.9v on Command Line	3.2.2.3	+5.5v	+5.5v	Incorrect bias circuit. Will be modified before prototype tests.
2. Power Line Noise	3.2.2.8.6	±75 mv	Acceptable value dependent on outcome of Category #3 tests.	200 mv peak-to-peak noise caused by DC-DC converter.
3. Power Turn-off Transient	3.2.2.8.6	±75 mv	Measured value is acceptable	ICS value will be defined such that the 35v p-p turn-off transient will be with specification.

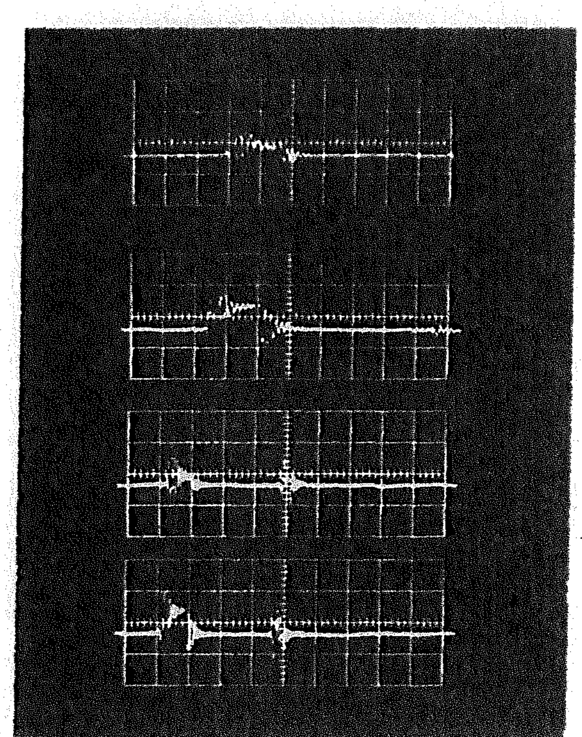
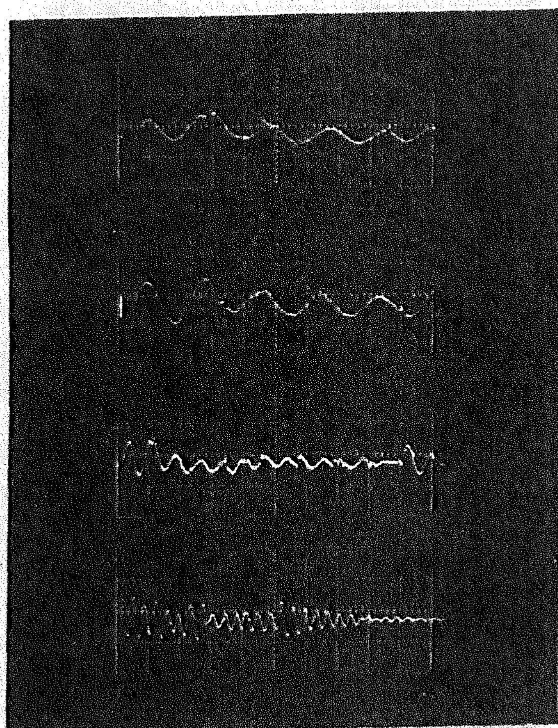


Figure 3.3.1-6 Passive Seismic +29v Noise,
X Level Power On, 1 v/cm

Figure 3.3.1-7 Passive Seismic, Noise On Science Line input to PSE A-D Converter - Systems Tests Analog Test Point #2 - Short Period Seismic



All records 500 mv/cm

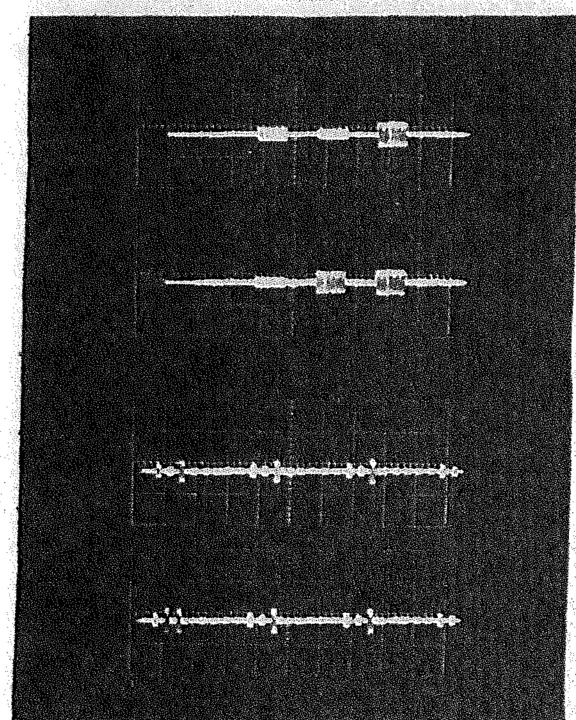
(a) 10 ms/cm and 50 ms/cm

10 ms/cm

10 ms/cm

50 ms/cm

50 ms/cm



(b) 2, 5 and 10μsec/cm

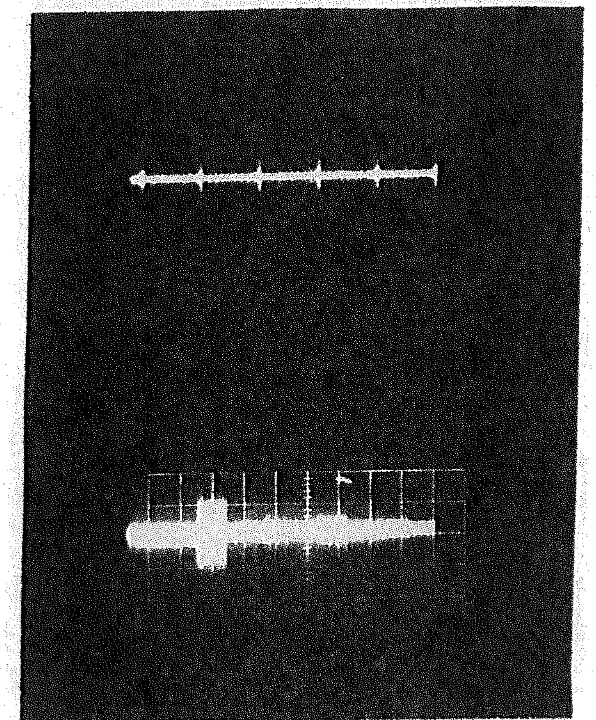
2μsec/cm

2μsec/cm

5μsec/cm

10μsec/cm

Figure 3.3.1-8 Passive Seismic, Noise On Science Line Input to PSE A-D Converter - Subsystem Tests

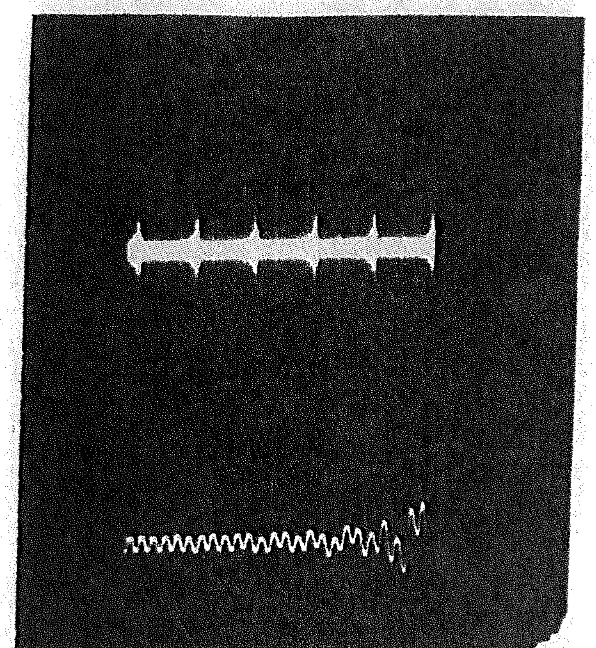


(a) Analog Test Point #4 - Y Tidal

200 mv/cm
10 ms/cm

(b) Analog Test Point #2 - Short Period Seismic

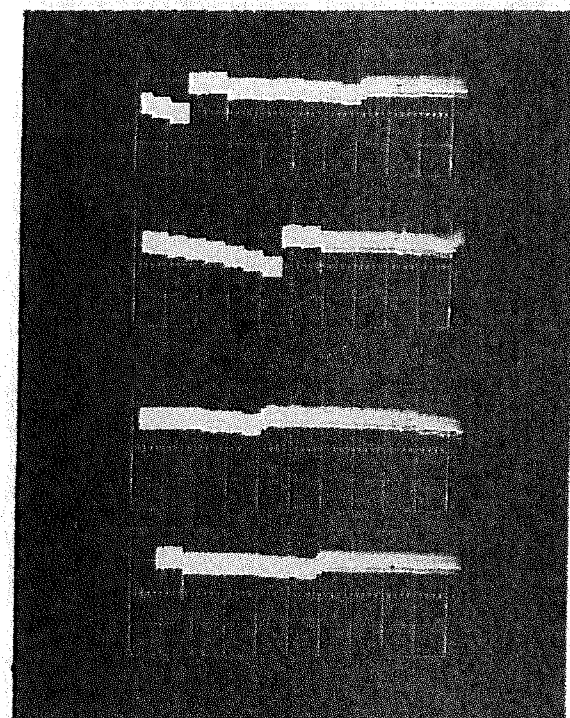
200 mv/cm
10 ms/cm



(c) Analog Test Point #8 - X Axis Low Period Seismic

200 mv/cm
10 μs/cm

200 mv/cm
0.5 μs/cm



100 mv/cm
2 sec/cm

Figure 3.3.2-1 Modulation of +29v Line to SWS with Steps in Sequence

Power line noise caused by the experiment DC-DC converter was similar to that seen on other experiments. Converter frequency was approximately 2.18 KHz which induced noise at a repetition rate of 230 μsec with an amplitude of about 200 mv.

Commands - the single command for dust cover removal was measured and its characteristic were within specifications. No provision was made to simulate the dust cover removal load.

Timing and Data Signal Waveforms - all timing and data waveforms were within specification. Rise and fall times, and pulse durations were photographed, in normal and the slow data mode. Figure 3.3.2-2 is a typical photograph depicting the timing relationship of the data and shift pulses.

Downlink Performance - The Solar Wind science data was received satisfactorily by the BxA downlink and readout equipment. Meaningful science data was not obtained because of the disabled high voltage connection to the sensors. Approximately 5000 bits of data printed out by ETS and downlink GSE printer were compared for errors. Two discrepancies were noted: one appeared definitely to be an ETS printer error while the other may have been a true discrepancy or an error of either the ETS or DDS-1000 printer.

3.3.3 Charged Particle Lunar Environments Experiment

3.3.3.1 CPLEE Subsystem Tests

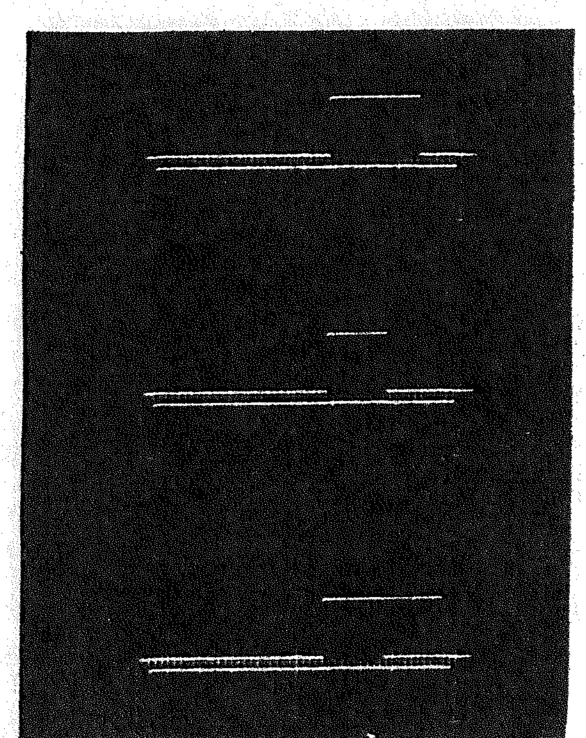
The test check out of the CPLEE Engineering Model continued on a subsystem basis during most of this report period. The electrical interface circuits that were damaged by the accidental application of 110 volts on 28 December, 1966 were replaced, and the unit was returned to BxA on 16 January, 1967. Preliminary performance tests were performed with the ETS during the period of 16 January through 24 January. These tests were performed with the experiment operating under atmospheric pressure so the switchable power supply and channeltron power supply were disabled in order to prevent damage due to high voltage arcing. These preliminary tests verified the interface compatibility between the ETS and experiment and provided the technical data to assure that the CPLEE Engineering Model was safe to operate with the ALSEP Central Station. However, the following electronic discrepancies occurred during these subsystem tests:

1. The current limiter in the low voltage power supply failed and a 4.0 ampere turn-on transient occurred. The current limiter was replaced in order to correct this problem.

2. The command line number 7 circuitry that increases the Channeltron power supply voltage from normal level (2700 volts) to high level (3100 volts) failed.

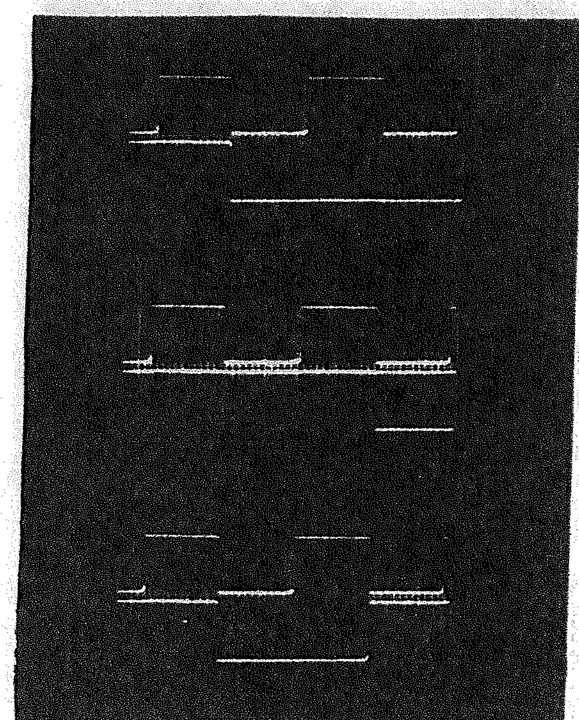
Figure 3. 3. 2-2 Data and Timing Signals - SWS

Data Processor Y



(a) Data and Data Demand

Both 2v/cm
1ms/cm



(b) Data and Shift

Both 2v/cm
200μs/cm

3. The programmer gates that provide commands to the switchable power supply for the ±35, ±350 and test oscillator sequence failed.

4. The six gates in module B-105 failed.

3.3.3.2 CPLEE System Tests

Preliminary system integration tests were started on 27 January with the ALSEP Central Station. These tests were performed with the experiment operating under ambient pressure, and the switchable power supply and channeltron power supply were disabled.

Preliminary checks of experiment response to commands, to ETS data print out format, housekeeping and power line noise were made before difficulty in the ALSEP uplink equipment prohibited further testing on the 27th. On Monday, the 30th, all tests were completed which could be run with the experiment operating under ambient pressure.

Figure 3.3.3-1 depicts the current transient caused by the CPLEE power converter. Repetition rate is 56μsec, corresponding to an 8.3 KHz converter frequency. Figure 3.3.3-2 was taken at a fast sweep speed and depicts a current rise time of greater than 130 A/ms. The ICS value for this parameter is 200 mA/ms. Figure 3.3.3-3 depicts the current transient caused by the 20 ms dust cover removal pulse. Power converter noise at the 56μ sec repetition rate causes the blurred image. The 50 mA transient within the specification limit for this function.

3.3.4 Lunar Surface Magnetometer

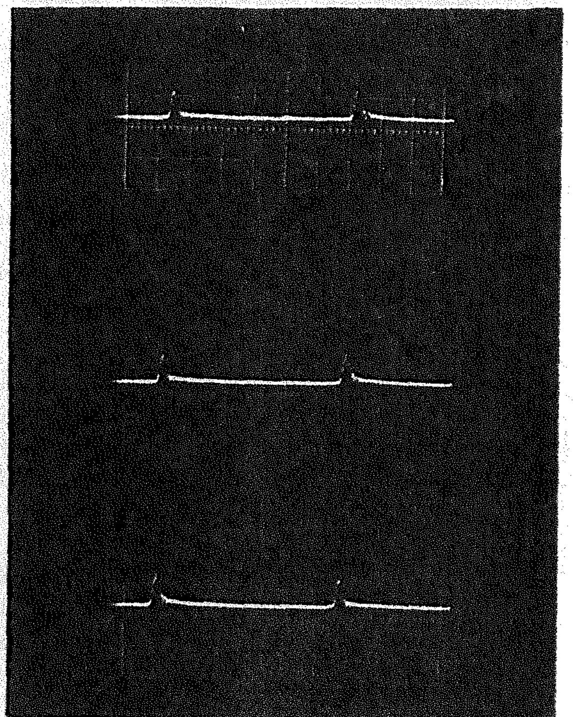
The testing of the LSM breadboard was conducted during the month of December and is summarized in the December Progress Report, ATM 604.

The deliverable LSM ETS was received at BxA on 30 January and the EM is scheduled for delivery on 7 February.

3.3.5 Suprathermal Ion Detector Experiment/Cold Cathode Guage Experiment

SIDE/CCGE breadboard tests were also completed in December and reported in ATM 604.

The breadboard is being returned to BxA by 6 February to be used to commence Category #3 and #4 tests. The present schedule calls for delivery of the SIDE EM to replace the breadboard prior to completion of Array "A" Category #4 tests.

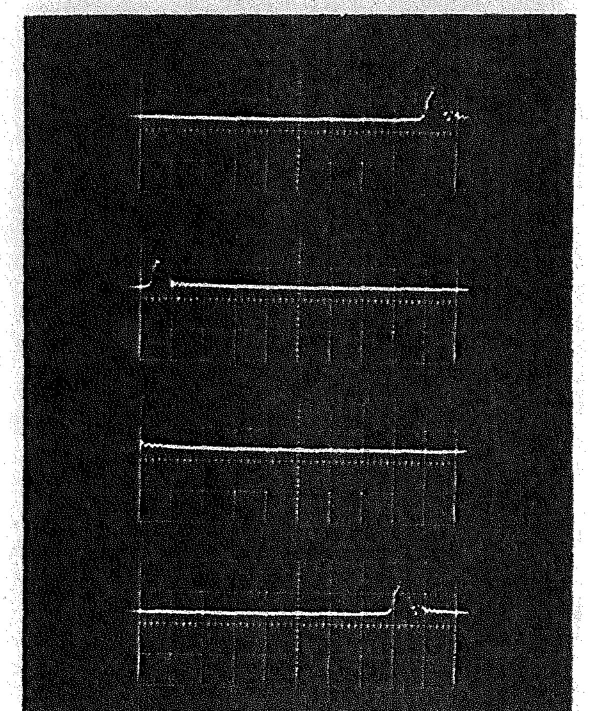


200 mA/cm

10 μs/cm

Zero Current at Center of Grid

Figure 3.3.3-1 CPLEE Power Converter Current Transient

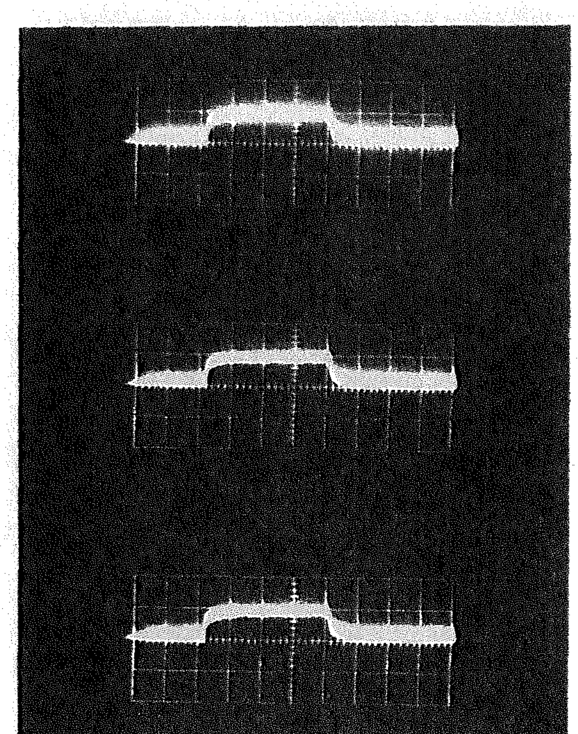


200 mA/cm

5 μs/cm

Zero Current at Center of Grid

Figure 3.3.3-2 CPLEE Power Converter Current Transient



50 mA/cm

5 ms/cm

Figure 3.3.3-3 CPLEE +29 v
Current During Dust Cover
Removal

3.3.6 Active Seismic Experiment

Figures 3.3.6-1 and 3.3.6-2 shows the ASE EM configuration. The mortar box electronics is not shown.

The ASE electronics for the thumper, mortar box, and Central Station Electronics was assembled and checked out at the component level using the ASE ETS and laboratory equipment.

The mortar box with the Engineering Model II GLA was shipped to White Sands and live grenade firing tests performed. These tests are considered a partial success with all four grenades fired and three-out-of-four detonating on impact. However, the mortar box over turned when grenade #1 was fired. This fault was attributed to improper repair of damage to the #1 launcher which occurred during a firing at SOS in November.

ASE receiver-antenna electric field strength measurements were performed over grenade deployment distances to verify the time-break link design. A simulated mortar box was used during these tests.

ASI detection tests were successfully completed with the brassboard thumper.

The ASE Central Station Electronics has operated off line with its Experiment Test Set. The interfaces between ASE and SBOB, Data Output Monitor Equipment and SBOB, and Central Station and SBOB have been checked out. Some difficulty in obtaining proper turn-on sequencing has been experienced during off line tests. Integration tests of the ASE and Central Station were commenced 1/31/67.

3.3.7 Dust Detector

The dust detector was integrated with Central Station on 17 January as originally scheduled, the outputs were read out through the Central Station and all were within the anticipated values. The experiment was powered by external $\pm$ 12 v supplies. Provision for the PDU to supply voltages and for on/off switching is provided in the prototype. The experiment was removed for further thermal tests and returned to EM system tests on 30 January. A seperate report is being prepared on the details of these tests. Figure 3.3.7-1 shows the EM Dust Detector.

3.3.8 Experiments Power Converter Noise

A fault common to all experiments and initially to the Central Station PCU is the introduction of noise spikes on interfacing lines. These spikes are most pronounced on the power and analog signal lines but are observable on all interfacing lines. The source of these noise spikes is the switching transients in the experiment power converters. In general the spikes are at double

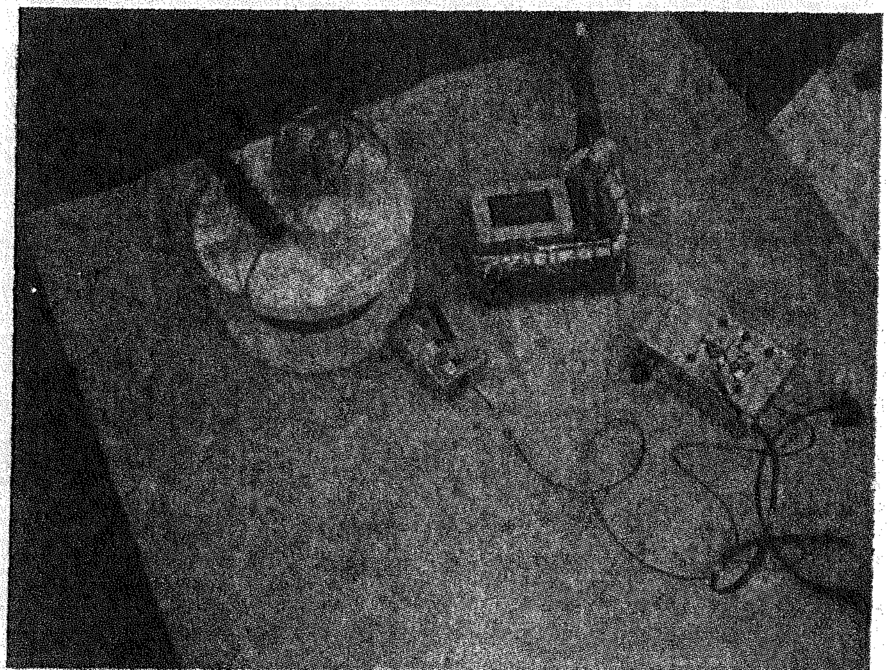


Figure 3.3.6-1 ASE Showing Central Station Electronics, Geophones, and Dummy Thumper

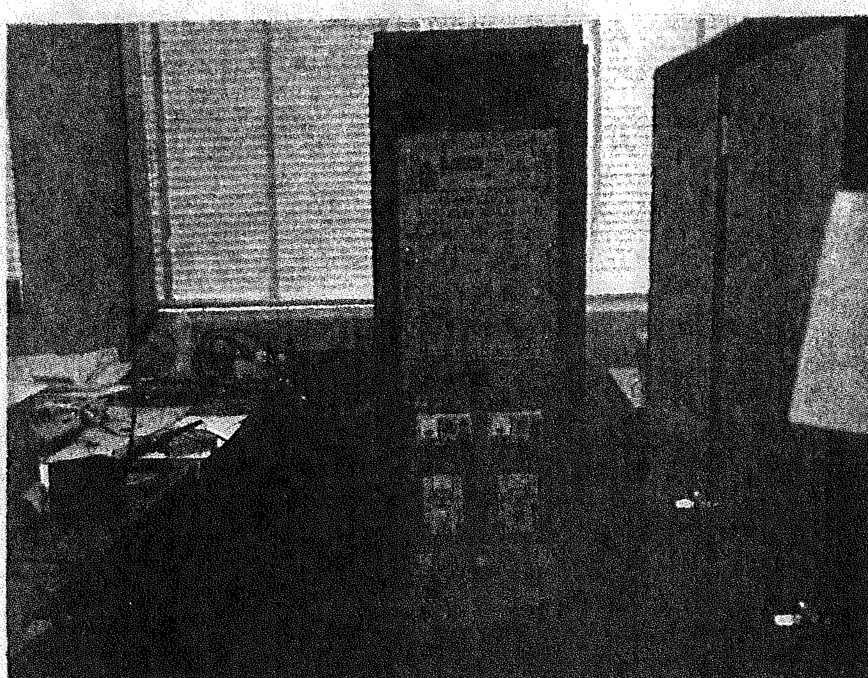


Figure 3.3.6-2 ASE, Experiment Test Set

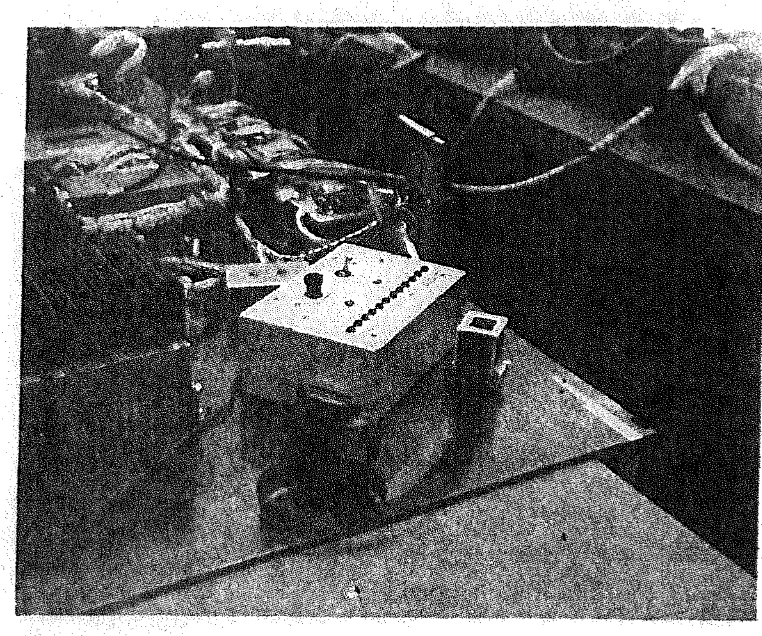


Figure 3.3.7-1 Engineering Model Dust Detector

the power inverter frequency and have a duration of a few microseconds. The detailed characteristics of these noise pulses are shown in Table 3.3.8-1.

Apparently the noise radiated within the component box containing the DC-DC converter is induced on all lines within component box. Filtering the output lines of the converter portion of the experiment without providing addition EMI containment appears ineffective since the noise is radiated around the filters and picked up on other lines. A brute force approach was applied successfully to the Central Station PCU. This approach incorporated a separate EMI enclosure within an EMI enclosure. The inner enclosure contained the EMI sources, (i.e. the regulators, inverters, switching, and rectifying circuits) while the outer enclosure contains filtering for all input and output lines. This approach reduced the noise on all PCU lines to less than 100 mv. An alternate approach involves applying special circuit elements directly at source of noise to reduce the switching transients. This approach is not recommended unless experimenter has considerable experience with these techniques. The best approach is a combination of both techniques.

The full significance of these noise spikes on system operation and the interaction between experiments will not be known until Category #3 testing. This noise is a serious problem in any experiment (such as PSE, ASE, or HF) where low level analog signals are being digitized. Of the experiments tested to date, the effects of power converter induced noise on the data outputs has been most pronounced on the PSE science channels and the SIDE analog channels.

4.0 ENGINERING MODEL SPECIAL TEST EQUIPMENT

Two items of special test equipment for Engineering Model Tests were completed during this period. They are the Data Output Monitoring Equipment (DOME) and a false command generator.

4.1 DATA OUTPUT MONITORING EQUIPMENT

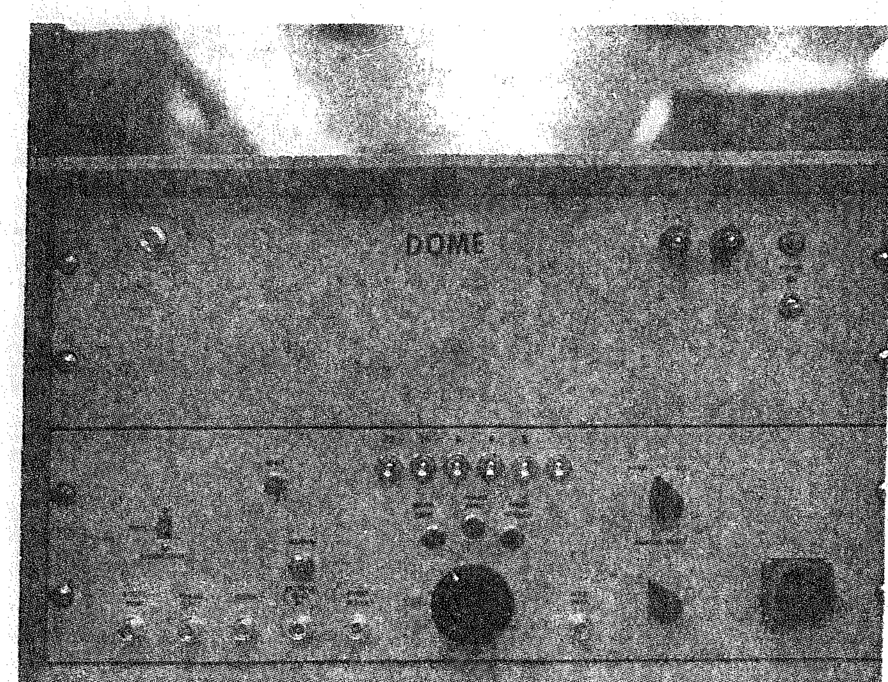
DOME contains the necessary logic and interfacing to allow both printing and digital-to-analog conversion of the data from the Active Seismic Experiment and could be modified to accommodate the Heat Flow Experiment. This equipment was necessitated by the fact that the current downlink display and print out equipment (DPS 1000) is not capable of print out at the ASE rate of 10.6 KHz. Also the ASE test set does not produce hard copy. The DOME is shown in Figure 4-1. It is designed to operate with a high speed printer using signals obtained from the ASE SBOB. In addition to the printed output, the DOME supplies an analog output converted from the digital data. This may be displayed and/or recorded on a scope or a strip chart recorder.

TABLE 3.3.8-1

EXPERIMENT INDUCED NOISE SPIKES

Experiment	Inverter Frequency KHz	Repetition Rate KHz	Noise Spike Duration μsec	Ringing Frequency MHz	Noise Spike Amplitude Peak-to-Peak Power Lines	Noise Spike Amplitude Peak-to-Peak Analog Lines
1. PSE	~ 27	~54	3	2	~1.5 volts	See 3.3.1
2. SWE	2.7	4.3	7	0.6	~200 mv	
3. LSM Breadboard	____	____	____	____	~600 mv	
4. SIDE/CCGE Breadboard	5	10	3	3-4	2-4 volts	4-5 volts
5. CPLEE	8.7	17	2	____	2.5 volts	

Figure 4-1 Data Output Monitor Equipment



The DOME uses two timing lines from the SBOB, clock and frame mark. The NRZ data may be obtained from either the SBOB or the GSE Downlink Demodulator. A front panel switch selects direct or downlink to adjust the synchronizing conditions for these two data sources.

The printer section has three modes of operation, word print, frame print and event search. In either word print or frame print, print out occurs once per ASE frame.

In word print, the word in the ASE frame which is selected is printed repeatedly. In frame print, each word in the frame is successively printed starting with word number 63 (77 octal) and ending with word number 0.

In the event search mode, the DOME searches for an event mark corresponding to grenade detonation or thumper "thump" and having found one prints the following word. This word contains a bit counter which shows the number of bit times by which the real-time event (grenade detonation or thump) preceeded the event mark.

Also there are two printing formats, housekeeping and scientific, which may be selected. In the housekeeping format the eight most significant bits are printed out as 3 octal digits while in the scientific format the 3 seven bit ASE subwords are printed out as 3 octal digits each.

The D-to-A converter outputs an analog equivalent of any one of the three-seven bit ASE subwords selected. A conversion is made for each ASE word, i.e., at the word rate of about 500 per second. The analog output is held between samples. This D-to-A is independent of the printing operations and is continuous.

4.2 FALSE COMMAND GENERATOR

The LK-1, when connected to a laboratory pulse generator and to any command line through an SBOB, will cause a false command of variable width on the line, command pulse widths from 50 nanoseconds to 20 milliseconds can be obtained. It is capable of driving up to 25 lines simultaneously. It will be used to test the immunity of the experiments to false commands and noise of less than standard width.

5.0 STATUS AND SCHEDULE

The Engineering Model Tests are proceeding according to the schedule contained in the December EM Progress Report, ATM 604. Category #2 tests on SWE and PSE were completed on 19 and 23 of January, while Category #2 tests were in progress on CPLEE and ASE at the end of the report period.

The Mod 14 RTG was integrated with the EM Central Station and operated continuously for about 14 hrs on 26 and 27 January.

Present schedule calls for replacement of the DSSTS with STS #1 in early February and commencement of Category #4 tests on about 13 of February. One potential problem in maintaining Category #4 schedule is the absence of data limits and calibration curves for the experiments data. An effort is presently underway to obtain best available data for use with STS in EM tests.

APPENDIX A

ENGINEERING MODEL SYSTEMS INTEGRATION TESTS - BRIEF LOG

Date	Comment
1/3/67	Investigation of noise on PSE data lines with Dr. Lathan in attendance. Photographs taken of noise on power and analog lines. Up to four bits of noise observed on data lines.
1/4/67	PSE ETS failed to shift particular patterns due to lack of driver stages on clock line. ETS modified to include additional drive capability. Investigation made of apparent turn on of experiment in random rather than preset mode. Determined that ETS voltage feedback was cause of problem.
1/5/67	Performed test sequence 211.
1/6/67	STS #1 installed in laboratory and operated with the Central Station. STS modified to send commands without use of computer and to display via DDS 1000. Program to read word 33 checked out.
1/7/67	Continued check of STS capability to read word 33. Logical fault in DPS 2000 program determined.
1/9/67	RF links installed and checked. System operated via STS RF link for morning. Multiplexer calibration checked. RF link fault in GSE receiver necessitated change over to hard link during afternoon. All commands executed properly.
1/10/67	No operation due to failure of DSSTS to be returned from calibration laboratory as per schedule. Partition installed in laboratory.
1/11/67	DSSTS reinstalled. Attempt made to operate RF equipments. Transmitter A and switch removed from system for further MSFN compatibility tests at MSC.
1/12/67	Documented PSE turn-on, turn-off transients and waveforms via oscillograph photographs.
1/13/67	Continued documentation of PSE interface characteristics. Installation of water hoses for cooling RTG transducer.

1/16/67 PSE operation during PCU changeover investigated. ASE work moved to EM laboratory area.

1/17/67 Unsuccessful attempt of operate system via RF. GSE receiver faulty. Broken wire in command decoder found and repaired. SWE put on line for completion of Category #2 tests.

1/18/67 Demonstration of system operation for MSC meeting with SWE and PSE on line. Continuation of documentation of SWE interface signals.

1/19/67 Completion of SWE tests.

1/20/67 Mod 14 RTG brought in and uncrated in laboratory.

1/23/67 RTG assembled in laboratory. Power dissipation measurements made on all components of the Central Station.

1/24/67 Continued investigation of PCU voltage, load characteristics. Investigation of ripple off.

1/25/67 Checkout of CPLEE interface. Attempt to put CPLEE on line unsuccessful due to lack of proper intercabling. RTGSBOB check out completed. RTG V-I plotting commenced on subsystem basis.

1/26/67 Checkout of RTG interfaces and completion of RTG SBOB. RTG connected and operated the Central Station and operated continuously for 14 hours. Completed data on system transient and steady state response with varing system powerloads.

1/27/67 Completion of Mod 14 RTG integration tests. RTG power off. Bad snow storm few people in. Continued preparation of CPLEE for integration. CPLEE operated with Central Station. All command response normal. DSSTS failure to send commands.

1/30/67 DSSTS repaired. Oscillograph photographs taken of CPLEE interface signals. Data output monitor equipment checked out with ASE and Franklin printer. Checkout of ASE SBOB.

1/31/67 Rewiring of Central Station wire harness for ASE preintegration checks completed. First test made with ASE.