Bendix
Aerospace Systems Division

Investigation Into the Scrambling Of Array E Qualification Model PDU Relays at Turn-On

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ABSTRACT

During the C/S Functional Test (TP2365551) on the Array E Qualification Model, it was determined that the initial position of PDU relays following a slow turn-on resulted in a scrambled status. This discrepancy was documented in DR AC4186 and FR E6.

This report documents the analysis and design change to be incorporated in the PDU to eliminate this discrepant operation.

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1.0 INTRODUCTION AND SUMMARY

During the Array E Central Station Qualification Tests it was noted that some relays in the PDU were not in the correct positions at turn-on, leading in one case to lock-out of the uplink. Trouble-shooting established that (a) the scrambling was definitely associated with the turn-on, rather than the previous turn-off, (b) it occurred only in low power out-of-regulation or slow turn-on conditions, and (c) it always affected the same few relays.

The initial assumption was that the scrambling was due to leakage currents in the command lines, but this was proved to be incorrect.

It was eventually established that the Command Decoder was emitting spurious commands as the +5volt supply (V_{cc}) to the output gates rose through the +2 volt level. This had been suggested as a theoretical possibility early in the Array E program (Reference #1), but it had never been observed during the DVM testing in any of the 158 (79 + 79) active command outputs.

The proposed corrective action is to use an automatic voltage-sensitive switch to hold off the +5 volt supply to the first stage of the relay drivers, until the Command Decoder logic chips have passed through the critical region.

This ATM outlines the investigation and explains the mechanism by which the spurious commands are produced. It gives the rationale for selecting the proposed +5 volt switch in preference to other methods, and shows that on the basis of worst-case analyses and initial breadboard tests the switch should provide a satisfactory solution over the Qualification temperature range.

2.0 LEAKAGE CURRENT INVESTIGATION

2.1 BACKGROUND

The original DVM relay drivers had an excessively high gain and responded to any small disturbance or leakage current. Reliable control of relay status was impossible. The temporary cure in the DVT model was to add 100K ohm pull-up resistors to each relay command line, as in Figure 1. (See also Reference #2). The permanent "fix", which was applied to the Qual model, was to redesign the relay driver circuits so as to reduce their gain to a level compatible with the available command line input.

When the Qual model relay scrambling occurred, the new relay driver circuits were analyzed for most efficient operation. It was found that command line leakage currents of 10 microamps might cause unwanted switching. Assuming that leakage currents were the answer, then the source had to be reverse currents into the logic "1" output of the TTL 54L command output chip (See Figure 1.)

2.2 TESTS ON TTL 54L GATE

Tests were run on eight TTL 54L gates. Earlier tests had shown reverse logical "1" leakage currents in the order of 4 nanoamps, but those measurements were taken with all inputs at logical "0". A theoretically more severe test, and one which would be representative of the operational situation, was to take one or more inputs to the logical "1" level, leaving only one input at the logical "0" level in order to maintain the logical "1" output. The test results in this case showed little difference from the previous set. Except for one gate with a reverse logical "1" leakage current of 60 nanoamps, all the gates had leakage currents of less than 10 nanoamps. Even the 60 nanoamp current was far below the minimum necessary for spurious switching. Since it was also difficult to reconcile the leakage theory with the obvious system stability at normal voltage levels, this approach was abandoned.

3.0 SPURIOUS COMMAND INVESTIGATION

3.1 ASSUMED MECHANISM

A TTL 54L gate is a four-transistor amplifier, as shown in Figure 2. Although the manufacturer provides no data or guarantees for operation at V_{cc} outside the range 4.5-5.5 volts it has been established by Bendix tests that at room temperature a gate cannot respond correctly as a logical element until the V_{cc} is equal to or greater than approximately 2 volts. The reason for this is clear from Figure 2; until V_{cc} exceeds (3 x V_{BE}) plus a small drop across the input stage 40 K ohm resistor, it is not possible to drive the lower half of the output stage hard on, and hence impossible to generate a logical "0". Assuming that the (3 x V_{BE}) model is correct, and assuming a diode temperature coefficient of -3 millivolts per degree Centigrade per diode, the gate characteristics should be as shown in Figure 3. (At the present time no high and low temperature test data are available.) Over the Qualification temperature range the predicted critical V_{cc} level varies from 1.5 to 2.5 volts.

By inference from data for other transistors, supported by tests on the eight TTL 54L gates, the tolerance on the critical V_{cc} level at any temperature should be about $\pm$ 100 millivolts, or less.

Figure 4 shows the mechanism by which a spurious command can be produced. It is particularly important to note that it is not the property of a single gate, but the relative critical levels of successive gates which generates the command.

Figure 4(a) shows a typical decoding stage - two multiple input gates (A and B), driving a single two-input gate, (C). When the V_{cc} is below the critical levels for all three gates then, from Figure 3, the outputs of all gates, and in particular the output of Gate C, will be a logical "1", i.e., no command. As the V_{cc} rises, first one gate then another will reach its critical level and begin to operate according to the normal logical gate rules. If gate C comes into operation before gates A and B, as in Figure 4(b), then it will see only logical "1"s at its input, and it will therefore set its output to a logical "0", i.e., a spurious command. As soon as gate A and/or gate B generate a logical "0", gate C will revert to a logical "1" output, and the spurious command will be terminated.

If gate C comes into operation at a higher V_{cc} level than gates A or B, as in Figure 4(c), then no spurious command will be generated. The length of a spurious command pulse which is generated by the above mechanism is a function of the spread of the critical levels and the rate of rise of V_{cc}; if the rate of rise is fast enough, then the spurious command pulse will be too short to operate a relay. Assuming a critical level spread of 200 millivolts and a minimum effective pulse length of 0.5 milliseconds, then a rate of V_{cc} rise in excess of 400 volts/second at the critical level should give immunity to relay scrambling.

Figure 5 shows the typical way in which the Command Decoder V_{cc} rises following the application of power to the system, or during a PC changeover. The plateau between 2.0 and 2.5 volts is the result of the turn-on transient temporarily causing the APM circuit to dump maximum power. Also marked on Figure 5 are the predicted critical V_{cc} levels at various temperatures, the current advice being that the PCU turn-on characteristic itself should not vary significantly with temperature. Note that at +70°C the critical V_{cc} level corresponds to a relatively high rate of rise, whereas between +25°C and -30°C there is a critical level corresponding to the slowest rate of V_{cc} rise. It is therefore expected that the probability of scrambling will increase at low temperatures.

A falling V_{cc} at turn-off or PC changeover will also generate spurious command pulses, but they will almost certainly always be too short to be effective.

If it is assumed that the critical levels of gates are random with respect to each other and that each gate is selected at random from the same batch, then it is easily shown that the multi-input gates A and B in Figure 4(a) have a high probability of generating logical "0"s at their outputs immediately they come into normal operation. On this basis it would be expected that the probability of a spurious command at any specific output would be between 1 in 3 and 1 in 4. Although it is impossible to predict the behavior of any specific output beforehand, it may be assumed that once the tendency to "spurious command" or "no spurious command" has been determined it will remain consistent from then on. The design changes defined in paragraph 4.1 will inhibit this initial spurious command condition.

3.2 EXPERIMENTAL OBSERVATIONS

The most persistent scrambling situation in the Qual Model was Experiment #4 changing from "Off" to "Standby" during turn-on in Uplink B, to a just-in-regulation condition. (Transmitter B changing from "Off" to "On" was also noticeable). Since an "Off" to "Standby" change is a "forbidden" change, it was assumed that the spurious command pulse was actually occuring on the "Operate" or "On" command line, and that the eventual "Standby" state was the result of a ripple-off. The Experiment #4 "On" command line and the PCU +5Volt supply line were therefore monitored with an oscilloscope. At turn-on a pair of traces similar to those in Figure 6 were seen, exactly as predicted. The relatively long 7 millisecond command pulse was assumed to be the result of the Experiment #4 load slowing the rate of rise of V_{cc}, thereby holding it in the critical region for an extended period. Other command lines showed "glitches" at the predicted point, but most were neither deep enough nor long enough to be an effective command.

Although the spurious command mechanism had been satisfactorily confirmed, there was not (and still is not) a completely proven explanation for the very low probability of occurrence. In Section 3.1 it was predicted that approximately 1 in 3 to 1 in 4 command lines should show spurious pulses at the critical V_{cc} level. The fact that so few spurious executions occurred in the Qual model,

and that none occurred in the DVT model, is attributed to closely similar critical levels within a batch of chips and/or the fact that the first and second tiers of decoding gates are of different types and cannot therefore be selected at random from the same batch. Following this line of argument leads to the conclusion that it is quite possible that in the worst case every command line in the Flight model could carry a spurious command at turn-on. Some means of protection is therefore essential.

4.0 PROPOSED "FIX"

4.1 RATIONALE

If only the initial lunar turn-on were involved, and if a high temperature, high powered turn-on could be guaranteed, then the system would probably be satisfactory without any modification, However, to be safe under other conditions, including PC changeover, it is necessary to consider doing one of the following:

(a) delay the application of the +5 volt V_{cc} to the Command Decoder until it is certain that it will rise to a point above the critical level at more than, say, 500 volts/second, under all conditions.

or (b) delay the +29 volt relay supply to the PDU until the Command Decoder V_{cc} has risen above the critical level.

or (c) delay the +5 volt (Z) supply to the first stages of the PDU relay drivers until the Command Decoder V_{cc} has risen above the critical level.

or (d) operate the final Command Decoder output gates at a V_{cc} about 200 millivolts below that for the other gates in the Decoder.

or (e) adjust the PDU relay driver gains and/or V_{cc} so that the drivers cannot operate at voltage levels corresponding to the Command Decoder critical level V_{cc}, but can be guaranteed to operate at normal V_{cc} levels.

or (f) crossfeed from the +16 volt input line to the PCU +5 volt output lines, via a zener diode network and isolating diodes, so that the +5 volt line reaches about +4 volts very rapidly, before any other circuits can respond. When the +5 volt PCU output exceeds +4 volts it will take over from the auxiliary input.

In a new design the recommended approach would be (d), but this is clearly impracticable for existing hardware. Approach (e) is also impracticable for existing hardware, and in any case it could present a difficult design problem, almost certainly requiring special selection of parts to very tight tolerances at all temperatures. If the minimum supply voltage at which the drivers could work was set too high then a heavy overload could produce a lock-out situation. Approach (f) could be implemented, but it produces some difficult reliability and power loss problems. Approaches (a), (b) or (c) could be partially implemented by an additional astro-switch; however, the PC changeover case would not be covered and there would be operational constraints. A simple RC delay, in the cases of (b) and (c), would not satisfactorily cover the low temperature, low power case, nor a slow turn-on.

The only completely satisfactory solution is an automatic, level-sensing switch. Since the problem is related to the +5 volt supply, the +29 volt approach, (b), is less preferred than (a) or (c); power considerations also make the +29 volt switch less attractive. In deciding between approaches (a) and (c) it will be seen that (c) is purely a voltage level system, whereas (a) also imposes a rise-time requirement. Approach (c), a hold-off switch in the +5 volt (Z) supply to the relay drivers, is therefore the preferred solution.

4.2 PRACTICAL DETAILS

Figure 7 shows the proposed switch circuit for the +5 volt (Z) supply, and the associated PDU and harness modifications. The new dual switch module will use the existing Experiment #6 position and the existing circuitry in the PDU. Apart from the removal of the two isolation diodes in the PDM (dump relay) module and the simple harness additions no physical changes will be necessary in existing hardware.

Various combinations of diodes and transistors could have been used in the switch. The TTL 54L/transistor circuit is preferred operationally since the chip should give the best match with the Command Decoder gates over the temperature range. The supply to the switch reference chip is two signal diode drops below the PCU +5 volt output level; the Command Decoder supply is one power diode drop

plus a circuit breaker resistive drop below the PCU +5 volt output level. The reference chip V_{cc} thus tracks approximately one diode drop, less the circuit breaker drop, below the Command Decoder V_{cc}, or: -

$$\text{Margin} = V_{cc}(\text{Command Decoder})_{MIN^M} - V_{cc}(\text{Switch Reference Chip})_{MAX^M}$$

$$-\left(\text{C/D Critical Level} - \text{Reference Critical Level}\right)_{MAX^M}$$

$$\text{i.e.,} \quad = \left(V_{PCU} - \text{Max. Circuit Breaker Drop} - \text{Max. Power Diode Drop}\right)$$

$$-\left(V_{PCU} - 2 \times \text{Minimum Signal Diode Drop}\right)$$

$$-\left(\text{Maximum Spread in Critical Levels.}\right)$$

Note that the margin is not directly a function of V_{PCU}, but assuming a mainly resistive load the drop in the Command Decoder series power diode and circuit breaker will be a function of current, and hence an indirect function of V_{PCU}.

The worst-case switching margins at three temperatures are estimated as follows:

TABLE I

1	Temperature	-30°C	+25°C	+70°C
2	Approx. critical level	2.50V	2.00V	1.50V
3	Approx. C/D current: $(75 \times \frac{\text{Critical level}}{5}$ mA)	38mA	30mA	23mA
4	Max ^{M} C/B drop +Power Diode drop (From Reference #3)	0.86V	0.75V	0.65V
5	Assumed Max^M spread in critical levels	0.20V	0.20V	0.20V
6	4 + 5	1.06V	0.95V	0.85V
7	2 x Minimum signal diode drop	1.40V	1.20V	1.00V
8	Worst case minimum margin = 7 - 6	0.34V	0.25V	0.15V

Selection of parts and/or tests at the module level can ensure that the +5V (Z) switch is biased towards providing the largest margin. The addition of a third diode in the reference chip V_{cc} line would guarantee a wide margin under all conditions, but the V_{PCU} value for switching at -30° C might then go as high as 5 volts, which is unacceptable.

4.3 EFFECT OF SWITCH UPON +5 V(Z) VOLTAGE LEVEL

The insertion of the series transistor switch will cause the +5V (Z) line to drop by $V_{CE\ SAT}$ below its current level. Practical measurements and manufacturers' data have shown that $V_{CE\ SAT}$ will be 0.2 to 0.3 volts at all temperatures, at the nominal 27mA. The existing extreme limit predictions for the +5V (Z) line are 5.0 V to 5.4V (See Reference #3), and hence the additional drop of 0.2V to 0.3V will do no harm. The isolation diodes in the new modules do not cause an additional drop since they simply replace the diodes removed from the PDM module.

4.4 EFFECT OF +5V(Z) SWITCHING UPON OTHER COMPONENTS

The system as a whole is designed for normal operation only at a nominal 5 volts. Unpredictable operation during the turn-on transients is inevitable, which is why all critical flip flops, etc., are preset by power reset circuits. In addition to the PDU relay drivers, the +5V(Z) line supplies the Command Decoder Uplink Switch/Periodic Command counter and the ADP. The delayed rise of the +5V (Z) supply should not affect either of these circuits, or the system, adversely.

5.0 BREADBOARD TEST RESULTS

A breadboard of the proposed 5V (Z) automatic switch circuit was tested at high, medium and low temperatures. The input voltage levels (V_{PCU}) at which the switch operated were compared with the predicted switching levels derived from the theoretical model. Parts for the breadboard were not specially selected.

TABLE II

Temperature	Predicted Extremes	Observed Start of Switch Action	Observed Completion of Switch Action
+70°C	2.4V to 3.0V	2.4V	2.65V
+25°C	3.0V to 3.6V	2.95F	3.2V
-30°C	3.7V to 4.3V	3.7V	3.9V

The test results are in good agreement with the predictions and tend to confirm the accuracy of the model. The load current for the switch was taken to 100 milliamps without any problems, although the normal load current is only 27 mA.

References

1. Bendix Internal Memo 9721-1914, dated 14 December 1970, by R. Dallaire, "Slow Turn-On Characteristics of the Array E Command Decoder".

2. Bendix Internal Memo 9713-316, dated 9 July 1971, by J. E. Kasser, "Uplink Switching Problem During DVT Integration".

3. ATM-1032, by N. Hadwick, "Theoretical Modeling and Analysis of PCU/PDU Output Voltages".

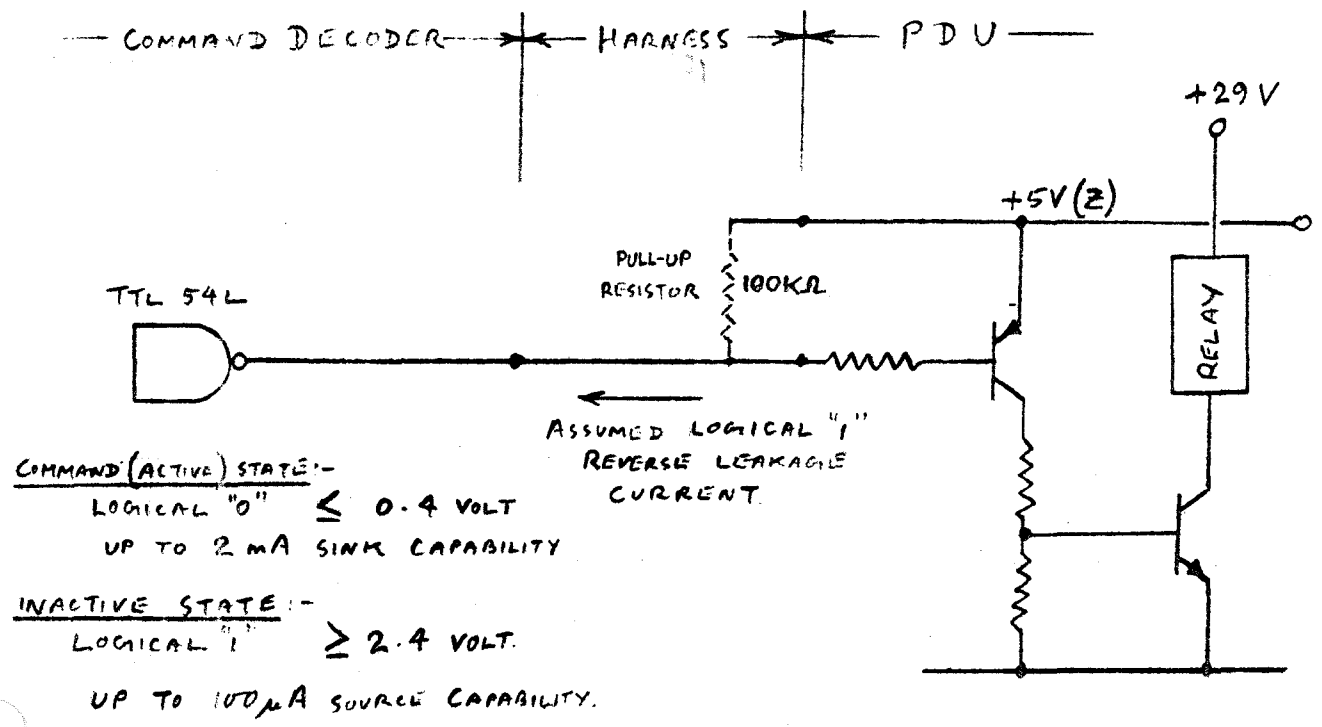


FIGURE 1 :- RELAY COMMAND INTERFACE.

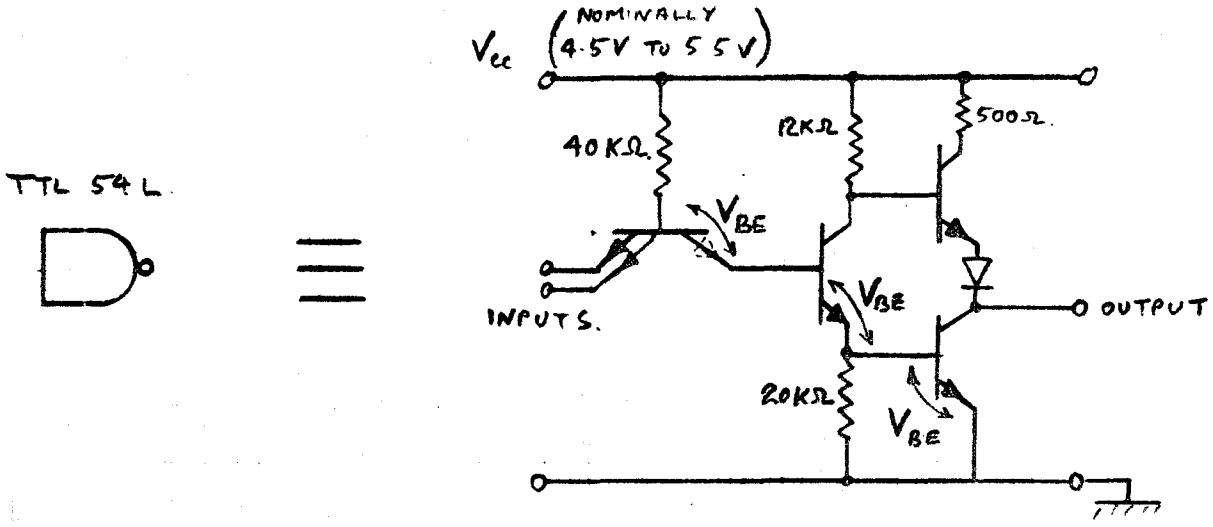
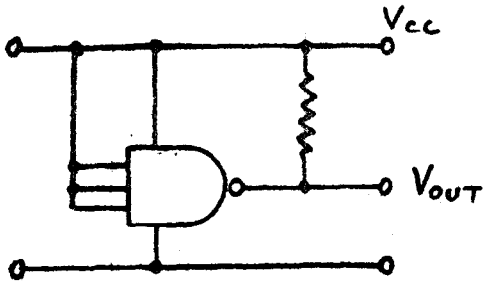


FIGURE 2 :- CIRCUIT OF TTL 54L GATE.



ASSUMED CONFIGURATION.

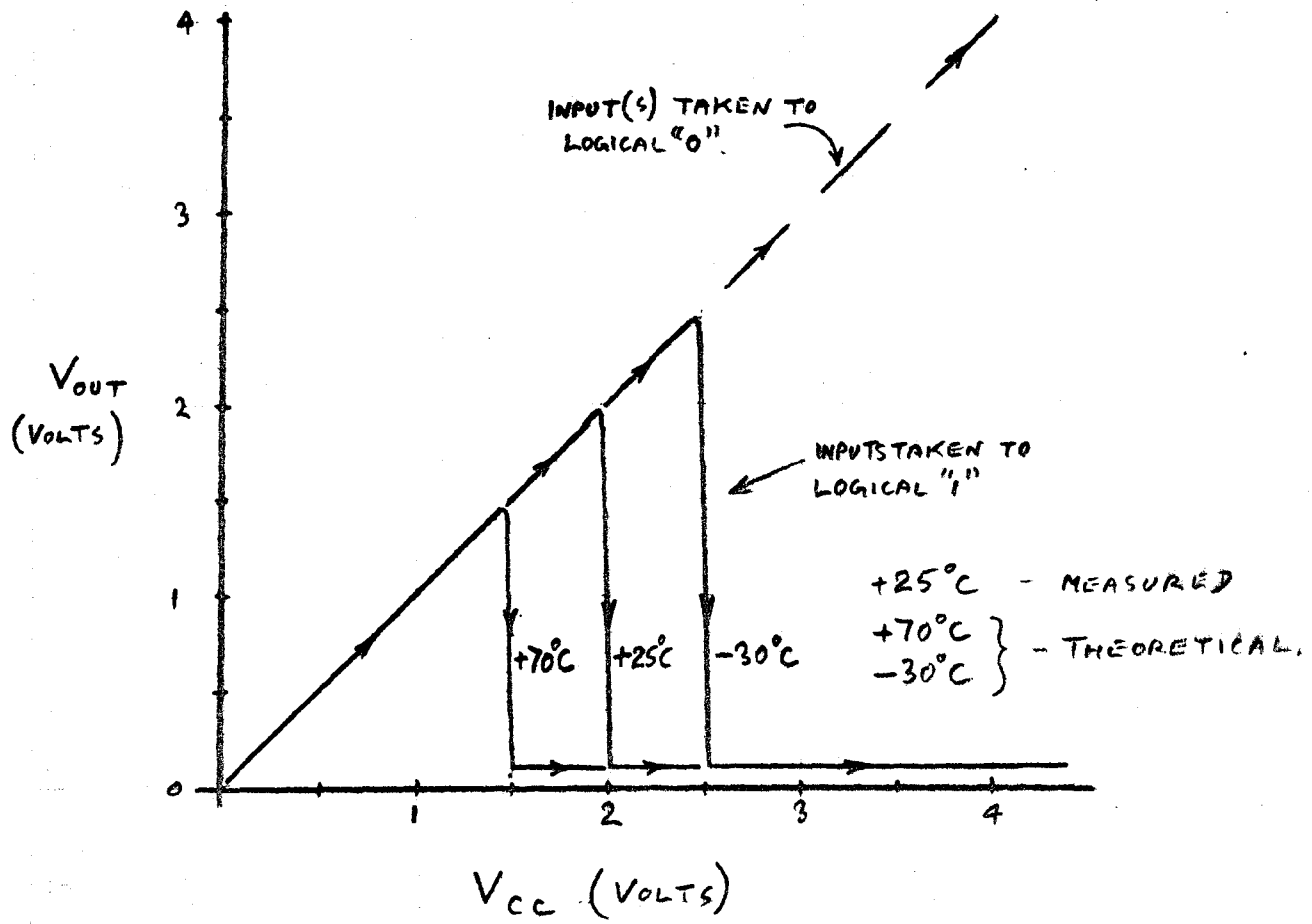


FIGURE 3:- ASSUMED MODEL FOR TTL 54L GATE.

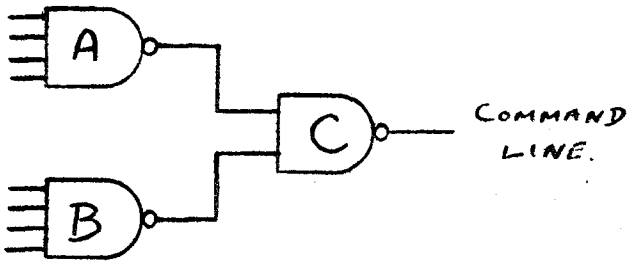


FIGURE 4(a) - TYPICAL COMMAND OUTPUT STAGE

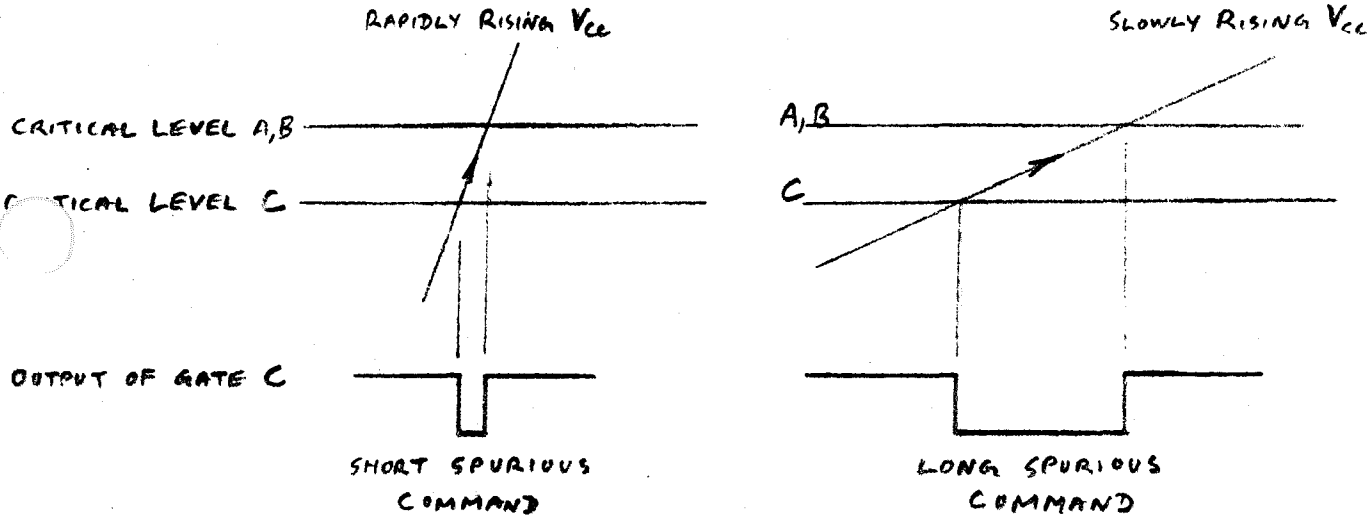


FIGURE 4(b) - GENERATION OF SPURIOUS COMMAND

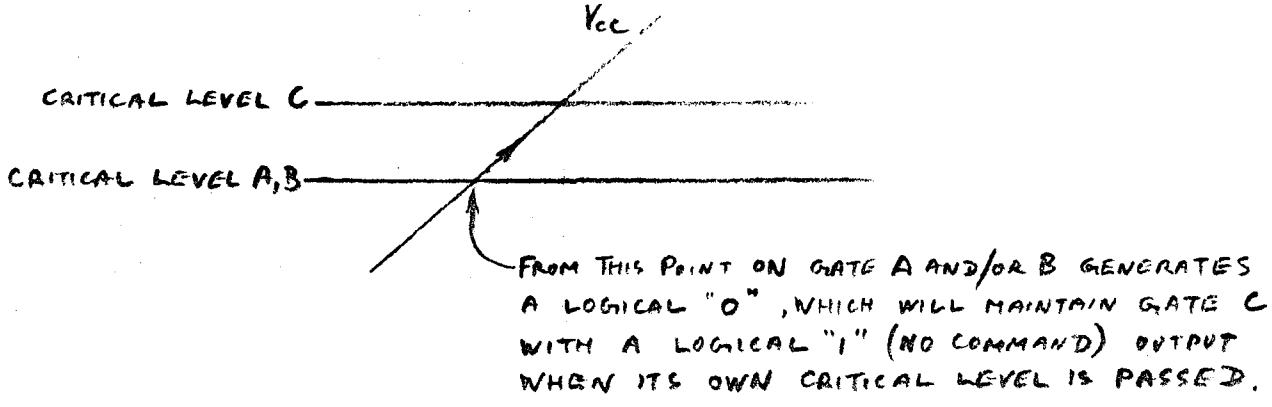


FIGURE 4(c) - CONDITION FOR NO-COMMAND.

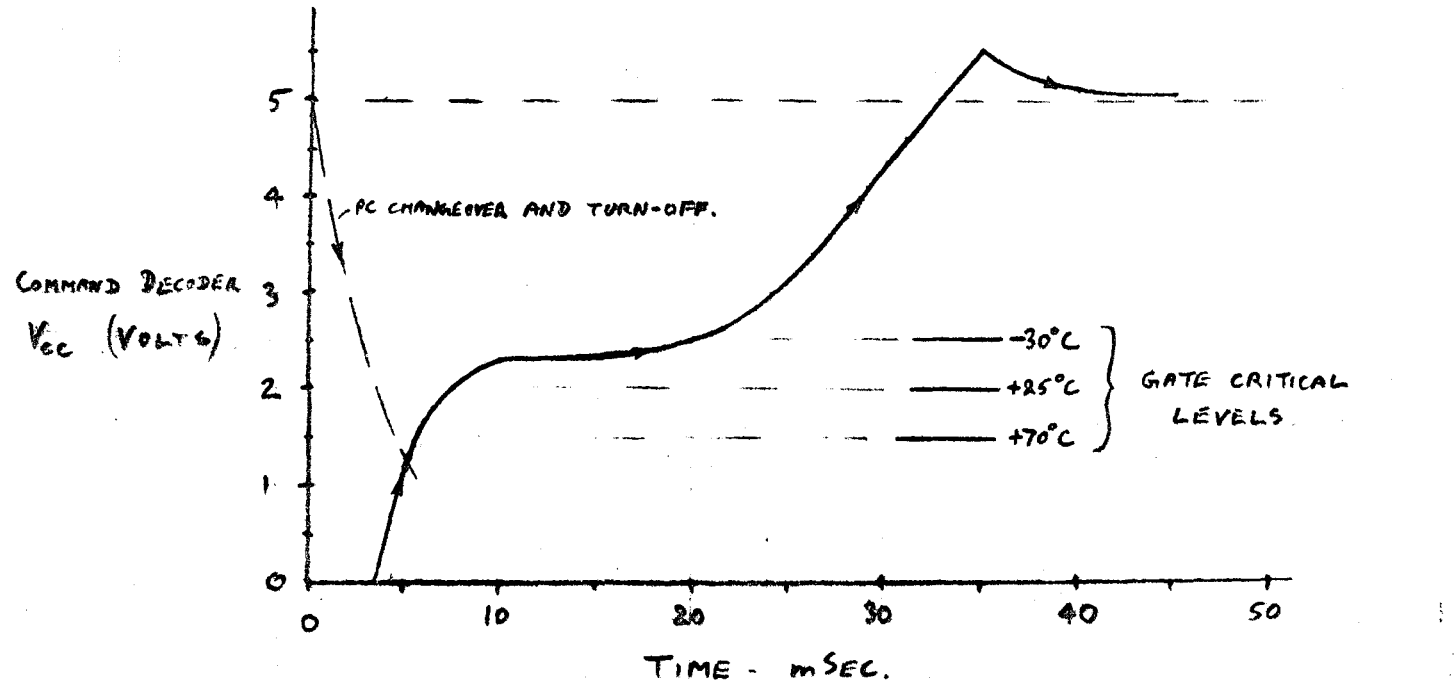


FIGURE 5 :- TYPICAL TURN-ON AND CHANGEOVER TRANSIENT

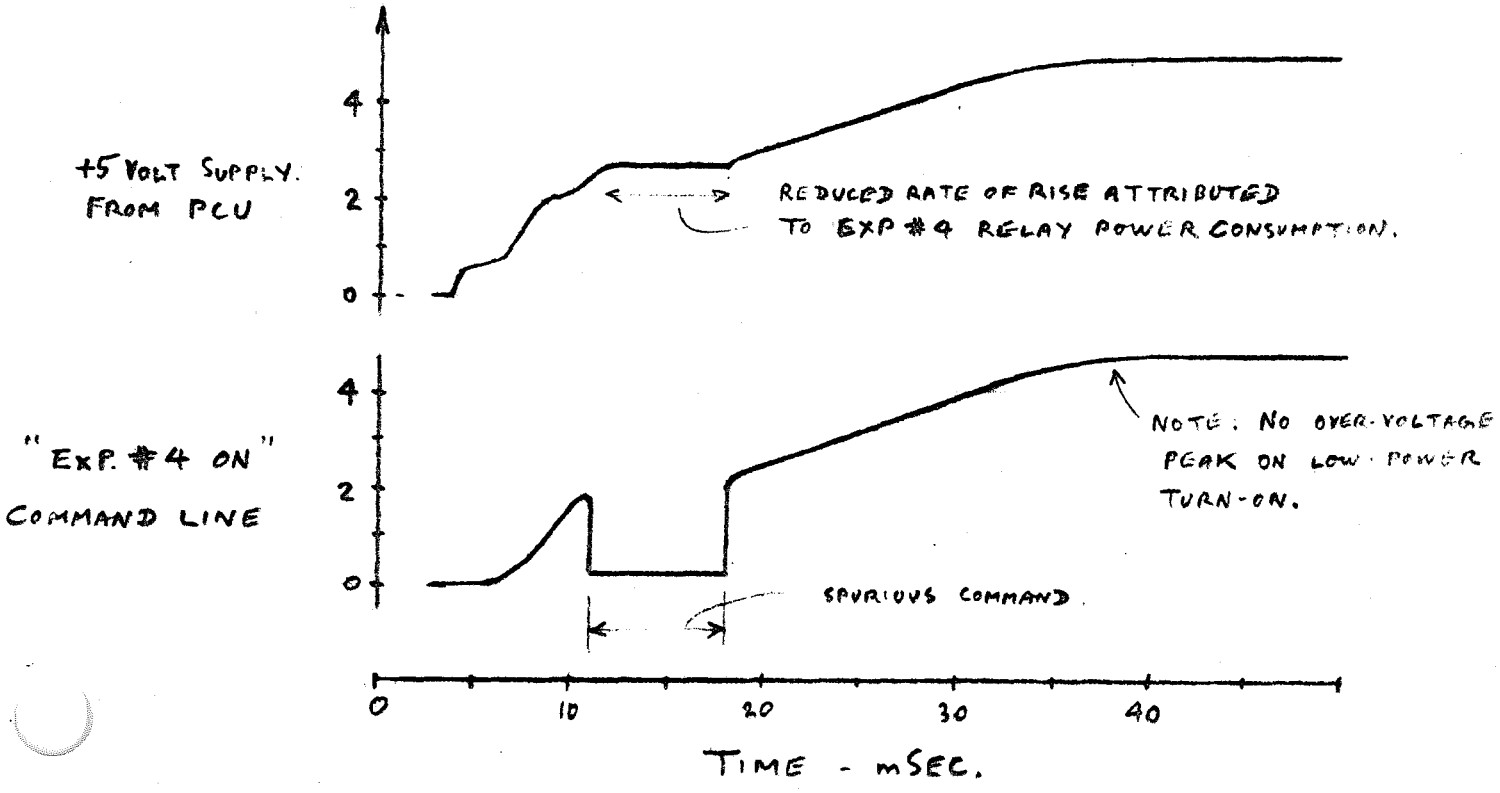


FIGURE 6 :- SPURIOUS COMMAND TO EXPERIMENT #4

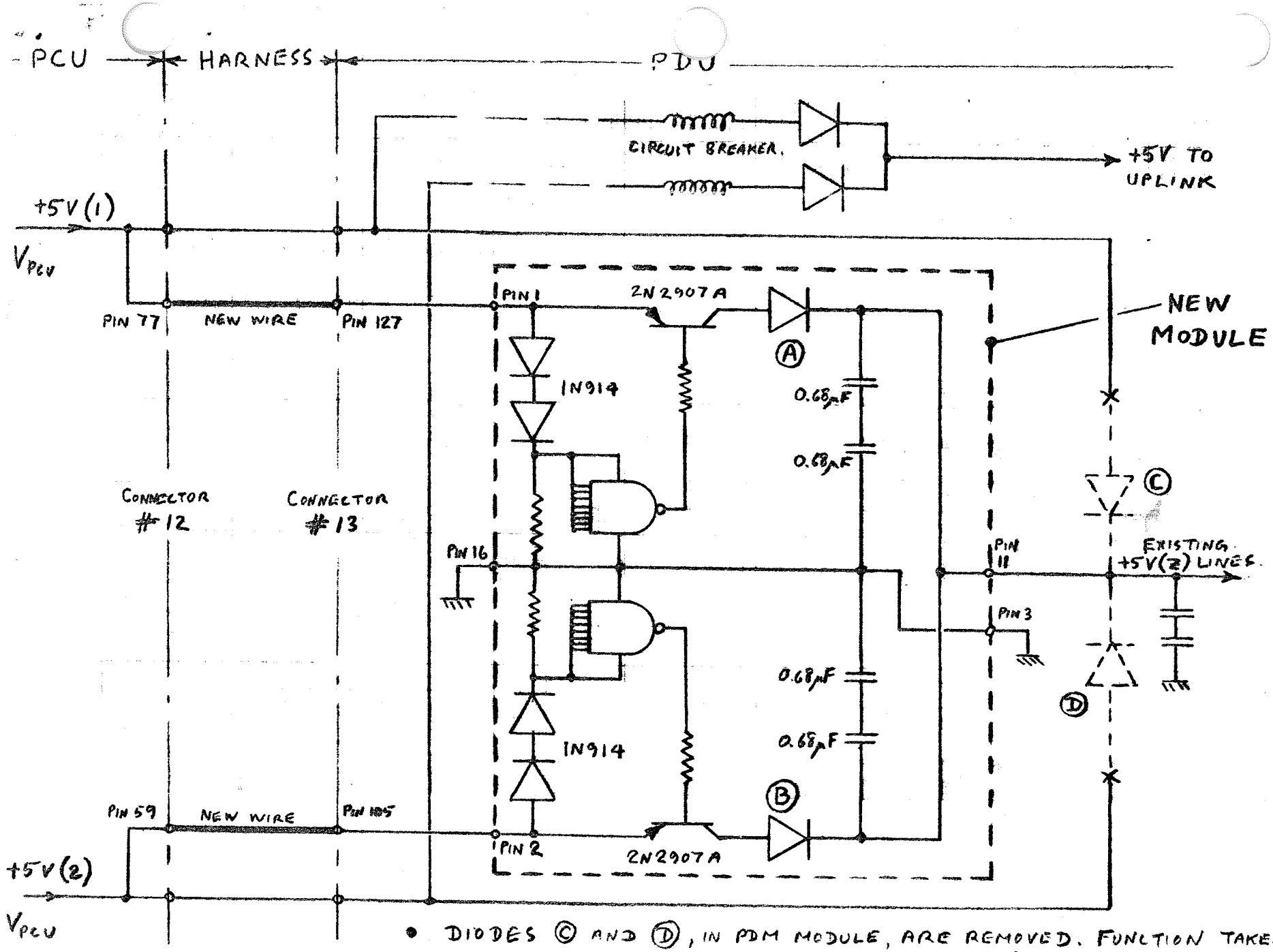


FIGURE 7.

- DIODES © AND ⓓ, IN PDM MODULE, ARE REMOVED. FUNCTION TAKEN OVER BY NEW ISOLATION DIODES Ⓐ AND Ⓑ
- TWO NEW HARNESS WIRES.
- NEW +5V(2) SWITCH MODULE IN EXP #6 MODULE POSITION.
- ALL OTHER HARDWARE REMAINS "AS IS".