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Spurious Status Changes in Array E

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ABSTRACT

During the C/S Verification Test (TP 2368960) on the Array E Qualification Model, several changes of status occurred at turn-on, PC changeover or following other power interruptions. These discrepancies were documented in DR AC 5068, 5069, 5071, 5072, and 5082.

This report documents the analysis of these anomalies, and discusses possible design changes to eliminate the discrepant operation.

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1.0 INTRODUCTION

The Array E Qualification Model Discrepancy Reports which are listed as References #1 through # 5 detail spurious changes of status which occurred at turn-on, PC changeover or following other power supply interruptions. The first three are the result of the same critical V_{cc} mechanism which caused Qualification Model relay scrambling, and which is fully described in ATM-1087 (Reference #6). The last two, Refs. #4 and #5, are caused by unusually high reverse leakage currents into the command output gates.

Where PDU relay scrambling is involved the system could be left in a locked-out condition, but in the case of flip-flop status changes it is always possible to regain the desired status by command.

This ATM discusses each DR in turn and then considers possible ways of eliminating the problems. As in the case of the turn-on relay scrambling, (Reference # 6), it is not possible because of program impact to remove the basic cause of the anomalies by fairly simple design changes. The only practical approach is to attempt to block some or all of the undesired effects by additional circuits incorporated into the harness, with the main emphases upon acceptable operation during an unmonitored automatic PC switchover, and the maintenance of stable relay status at all times.

2.0 DR AC 5068: CHANGE FROM DP FORMATTING TO LSPE FORMATTING FOLLOWING OCTAL COMMAND 110

Figure 1 shows the uplink +5 volt switching circuit. The relay which Command 110 controls selects redundant power routes to the main Select Uplink A/Select Uplink B relays, the redundant routes being necessary to prevent a possible single point failure mechanism in the main relays. Normally the W/X relay will be flown in the W position and will remain there for the whole mission. If an automatic uplink switch does take place, then the W/X relays and the Uplink A/B relay will change simultaneously. Only then will it be necessary to consider transmitting Octal Command 110 with the intention of causing an actual relay changeover, back to the original position. (An Octal 110 command may be transmitted immediately after station turn-on in order to ensure that the W/X relay really is in the W position. However, since no magnetically latched relay has so far changed position due to mechanical causes, and since telemetry channel HK 26 indicates the position of this relay, it is unlikely that Command 110 will need to be transmitted. Even if it is, the only result should be a CVW, with no change of status).



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The typical effect of the X/W relay changeover is shown in Figure 2. The +5 Volts is switched from one redundant power route to the other, and while the relay is in transition the Uplink, and in particular the Command Decoder, is effectively unpowered. The individual PC board decoupling capacitors in the Decoder will discharge very rapidly, and it is quite possible that the +5 Volt V_{CC} line will drop below the critical level. Once the V_{CC} has dropped below 1.5 Volt to 2.5 Volt, depending upon temperature, the subsequent recovery state of any flip-flop will be indeterminate, unless reset by some external input. This lack of memory in symmetrical flip-flops following loss of power is not peculiar to Array E, but in this case it is accentuated by the inability of the TTL 54L gates to function correctly once the V_{CC} is below the relatively high critical level. (See Reference #6). During a normal turn-on, or an Uplink changeover, the Decoder power - reset circuits will operate to initialize all flip-flops in predetermined states; in the case of Cmd 110 the power interruption is too short to trigger the power resets.

Although only a DP to LSPE formatting change has been observed so far, any of the following spurious operations are theoretically possible: -

- a) DP Formatting to LSPE Formatting, or vice versa.
- b) Periodic Command Inhibit to Periodic Commands Enable, or vice versa.
- c) Random setting of the Command Decoder sequencing logic flip-flops, mode sequence counter, and command register, such that one or more spurious commands may be issued.

The commands may range from one of 21 milliseconds, with CVW, indistinguishable from a normal command, to approximately ten 1 millisecond commands, with or without a single CVW. Alternatively a CVW may be received with no corresponding change of status, or the Decoder may temporarily lock itself out, requiring a modulation or carrier break to restore control. It should be noted that for these events to occur several flip-flops must change states into specific combinations, and the overall probability is fairly low.



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There are four ways in which this problem could be overcome: -

- a) Modify the power reset circuits so that they will respond to any voltage reduction, however short, which drops the V_{CC} line below the critical V_{CC} level. This would be the preferred method, if the impact of its practical implementation in Array E were not completely prohibitive.
- b) Bias the turn-on state of every flip-flop in the Command Decoder with capacitors. This method would be simple and effective, but it involves internal modifications and additional parts inside the Decoder.
- c) Deliberately lengthen the interruption to the +5 Volt Uplink supply, so that the internal Decoder power reset circuits will be triggered. This requires the design and construction of a special switch, to be inserted in the PDU/Decoder harness leads. (See Reference #7)
- d) Hold up the Command Decoder +5 Volt line with storage capacitors during the power interruption. Only a few microfarads would be necessary, but because of possible undesirable side effects this approach is not favored. Previous tests have shown that, in curing one problem with similar capacitors, spurious commands were produced due to the much slower V_{CC} run-down at Uplink changeover. The capacitor value is critical, if indeed there is one value which is satisfactory in all respects.

A fifth possibility is to do nothing, based on the following rationale: -

- a) The transmission of Cmd 110 following an automatic Uplink switch is not absolutely essential for continued operation. If the original loss of Uplink was due to a failure in the primary power routing itself, then Cmd 110 would produce a further temporary loss of Uplink, until the next auto-switch.



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However, since we are concerned here mainly with the mechanical failure of a relay, or the shaking of contaminant particles across contacts which are normally never disturbed during the mission, it may be argued that once the system is deployed and is mechanically quiet, then the probability of power routing failure is extremely small. If this failure mode does not occur at deployment, it probably never will. Any subsequent Uplink loss will most likely be due to an electronic failure, and Command 110 is irrelevant in that context.

- b) Whatever undesirable status changes may occur following Cmd 110, they can be quickly corrected, since Cmd 110 can be sent only during real-time coverage.

3.0 DR AC 5069: APM CAME UP IN "OFF" STATE AT TURN-ON (HK-76)

This has been conclusively shown to be caused by a 0.1 millisecond spurious command from the Command Decoder during turn-on. Although a relay would not respond to such a short pulse, (and all PDU relays are in any case protected by the new +5 Volt (Z) switch), it is far in excess of what is required to toggle a flip-flop. Figure 3 shows the relevant circuit details. Although the flip-flop does have a RC power-reset circuit, it has a very short time constant (~ 1 millisecond) and it can do nothing to overcome the effect of a spurious command which occurs several milliseconds after the application of power to the PCU. The only guaranteed solution in this particular case would be a much improved power-reset circuit. Even if the spurious command from the Decoder was completely eliminated, the PCU inverters 3) and 4), and 5) and 6) in Figure 3 are potentially capable of generating spurious commands themselves, although it is possible that in this case they would be swamped by the effect of the existing RC power reset circuit.

The problem of eliminating all spurious commands from the decoder will be considered later. Assuming for the moment that spurious commands to the PCU will continue to be a possibility, the most likely response is the APM status change already observed; it could theoretically occur at initial turn-on or during a PC changeover. Changes of status of the PC Select and PC Autoswitch Select relays are also theoretically possible,



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but circuit analysis in the light of typical operation has shown that the probability is extremely low. (Note that the PCU relays are internally powered and are not protected by the +5 Volt (Z) switch).

Incorrect APM status at turn-on is easily corrected by immediate command, but incorrect APM status following an automatic PC changeover might lead to all reserve power being dumped internally during the lunar day. This could be tolerated for some time, but it would eventually become highly desirable to command the APM "On".

The +5 volt capacitive hold-up circuit discussed in Section 7.4a, Page 13, provides an effective preventative measure in the case of an automatic PCU switch-over resulting from regulator failure in which an overvoltage transient occurs. In this case the switching circuit will operate to transfer PCU's within 5 milliseconds and the 5 volt line will hold up during the switchover. In the case of an automatic low-voltage switchover, however, the auto-switch circuit delays for 300 milliseconds before responding, and in a genuine failure condition, there is no limit to the 5V line voltage drop.

The normal operational rule will be to leave the APM enabled at all times, and it is possible to produce a fairly strong rationale for locking the APM command flip-flop into the "Enable" state, and eliminating the APM commands.

If an automatic PC changeover should occur, the duration of the automatic command is such that it will over-ride any spurious commands which try to prevent it.

4.0 DR AC 5071: UPLINK SWITCH DELAY STATUS CHANGED TO "DELAYED" AT PC CHANGEOVER (HK-01)

This circuit is powered from the +5 Volt (Z) line. The most probable explanation is that during the PC changeover the +5 Volt line dropped close to or below the critical level, causing the 5 Volt (Z) switch to cut off the supply to the flip-flop for a period which was not long enough to trigger the power reset. When the power was re-applied the Uplink Switch Delay/Enable flip-flop came up in an indeterminate condition. Even without the +5 Volt (Z) switch, a sufficiently deep drop in the +5 Volt supply could cause a similar effect; the +5 Volt (Z) switch simply increases the probability.



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Although not observed, similar changes of status could occur in the Uplink Switch routing flip-flop, the timing (counter) circuit and the Ripple Off counter.

The possible methods of prevention are similar to those discussed in Section 2.0 above, (Page 3), with the following qualifications:

- a) **Modified power-reset.** As in Section 2a, Page 4. Preferred method.
- b) **Capacitive bias.** As in Section 2b, Page 4.
- c) **Lengthening the interruption to the +5 volt supply would be effective, but in this case the switch would have to be in the +5 volt (Z) line.** It would be in effect a much more complicated version of the existing +5 volt (Z) delay module.
- d) **Capacitive hold-up of the +5volt supply is in this case a non-critical, acceptable solution, provided that the capacitance is large enough.** The capacitor could be at the PCU/PDU interface, or at the +5 volt (Z) output, the latter requiring the lower total value. To cover the case of a low-voltage auto-switch, the +5 volt (Z) line capacitance should be at least 3000 μ F.

5.0 DR AC 5072. EXPERIMENT #2 CHANGED FROM "STANDBY" TO "OFF" AT PC CHANGEVER (HK-12)

This occurred only once, and could not be made to recur during several subsequent PC changes. It was established that the redundant side of the PDU had remained in the "Standby" state and that both sides of the PDU tracked correctly from then on. It was not possible to determine exactly when the change had occurred (it could have preceded the PC switch), nor, with any certainty, what the cause might be. Noting that the circuit affected was fairly sensitive and that it drove a rapidly responding Teledyne relay, it was suggested that a short spurious command or power glitch was just able to affect one relay without being sufficient to drive any of the other three. If the reason was a spurious command, then it implied that the +5 Volt (Z) switch was not cutting off rapidly enough as the supply fell, in which case a possible solution was to reduce the +5 Volt (Z) fall time, once the switch had cut off, by removing the extra capacitors in the new module, leaving only the original 0.34 microfarad of the existing PDU Circuit. (Currently the total capacitance



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across the +5 volt (Z) output line is 1.02 microfarads.) However, oscilloscope photographs of the Uplink +5 volt switched supply and the +5 volt (Z) supply did not support this idea, but these photographs were taken some time after the anomaly had become apparent.

Following further spurious changes of Experiment #2 status during subsequent test operations, the true cause was found to be a current leakage in the command line. The investigation is described in Section 6.0 below.

6.0 DR AC5082. EXPERIMENT #2 CHANGED SPONTANEOUSLY FROM "ON" TO "STANDBY", AND FROM "STANDBY" TO "OFF".

When the Qual model Central Station was in Uplink A and PC #2, the Experiment #2 power status several times changed spontaneously from "ON" to "STANDBY", and from "STANDBY" to "OFF". The periods before the changes occurred varied from several minutes down to apparently zero. As the temperature fell from about 125°F to room temperature, the "ON" to "STANDBY" spontaneous change ceased, and the "STANDBY" to "OFF" change occurred less frequently. The relays appeared to respond correctly to all commands, even if the spurious drive then set them immediately to another condition. When PC #1 and/or Uplink B was selected there was apparently no anomalous behavior, and it was found that whichever PC/Uplink combination was selected, the Experiment #2 relays in PDU #1 always tracked the commands correctly, inrespective of the behavior of the relays in PDU #2.

In order to localize the fault more precisely, the voltages on the harness command lines to the relay drivers were measured. The typical value on an experiment command line was 4.7 volts, but with Uplink A operating the "Experiment #2 OFF" line showed only 4.2 volts. (See Figure 5) When the current in this command line was measured, it was found to be about 10 microamps into the logical '1' output of the TTL 54L gate, compared with only some tens of nanoamps on the other command lines. When Uplink B was selected, the "Experiment #2 OFF" command line showed no anomaly.

The final tests at system level were to note the command line behavior with both Uplinks powered and with both Uplinks unpowered. Summarizing all results:

	A ON	A OFF
B ON	No anomaly	No anomaly
B OFF	Anomaly	Anomaly

It was clear that the anomaly occurred only if Uplink B was "OFF";



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the state of Uplink A had no effect. The problem therefore appeared to lie inside the "Experiment #2 OFF" command gate, in the 'B' side of the Command Decoder.

Tests at card level consisted of connecting the outputs of the unpowered command gates to +5 volts, through a 50,000 ohm resistor, and measuring the leakage current at various temperatures. Starting at approximately 200 nanoamps at room temperature, the leakage current into the suspect gate increased with temperature, approximately doubling every 10 degrees Centigrade, until at 110°F - 120°F several microamps were flowing. The remaining "good" gates showed leakage currents which followed the same doubling law, but which were at least one order smaller.

Having definitely traced the cause of the problem to the command gate, the relevant chip was replaced. Further investigations into the reasons for the unusually high leakage current are still in progress, and will be reported separately. It is relevant to note at this point that reverse leakage into the logical '1' output of a powered or unpowered TTL 54L gate is not a parameter which the manufacturer formally tests or specifies, nor, it appears, has any knowledge of. In the early stages of the PDU design it was realized that such leakage could be a potential problem, and initial proposals incorporated base-emitter resistors, as in the current PDM dump drivers, in order to desensitize the system. However, low measured leakage currents, and reliability parts-count trades off, led to their removal.

When the relay scrambling problem occurred (See Reference #6), the immediate line of attack was "gate leakage", but despite all attempts to induce leakage this approach had to be abandoned. The current problem is the first practical evidence of the "fault", which was searched for, and not found, in at least three earlier series of tests.

Since we do not yet know the mechanism which causes the leakage, it is not possible to say whether screening all gates and rejecting those giving more than, say, 1 μ A at any temperature would be sufficient to eliminate any future recurrence of the problem. The leakage may be subject to an aging process, or it may be mechanical deformation susceptible to the expansions and contractions of successive temperature cycles, or it may be simply an unchanging manufacturing problem, etc. - there is not sufficient evidence so far to draw any statistically significant conclusions. The only hopeful evidence available at the moment is that in testing about 150 gates for reverse leakage it was found



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that the "good" and the "unacceptable" groups are fairly distinct, i. e., the "unacceptables" are not simply the arbitrarily separated tail-end of an overall normal distribution. This suggests that there is a definite physical difference and that it is probably not an ageing effect. If all the gates are in reality from one continuous population it is difficult to explain why there are roughly 3% - 5% "unacceptables" when their position at about ten sigma from the mean gives their probability of occurrence as considerably less than $1\text{-in-}10^{12}$.

Assuming that permanent elimination of high leakage currents by selection cannot be guaranteed, the ideal solution would be to modify the designs of the PDU relay drivers so as to make them compatible with the specified logic '1' and logic '0' voltage levels of the TTL 54L gates, when the problem of leakage effects would automatically disappear. This is clearly impracticable because of the program impact. A less elegant, but a simple and effective expedient is to add a 5 Kilohm pull-up resistor from the +5 volt (Z) line to each susceptible command line.

Two aspects of the anomaly which remain to be explained are why only the PDU #2 relays were affected, and why the spurious change to "OFF" occasionally delayed for a considerable time at the "STANDBY" stage. The relay driver performance charts in BxA Memo 9713-530 (Reference #8) show that there is a common reason.

The normal ranges of parameter variations for the driver transistors are quite wide, and the required switching input current from the TTL 54L gate may vary by a ratio of at least 6 to 1. At a leakage current of 10 microamps the probability of switching is very roughly 20%. Hence, with two randomly selected relay drivers connected in parallel to the same command line it is not surprising that one of the two never responded to the spurious input. At half the leakage current probably neither would switch; at five times the leakage current both would switch. It was simply chance that gave a leakage current in the "may switch/will not switch" transition region. Extending this argument to individual relays, rather than relay drivers, explains why the transitions to "OFF" occasionally lingered in "STANDBY". The "ON" to "STANDBY" or "OFF" change is a function of the Potter-Brumfield relay, while the selection of "STANDBY" or "OFF", once the system is not "ON", is determined by the separate Teledyne relay. If one assumes that the P. B. relay is at the more sensitive end of the specified characteristics, and that the Teledyne relay is at the less sensitive end, and also that the temperature and/or leakage current is slowly changing, it is easy to see that in marginal switching conditions the relays will almost certainly not change simultaneously. Variations of this theme, assuming differing temperature gradients and variations of relay resistance with temperature, can explain all the observed behavior.



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7.0 GENERAL DISCUSSION.

7.1 If the impacts upon the program were not completely unacceptable, it would be possible to eliminate with 100% certainty every anomaly discussed above, and all other spurious commands and Central Station status changes, by the following three design modifications:

- a) Supply each command output gate with a V_{CC} which is always at least 200 millivolts lower than the V_{CC} to any other gate in the Command Decoder. In particular, this difference must be maintained over the 1.5 volt to 2.5 volt V_{CC} range, whatever the direction and rate of change of voltage. This modification would eliminate all spurious commands due to the critical V_{CC} level mechanism.
- b) Change all power reset circuits so that they generate a 100 millisecond pulse whenever the +5 volt supply line returns from below 2.75-3.00 volts, with no minimum requirement for the duration of the power supply "glitch". This would ensure that all flip-flops would be set to acceptable, predetermined conditions in the event of a major power disturbance which took the V_{CC} below the critical level.
- c) Reduce the V_{CC} of the input stages of all relay drivers to about 3 volts, with appropriate driver circuit resistor value changes. This would make the drivers compatible with the manufacturer's specified performance of the TTL 54L gate, irrespective of any tendency to generate reverse leakage currents.

7.2 In addition to the above it would also be desirable, if program impact permitted, to modify the PCU regulator loop gain to give a rapid rise to full output voltage at turn-on, eliminating the existing 10 to 15 millisecond plateau at the critical 2.0 to 2.5 volt level. (See Figure 5 of Reference #6) This plateau was originally attributed to the action of the APM circuit, but a recent analysis has shown that it is primarily due to a Miller integrator action in the third stage of the regulator feedback amplifier. The APM, input power, and output load contribute only in determining the level at which the saturation plateau occurs; under normal turn-on conditions the plateau occurs at or near the critical V_{CC} level. Since all the outputs, including the +29 volt lines, follow the same waveform, a more rapid rise would be beneficial in preventing experiment status changes during PC changeover due to power reset-circuits. It is



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known that such changes have occurred in HFE and that they could theoretically occur in at least the LSG experiment. Within the Central Station, the previously suggested power reset modifications would prevent random status changes at a PC changeover, but it would be preferable if the supply voltages never had an opportunity to drop to the critical level.

The above remarks, of course, apply mainly to a commanded PC changeover, or an automatic over-voltage changeover. In the case of an automatic under-voltage changeover, due to a heavy and sustained overload or a regulator failure, it is impossible to guarantee that the voltages will not drop to the power-reset level during the 300 millisecond delay period. In any case, a severe overload would probably cause all experiments to be ripped to "STANDBY" before the PC change could occur.

7.3 The changes discussed above constitute the only 100% satisfactory solutions, and they are the only changes which would attack the root causes of the anomalies. All the other "fixes" which have been discussed, and which will be discussed below, are attacks upon the symptoms only, and complete success cannot be guaranteed.

7.4 The earlier sections discussed specific anomalies and specific solutions. The following paragraphs outline other system modifications, which may be acceptable from a program impact-point of view and which mask as many symptoms as possible.

In discussing spurious commands, flip-flop status changes and relay scrambling, it must be remembered that only relay scrambling could place the system in an irrecoverable, failed situation. The +5 volt (Z) switch, discussed in Reference #6 appears to solve satisfactorily the turn-on relay-scrambling problem, making less than perfect solutions for the other problems acceptable.

Possible approaches are as follows:

- a) Hold up the +5 volt supply from the PCU to the PDU with capacitors during a PC changeover, such that the +5 volt (Z) switch does not operate, nor do any gate V_{CC} fall to the critical level. Figure #4 shows the proposed circuit. Because of the limited availability of capacitors it would be necessary to restrict the hold-up circuit to the PC #1 to PDU #1 +5 volt line. The very large capacitance value leads to a noticeable weight penalty, of about 0.7 lbs per capacitor module.

This circuit eliminates only those Central Station problems which occur during a normal 35 millisecond PC changeover



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transient. It does not in any way affect a turn-on problem, such as APM status, nor the effects of Command 110. There will also be no protection if the power supply is lost for appreciably longer than 35 milliseconds. The +5 volt (Z) switch must be retained for protection from relay scrambling at initial turn-on.

- b) Place voltage-sensitive relay switches in the +5 volt supply line to each half of the Command Decoder, and a 3,000 μ F hold-up circuit on the +5 volt (Z) line. The switches would detect when the +5 volt lines dropped below about +3 volts and would then cut off the supply to the Decoder very rapidly, using a transistor "crowbar" to discharge any capacitors. Following a switch-off, there would be a delay of at least 100 milliseconds after the input voltage had risen above +3 volts before the series relay would reconnect the supply to the Command Decoder, for a rapid rise through the critical level. The 100 mS delay would ensure that the Decoder power-reset circuits would be triggered. The full requirements, design rationale and circuit details for the switch are given in Memo 9713-560 (Reference #7). The switches would not prevent spurious commands from occurring,

but they would ensure that the rise and fall of the V_{CC} through the critical region would be so rapid that any spurious commands would be extremely short, probably much less than a microsecond, and the probability of effecting any status changes would be very small. The hold-up circuit on the +5 volt (Z) line would ensure that during a normal PC changeover the voltage level would not drop low enough to take any of the associated flip-flops into the critical region. These fixes in combination should give a high probability of preventing any of the observed or theoretically possible critical level anomalies from occurring.

- c) Insert two series gates in each command line, (or at least in each critical command line), the first gate being supplied from the +5 volt switched supply to the Command Decoder, the second through a constant 200 millivolt drop from the same supply. These would prevent any spurious commands at turn-on or at PC changeover, but would have no effect upon spurious flip-flop changes of status due to low V_{CC} .



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8.0 SUMMARY AND RECOMMENDATIONS

The basic causes of all the observed and theoretically possible anomalies (except experiment power resets at PC changeover) are the relatively high critical level of the TTL 54L gates, and the occasional unusually high value of the unspecified reverse leakage current. The insensitivity of the power-reset circuits to short "glitches" and the slow rise of the PCU outputs contribute to the final anomalous behavior, or allow it to occur. A 100% guaranteed "fix" program is theoretically possible, but it cannot be implemented because of the general impact. Various partial fixes of the symptoms have been discussed, and of these the best practical compromise would be:

- a) Voltage-sensitive switch in each +5 volt lead to the Command Decoder, plus a 3,000 μ F capacitor hold-up on the +5 volt (Z) line.
- b) Screening of all relay command gates to eliminate high reverse leakage, plus the possible addition of 5 Kohm pull-up resistors on all critical command lines, this latter only being necessary if the nature of the leakage mechanism and its assumed long-term stability cannot be demonstrated.

At present, the only corrective measures which have been implemented are reverse leakage screening, plus a 5,400 μ F hold-up circuit on the PCU #1 to PDU #1 +5 volt line (See Paragraph 7.4 a)).



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Addendum to Section 6.0

Late Information - The latest information on the gate reverse leakage problem is that examination of the "faulty" gate has shown that its high leakage is caused by a manufacturing anomaly, and that there is no reason to believe that the low leakage of acceptable gates will drift up to unacceptable levels within the intended life of Array E. This information is in agreement with the tentative conclusions which were drawn in Section 6.0 from the simple analysis of the grouping of the "faulty" and "acceptable" leakage current results.



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REFERENCES

1. DR AC5068 - Change from DP Formatting to LSPE Formatting following Octal Command 110.
2. DR AC5069 - APM came up in "OFF" state at turn-on (HK-76).
3. DR AC5071 - Uplink switch delay status changed to "Delayed" at PC changeover (HK-01).
4. DR AC5072 - Experiment #2 changed from "Standby" to "Off" at PC Changeover (HK-12).
5. DR AC5082 - Experiment #2 changed from "On" to "Standby", and "Standby" to "Off" spontaneously.
6. ATM-1087 - "Investigation into the Scrambling of Array E Qualification Model PDU Relays at Turn-On".
7. BxA Internal Memo 9713-560, "The Elimination of Spurious Commands From Array E Under All Power Transient Conditions".
8. BxA Internal Memo 9713-530, "PDU Analysis".

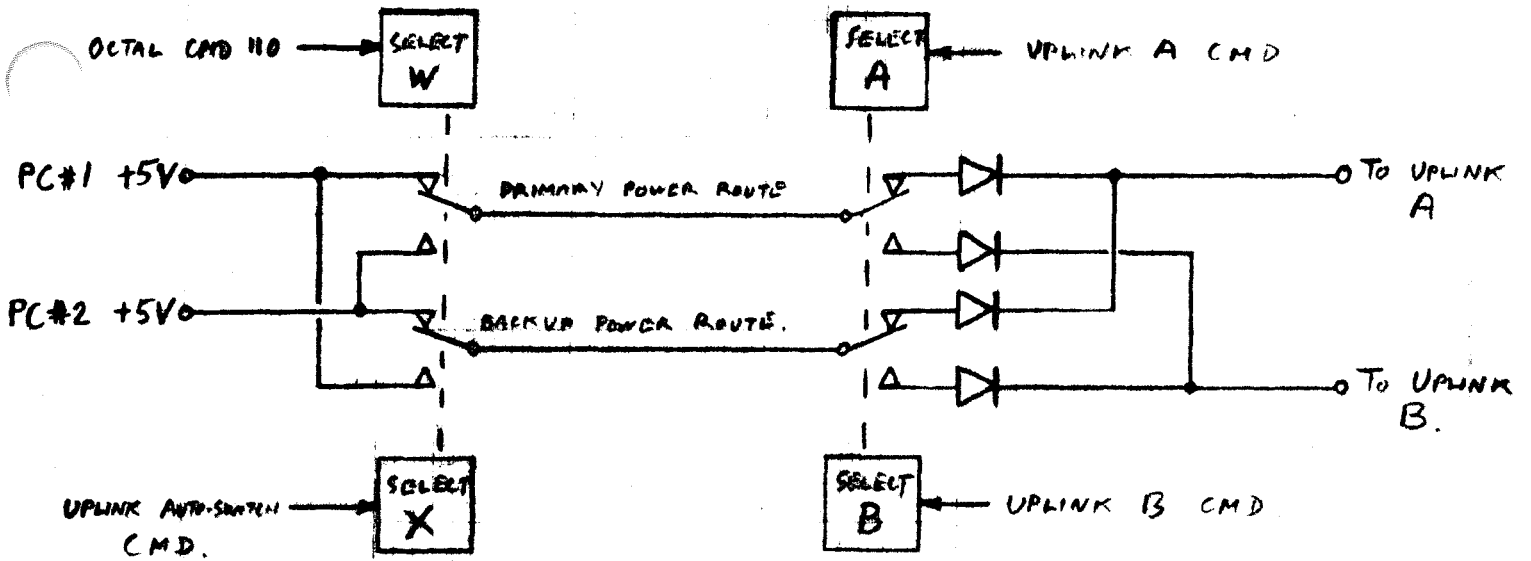
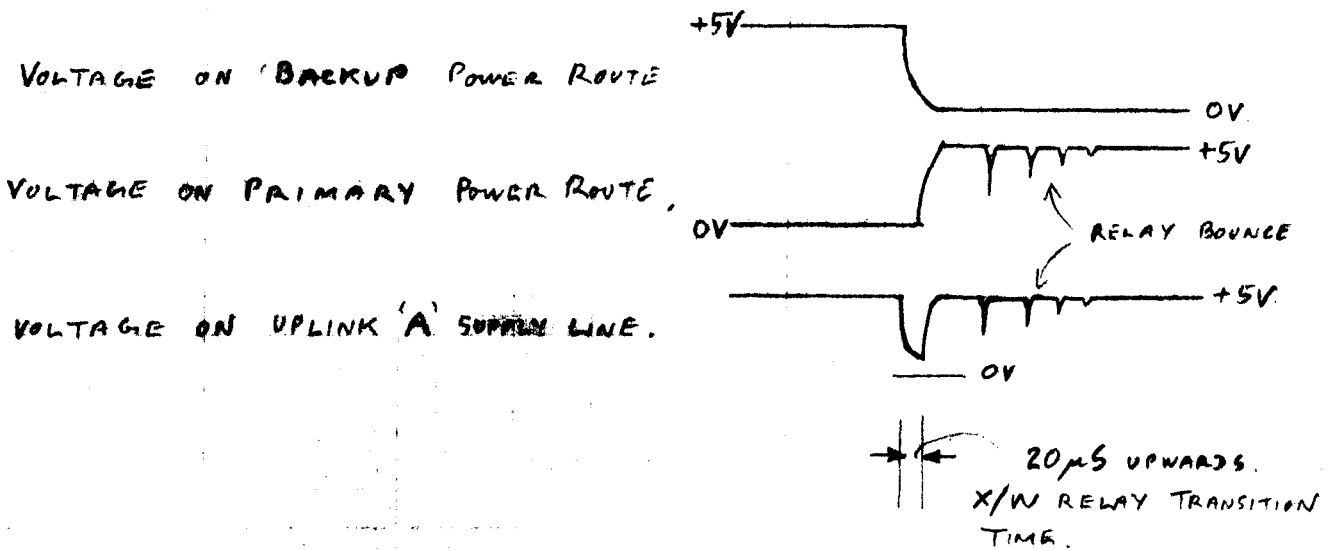


FIGURE 1 :- UPLINK +5 VOLT SWITCHING.



- NOTE
1. PC IN USE DOES NOT CHANGE.
 2. UPLINK IN USE DOES NOT CHANGE.

FIGURE 2 :- TYPICAL EFFECT OF CMD 110.

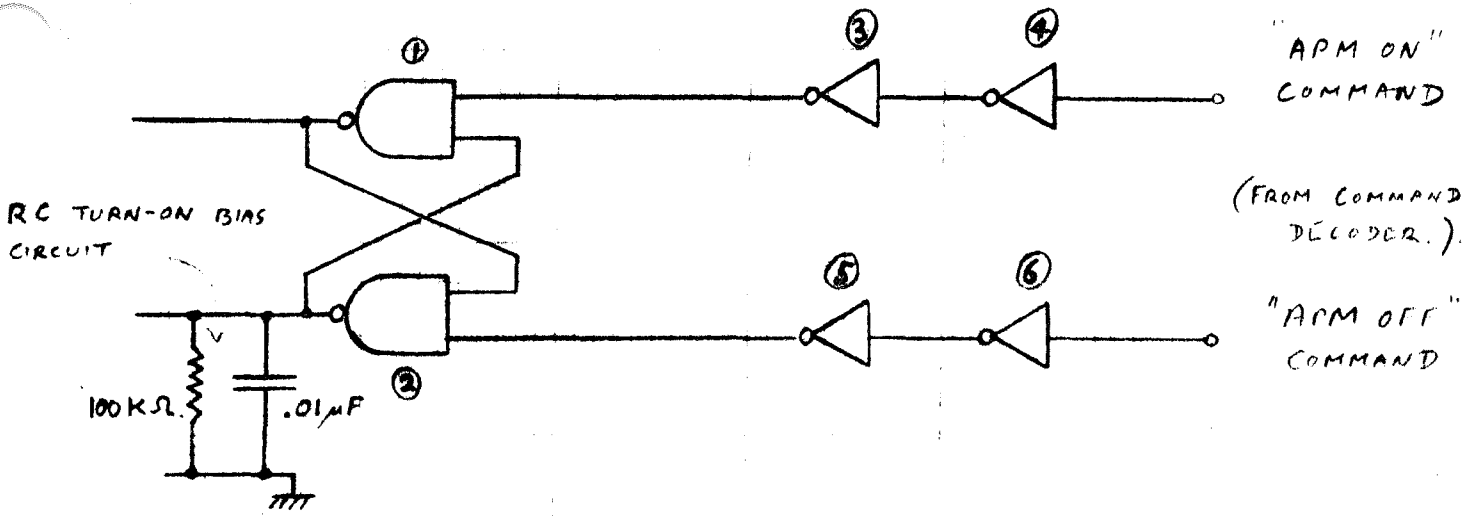
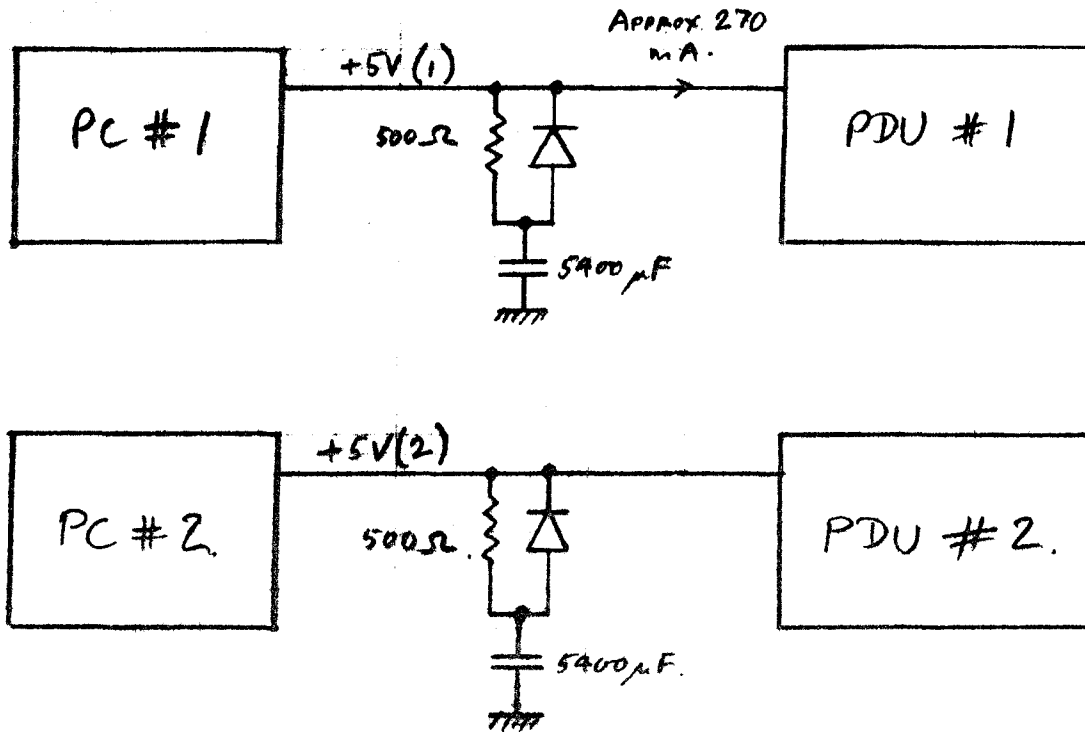


FIGURE 3:- DETAIL OF APM CONTROL FLIP-FLIP.



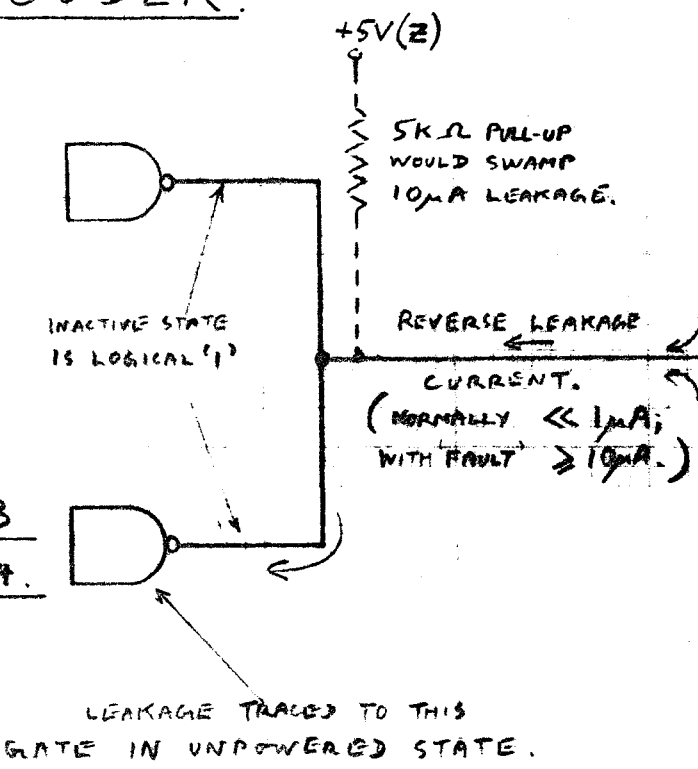
HOLD-UP CIRCUIT CHARGES SLOWLY, WITH NEGLIGIBLE EFFECT UPON NORMAL OPERATION. CAPACITOR DISCHARGES RAPIDLY THROUGH DIODE, LIMITING MAXIMUM DROP IN 35 MILLISECONDS TO 2.25 VOLTS, INCLUDING FIXED DIODE DROP.

FIGURE 4:- CAPACITIVE HOLD-UP CIRCUIT.

COMMAND DECODER.

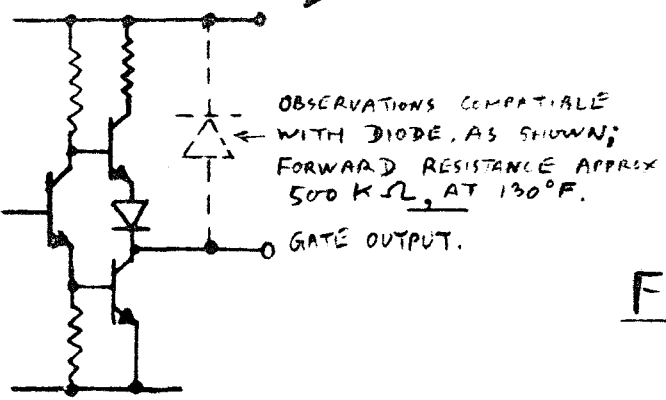
UPLINK A
CMD 044

UPLINK B
CMD 044.



LEAKAGE TRACED TO THIS GATE IN UNPOWERED STATE.

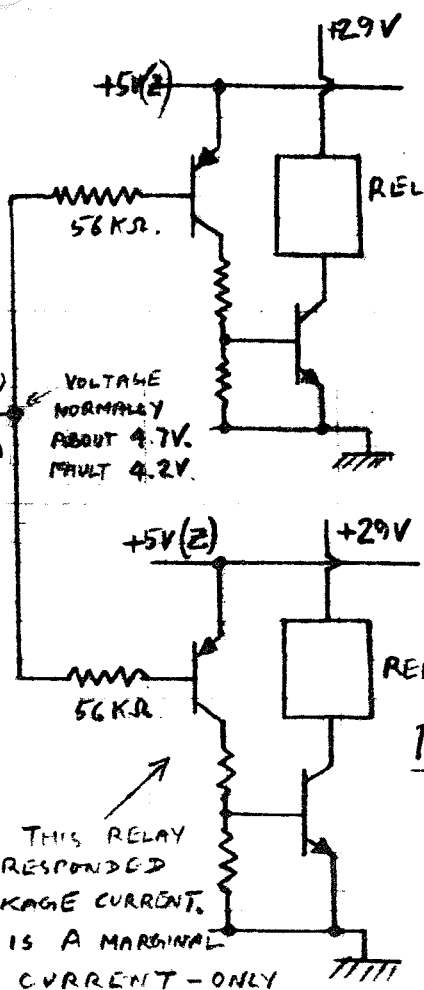
POSSIBLE MODEL FOR FAULT MECHANISM



PDU.

PDU #1; EXP #2.

PDU #2; EXP #2.



RELAYS: "OFF" SOLENOIDS

RELAYS SHOULD TRACK ALL COMMANDS IN PARALLEL.

RELAYS: "OFF" SOLENOIDS.

FIGURE 5: SUMMARY DIAGRAM OF REVERSE LEAKAGE PROBLEM.