ATM 643

MARCH ENGINEERING MODEL TEST PROGRESS REPORT

31 March 1967

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1.0 PROGRESS SUMMARY

This is the fifth monthly progress report on the ALSEP Engineering Model Systems Tests which covers the efforts during the time period 1 March through 31 March.

The EM Systems Tests are proceeding substantially in accordance with the schedule established in ATM 604 although the Heat Flow Experiment has not been available for integration with the Central Station during this reporting period.

To permit meaningful Category #3 tests to be performed with the CPLEE on line the Central Station wire harness and data processor were reworked into the Array A3 configuration in which CPLEE replaces SIDE. After these tests had been completed the system was again reworked, this time into the Array B configuration.

Due to the time required to incorporate the changes to obtain the A3 and B experiment arrays, and also due to factors associated with the testing of the ALSEP Prototype Model, the time available for on-line EM Systems Tests has been restricted, and so relatively less has been achieved compared with previous months testing.

Category #2 tests are complete on the CPLEE, and Category #3 tests are complete on the A3 experiment array which consisted of the PSE, SWE and CPLEE, the LSM was not available to complete this array. The limited Category #1 tests which were required after conversion of the Central Station to the Array B configuration are complete. Integration of the ASE, Category #2 and #3 tests are under way. The STS computer programs for SWE and CPLEE are complete and checked out, and minor revisions are being incorporated in the SIDE program.

The modifications of the Central Station to the Array A3 and the Array B configurations were incorporated smoothly. No operating problems and faults have been encountered in the data subsystem, which throughout this reporting period was operated with hardwire links.

The operation of the PSE and SWE has continued to be good. A problem was encountered during the integration tests of the CPLEE, when the experiment was operated in the ETS vacuum chamber the experiment data stream was initially meaningless, and improved shielding of the digital timing and data lines was necessary to obtain valid data. During the Array A3 Category #3 tests, errors were apparent on the CPLEE status bits although all other information indicated that the experiment was functioning correctly. No correlation could be established between the status bit errors and the operation of the other experiments.

A modification was required to the Data Output Monitoring Equipment to enable it to read the ASE data via the Central Station downlink, and insufficient testing has been performed to permit a definite evaluation of the experiment.

2.0 MONTH'S ACCOMPLISHMENTS

The significant accomplishments of this months EM tests are:

1. Completion of Category #2 tests on CPLEE EM.

2. Completion of Category #3 tests on Array "A3" experiments consisting of PSE Central Station Electronics, SWE and CPLEE.

3. Rework of the Central Station wire harness and data processor into the Array B configuration, and satisfactory checkout and Category #1 tests after rework.

4. Integration of the ASE, and incorporation of a modification to DOME to enable it to read the downlink data stream correctly.

5. Confirmation of the STS software programs for testing the SWE and CPLEE.

6. Checking of the SIDE STS program, which only requires minor correction.

3.0 TEST RESULTS

3.1 ENGINEERING MODEL TEST CONFIGURATION

The EM test configuration has been the subject of two major changes during this reporting period. In order to permit the continuation of STS software checkout during the period when the initial integration of the CPLEE was taking place, the Array A experiments configuration of the Central Station was supplemented in February by additional cables and connectors to permit the CPLEE to be substituted for the LSM. This temporary arrangement was changed on 3/12/67 to the Array A3 experiments configuration, i.e., PSE, LSM, SWS and CPLEE.

Category #3 tests were then performed on this experiment array less the LSM which was not available for testing at BxA.

On completion of the Array A3 Category #3 tests the Central Station wire harness and data processor were reworked prior to the start of the Array B experiments EM tests of the PSE, SIDE, CPLEE, HFE and ASE. Table 3.1-1 shows the status of all equipment on line during the month.

TABLE 3.1-1

STATUS OF ENGINEERING MODEL HARDWARE ON LINE

Month Ending: 31 March 1967

Prime Equipments

Subsystem/Component	Breadboard	Modified Brassboard	Engineering Model	Remarks & Status
Data Subsystem				
Data Processor		X		
Multiplexer - A/D Converter		X	X	
Diplexer			X	
Diplexer Switch			X	
Transmitter "A"	Returned after repair 3/17/67			
Transmitter "B"	Returned after repair 3/27/67			
Receiver				Hardwire link
Command Decoder		X		
PDU			X	
Wire Harness			X	
Terminal Strip			X	
Power Subsystem				
RTG Simulator (BxA)			X	
RTG Generator (GE)				
PCU			X	
PDM			X	
Structural/Thermal				
Base Plate			X	
Dust Detector			X	Part time
Experiments				
Passive Seismic			X	
Solar Wind			X	
Magnetometer				Returned to Philco 3/1
SIDE/CCIG		X		Returned to RICE 3/22
CPLEE			X	Returned to BRLD 3/17
ASE			X	
Heat Flow				Subsystem test at BxA

STATUS OF ENGINEERING MODEL HARDWARE ON LINE

Month Ending: 31 March 1967

GSE

Subsystem/Component	On Line	Operation		Remarks
		Satisfactory	Unsatisfactory	
Signal Breakout Boxes				
Passive Seismic #1	X	X		
#2	X			
Solar Wind	X	X		
Magnetometer	X	X		
SIDE/CCIG	X	X		
CPLEE	X	X		
ASE	X	X		
Heat Flow	Used in experiment subsystem tests			
Data SS Test Set				
DDS 1000	X	X		
Uplink	X	X		Returned to GSE
Downlink	X	X		group for modifi-
Experiment Simulators	X	X		cation prior to
RF Test Set	X	X		qual model tests
Experiment Test Sets				
Passive Seismic	X	X		
Solar Wind	X	X		
Magnetometer				
SIDE/CCIG	X	X		
CPLEE	X	X		
ASE	X	X		
Heat Flow	Used in experiment subsystem tests			
System Test Set				
Data Unit	X	X		
Programmer Processor	X	X		

To prepare for the imminent increase in ALSEP test activity associated with the build of the ALSEP Prototype and Qualification Models, the experiment test sets were transferred to a site in the BxA South Lab on 3/6/67, and the ALSEP EM was transferred and reassembled at the new site.

In addition, as a consequence of the over run of Engineering Model Tests into the ALSEP Prototype Model testing phase conflicts in the utilization of test equipment have arisen; the STS #1 being required for the Prototype Model tests and towards the end of March the DSSTS was returned to the GSE group for modifications which are required in order to test the ALSEP Qualification Model data subsystem. To minimize the impact of these conflicts on EM testing two measures have been taken: 1) Suitable interconnecting cables and an intercom have been installed to allow remote operation of the STS #1 when this is not being used for ALSEP Prototype Model tests; 2) a command decoder test set which provides an uplink capability is used together with a specially constructed downlink demodulator. This demodulator may be used to drive the second DPS 2000 telemetry data processor or other readout equipment. This second arrangement has the advantage that the STS software checkout of the Array B experiments can progress independently of ALSEP Prototype Model tests, but it is restricted to hardwire up and downlinks.

3.2 CENTRAL STATION STATUS

The changes required in the Central Station wire harness and data processor to obtain the Array A3 and the Array B experiment configurations referred to in Section 3.1 were implemented without difficulty, and the Central Station checked out and functioned correctly with these changes incorporated.

In fact, no operating problems or faults have been encountered in the data subsystem, either in the uplink or the downlink portions during this reporting period. However, due initially to the absence of the downlink transmitters which were at Philco for rectification, and later in the month to the lack of RF GSE test equipment, operation of the RF links has not been possible this month.

The PCU is still subject to the two intermittent failures reported last month in ATM 626, i.e., occasional failure to respond to a PCU #2 to PCU #1 changeover transition, and loss of regulation of PCU #1. These faults are considered to be of secondary importance in the present phase of EM tests, as the great majority of the current tests can be performed perfectly satisfactorily using PCU #2.

Limited Category #1 tests were performed on the Array B configuration, primarily to check that power line quality and power protection circuits were correct. The changes to the data subsystem are minor, and apart from checking that the command verification is correctly received via the downlink, it was only necessary to shown that timing signals were being distributed to the HFE and CPLEE connectors correctly.

3.3 CATEGORY #2 TESTS

3.3.1 Passive Seismic, Solar Wind, and Suprathermal Ion Detector Experiments

Category #2 tests of these experiments were completed in January and the results were published in ATM 618. Certain rechecks were made during February which were reported in ATM 626. During March, only Category #3 tests have been performed on these experiments.

3.3.2 Charged Particle Lunar Environments Experiment

Subsystem tests with the CPLEE operating in vacuum were completed in February and Category #2 tests in vacuum commenced at the beginning of March. At this time the EM System was substantially in the Array A experiments configuration but with the CPLEE connected in place of the LSM, utilizing the LSM commands and data slots, although the CPLEE analog signal outputs were correctly connected to the Central Station multiplexer. This arrangement permitted Category #2 tests of CPLEE to be performed and also allowed the Array A experiments STS software to be checked and debugged.

The Category #2 tests of the CPLEE which were made at the end of January in the arrangement described except that the experiment was operating in air had proceeeded very smoothly, but when the tests in vacuum were started the experiment data stream was meaningless. In consequence a careful investigation was made to determine whether the change in the behavior of the experiment, which had passed its subsystem tests satisfactorily, was due to some spurious condition of the test set up with the Central Station. All the interface signals were proved to be in accordance with the ICS, and the only apparent change from the earlier test in air was the use of a non-standard cable between the Central Station and the CPLEE ETS vacuum chamber. This cable is required as the standard flat cable cannot be used with the vacuum chamber connectors. Measurements made at the chamber connector showed that high frequency noise induced from the experiment power convertor was present between the shields of the digital timing and data lines and the signal return, of about 200 mV peak-to-peak amplitude.

After further investigation it was established that valid experiment data could be obtained either by connecting a .025 μF capacitor between the data line shield and the signal return at the vacuum chamber end of the cable, and/or by making more direct connections between the cable shields and the Central Station ground. Category #2 tests were performed with these revised timing and data line shielding arrangements.

Table 3.3.2-1 is a table of functional discrepancies noted during the Category #2 and #3 tests. A brief summary of the Category #2 test results is given below:

TABLE 3.3.2-1

CPLEE DISCREPANCIES NOTED IN EM TESTS

	Discrepancy	ICS Paragraph	ICS Value	Acceptable Value to Bendix	Remarks
1.	Intermittent Digital Data Operation with EM Central Station	NA	NA	NA	Investigation indicates that the experiment logic may have a low noise margin. Category #2 tests completed with revised grounding and filtering of timing lines to reduce noise input to the experiment. Improved shielding incorporated in the prototype.
2.	Power Line Noise	3.2.3.4	100 mV p-p	Dependent on Cat. #3 tests	1 V p-p noise in the 29 V line. Additional shielding incorporated in prototype model.
3.	Power Converter Noise on Analog Lines	3.2.2.2	10 mV p-p	———	Affects data accuracy, refer to 2. Acceptable value depends on accuracy required.
4.	Power Converter Noise on Timing and Command Lines	Not specified.		100 mV p-p	About 150 mV p-p on timing, about 250 mV p-p on command lines. Can carry the logic "low" level marginally above the +0.4 V limit. See Item 1 regarding sensitivity of experiment to this noise.
5.	Errors on Status Bits Transmitted by Experiment	3.2.2.3.4	———	Errors are not acceptable	Observed during Category #3 tests. All other data indicates that experiment is functioning correctly. Errors could not be correlated with operation of the other experiments.

Power

The experiment power profile and the turn-on transient were within the limits quoted in the interface specification. Observed values of input current are:

CPLEE Status		Current
1.	Normal	98 mA
2.	Ripple during analyzer voltage sequence	10 mA p-p
3.	Turn on	
	1st peak	240 mA
	2nd peak	280 mA
4.	Heater on increment	90 mA
5.	Initial heater on transient	80 mA

The turn-on-current transient, which has a characteristic double peak arising from the operation of the current limiter, is shown in Figure ure 3.3.2-1.

The recorded turn-off transient peak voltages were +65V and -25V. These values are considered to be high but acceptable to the data subsystem. The turn-off voltage transient is shown in Figure 3.3.2-2.

The experiment power convertor noise substantial. Variations in the noise voltage recorded at the signal breakout box close to the Central Station at different steps in the analyzer sequence and on alternate convertor half cycles. The maximum level observed was about 1.0V. In Figure 3.3.2-3 typical waveforms for the observed voltage noise and for the transient on the input current to the experiment are illustrated.

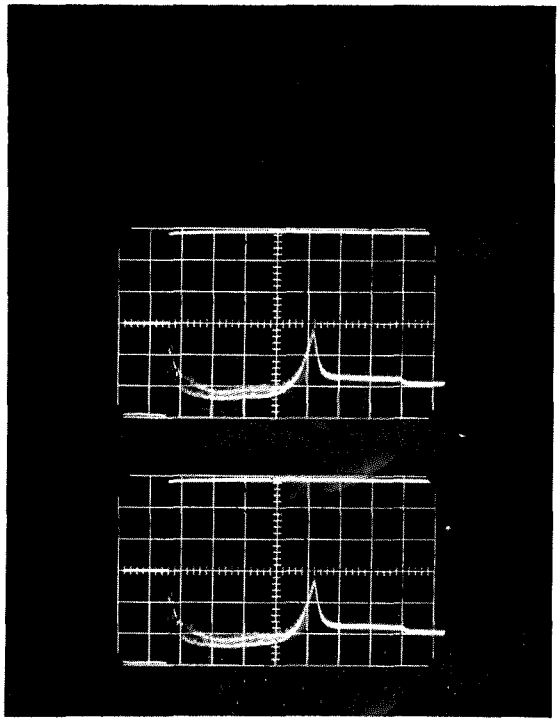
Commands

Command response was normal, the experiment responded correctly to all commands and no spurious interactions were detected.

Examination of the waveform on the experiment to Central Station interface lines showed that substantial loading of the Central Station by the experiment occurred, raising the logical "low" level during the command to a value which depended on the command line being examined, and which was between +150 mV and +300 mV. Also about 250 mV peak-to-peak noise induced from the CPLEE power convertor was present, so that on certain lines the level could rise marginally above the ICS value of +400 mV maximum.

Both records:
Top trace: 29 V to experiment 10 V/cm
Bottom trace: 29 V line input current to experiment 100 mA/cm

Both records: 10 mS/cm

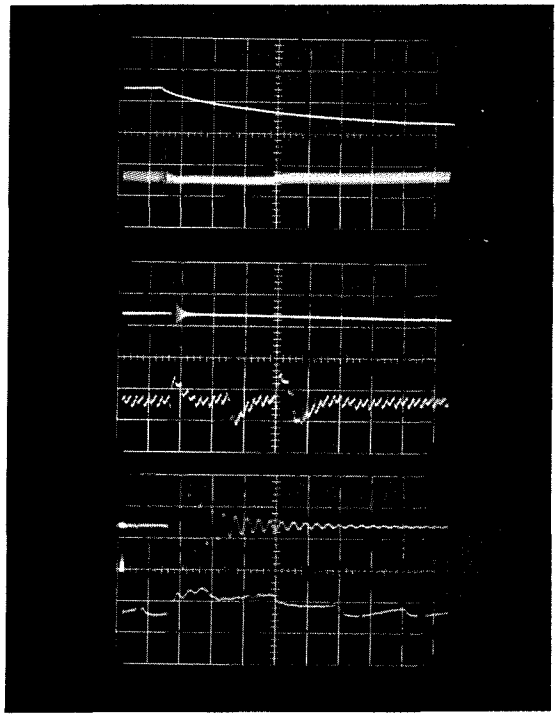


(a) PCU #2

(b) PCU #1

Figure 3.3.2-1 CPLEE Turn-On Transients

All records:
Top trace: 29 V line to experiment 20 V/cm
Bottom trace: 29 V supply from PCU 200 mV/cm



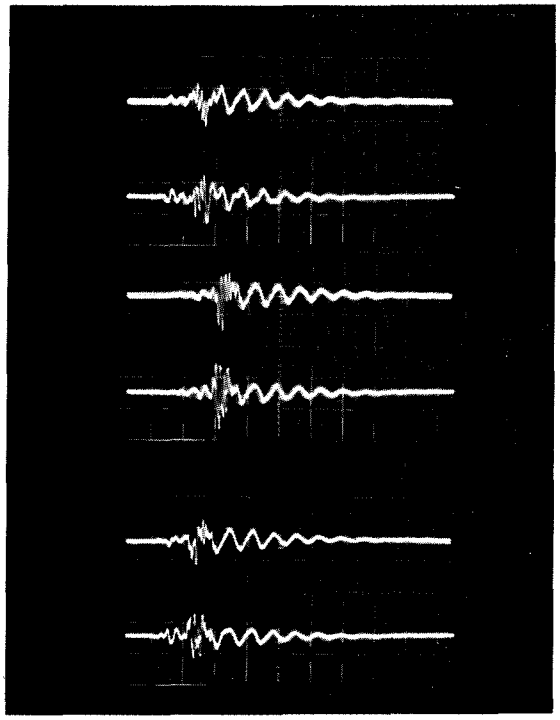
(a) 5 mS/cm

(b) 200 μs/cm

(c) 20 μs/cm

Figure 3.3.2-2 CPLEE Turn-Off Voltage Transients

All records:
Top trace: 29 V to experiment 0.5 V/cm
Bottom trace: 29 V line input current 100 mA/cm
All records: 2 μs/cm multiple sweep exposures



Note that variations occur:

1. Between each convertor half cycle.

2. At different steps in the analyzer sequence.

Figure 3.3.2-3 CPLEE 29V Line, Typical Power Convertor Noise

Oscillograph records were obtained and are available at BxA, but the noise frequency is sufficiently high to be at the limit of the speed of the camera and film which was available and the records are not suitable for reproduction.

Timing and Data Signal Waveforms

All the timing and data signal waveforms were normal and were in accordance with the ICS specification values. Typical data words are shown with the corresponding demand pulses in Figure 3.3.2-4.

Detail oscillograph records were taken of all the waveforms, and these are available at BxA. It was observed that the loading of the experiment raises the low level of the timing lines, of the even frame mark to +0.15V and of the shift and data demand lines to +0.3V, and that about 150 mV peak-to-peak of power convertor induced noise was superimposed on these levels. However, as explained above for the command lines the records are not suitable for reproduction.

Downlink Performance

With the revised shield grounding and filtering as described above, the downlink performance appeared to be good, but a detailed verification of the downlink performance was deferred until the Category #3 tests.

3.3.3 Lunar Surface Module Experiment

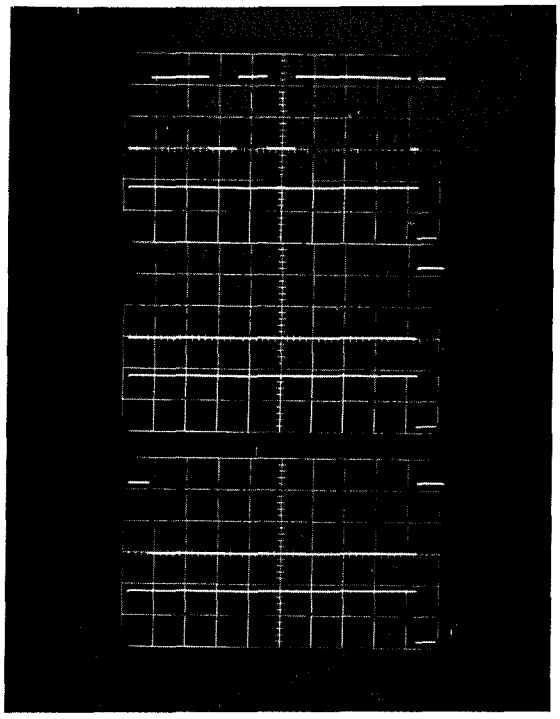
The test results of the LSM EM Category #2 are documented in the February report, ATM 626. The LSM EM was returned to Philco 3/1/67 so that no further testing has occurred since the publication of ATM 626.

3.3.4 Active Seismic Experiment

Initial operation of the ASE with the Central Station revealed unexpected problems associated with the power control logic design, as reported in ATM 626. A redesign was developed by the experiments group and after subsystem tests the experiment was put back on line for Category #2 tests 3/30/67.

Insufficient testing has been performed to permit a definite evaluation of the experiment's status at the time of writing. The presence of a one bit delay in the Central Station data processor which was not appreciated at the time of thedesign of the Data Output Monitoring Equipment (DOME) has

All records:
Top trace: 10 MSB's of CPLEE word #2, 2 V/cm
Bottom trace: Data demand 2 V/cm
All at: 1 mS/cm



(a) Calibration count

(b) All "zeros"

(c) Leading "one" followed by all "zeros"

Figure 3.3.2-4 CPLEE Data and Data Demand Signals

necessitated a modification to enable DOME to read the downlink bit stream. Development of the modification has delayed the testing of the experiment. The modification has been incorporated and the DOME is reading the downlink bit stream correctly.

Test results so far obtained are discussed below:

Power

The experiment is operating correctly with the Central Station power supplies. It should be noted that this experiment does not contain an internal power convertor. However, detailed records of power line quality have not been made. The total power consumption of the ASE EM in normal operation modes, engineering data and scientific, is 3.2W.

Command Response

The experiment responds correctly to all commands except the "Fire Grenade #1" command.

Shift and Data Signal Waveforms

The shift and data signal waveforms at the ASE/Central Station interface are correct, and are illustrated in Figure 3.3.4-1. The characteristic 10 μs delay between the trailing edge of the shift and the change in data line level should be noted. As the ASE electronics is normally mounted in the Central Station, the falling edges of the waveforms are acceptable and normal although the fall time is about 2 μs.

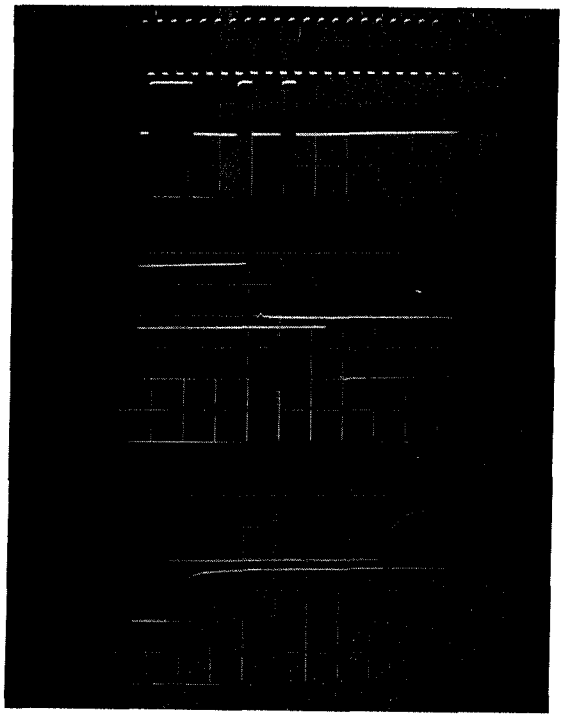
Real Time Events

On occasions, the real-time event detector circuitry in the EM has produced spurious outputs, and the operation of this portion of the experiment will be subject to further investigation.

3.3.5 Heat Flow Experiment

The HFE EM was received at BxA on 3/27/67 and its subsystem tests were satisfactorily completed on 3/31/67. Before the experiment could be integrated with the Central Station it was accidently damaged. It has been shipped back to the manufacturers for an assessment of damage. It is now anticipated that the HFE will be available for integration 4/10/67.

All records:
Top trace: Shift 2 V/cm
Bottom trace: Data 2 V/cm



(a) Full word
200 μs/cm

(b) Falling edges
5 μs/cm

(c) Rising edges
5 μs/cm

Figure 3.3.4-1 ASE Data and Shift Signals

A brief summary of the subsystem test results is given below:

Power

The operating power profile was within the peak ICS value, but exceeded the average value specified. The normal operational input current from the 29V supply is 150 mA, with an increment of 55 mA for 10 sec during the power programming transient, which occurs once every 90 ALSEP frames.

The HFE EM turn-on transient exceed the ICS limit, peaking to 610 mA, the peak level exceeding 400 mA for approximately 6 mS. An external current limiter will be used during the integration testing to enable the experiment to be turned on with the standard experiment circuit breaker setting. The transient is shown in Figure 3.3.5-1.

Command Response

The HFE EM responded correctly to all its commands.

Data

The Heat Flow subsystem accuracy cannot be determined at BxA, especially with regards to the differential temperature sensing. However, the data outputs looked reasonable in all modes for all the sensors of the single probe which was operated with the electronics.

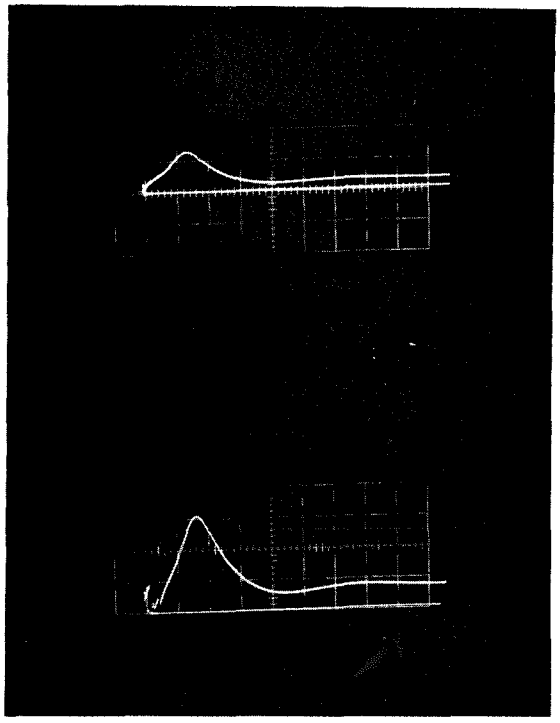
One discrepancy was observed in the subsystem test configuration, the waveforms of the digital timing signals were poor, although this had no detectable effect on the performance of the experiment. The electronics was connected to the ETS via a long non-standard cable which is believed to cause the waveform distortion, this will be confirmed when the HFE is integrated with the Central Station using the standard flat cable.

Compatibility

The HFE EM satisfied all the ALSEP compatibility requirements except that the power turn on transient exceeds the allowable limit, as described above. The power convertor noise level will be examined during integration tests.

3.3.6 Dust Detector

Checks have been made of the Dust Detector EM analog outputs in ALSEP word 33 on two occasions during March. The outputs appeared to be normal.



(a) 500 mA/cm
5 mS/cm

(b) 200 mA/cm
5 mS/cm

Figure 3.3.5-1 HFE Turn-On Current Transient

3.4 CATEGORY #3 TESTS

3.4.1 Array A Tests

Category #3 testing of the Array A experiment configuration was completed during February and is fully reported in that month's Progress Report, ATM 626. No further Category #3 tests of Array A were attempted during March.

3.4.2 Array A3 Tests

Category #3 testing was limited to three days operation of the Array A3 configuration of experiments, the PSE, SWE and CPLEE were operated together, the LSM was not available to complete the array. In this configuration CPLEE replaces the SIDE, and the SIDE data slots are used, i.e., words 15, 31, 47, 56 and 63 in the ALSEP format, together with word 24 which was previously a SP PSE word.

Most of the testing was directed towards checking the CPLEE, as the other experiments had previously been checked during the Array A Category #3 tests as reported in ATM 626. A new problem was encountered, the count data on both the science and calibration steps appeared to be correct, examination of the analog lines indicated that the analyzer voltage was sequencing correctly but a substantial number of errors on the experiment sequence status bits were detected. These errors only occurred on the positive analyzer voltage steps of the sequence, no errors were recorded on the negative voltage steps.

Large fluctuations of the error rate were observed during the three day test period. It was established that the interface signals to the CPLEE were in accordance with the ICS values, and also that the error rate at a given time was unaffected by the operation of either or both the PSE and the SWE. Consequently, it was decided to perform the planned Category #3 tests, and to treat the observed errors as a simple experiment malfunction not associated with the rest of the system. During the course of the tests, no correlation between error rate and experiment operating time or temperature could be discerned.

3.4.3 Power Subsystem

No power subsystem problems were anticipated with the Array A3 experiment array following the satisfactory operation of the power subsystem with the Array A configuration. During the A3 Category #3 tests, a 5W resistive load was used to simulate the LSM, and the experiments in general provided a simpler power system load than the Array A, for example the only significant operating transient was the normal SWE sequence, and all the experiment turn-on transients were limited.

All aspects of the power system performance were good during the Category #3 Array A3 tests, no turn on problems were encountered, and no interactions of the power protection circuits or the power relief sequencer were detected. The experiment induced noise voltage on the +29V supply was dominated by the PSE noise as would be anticipated, and the CPLEE contribution was also evident. However, the limited time available for the tests did not permit similar detailed recording of the power line noise to the records taken during the Array A Category #3 tests.

3.4.4 Data Subsystem

No noise peaks which would take the levels of the timing signals outside the limits given in the various ICS's were detected when the interface was examined.

3.4.5 Experiments

The system command response was checked with all the experiments operating in a similar test to that performed on the Array A experiment configuration. Command sequences for both central station control and for the individual experiments were employed. During this tests, the experiments which were not being directly addressed were set in their reset mode, and the operating mode status of the experiments was verified by the ETS's.

No major interactions which would permanently affect the experiment operating mode were detected, although on two occasions the CPLEE apparently jumped forward in its analizer voltage sequence. This behavior could not be made to recur on repeating the commands. However, as the CPLEE status bits reflect the current state of the experiment, the effect of any jump is restricted to the possible loss of one or two frames of CPLEE data which would appear to be of minor significance.

3.4.6 PCU Changeovers

PCU changeovers were performed with all the experiments operating, and no significant problems were encountered. As anticipated from the results of earlier Category #1 and the Array A Category #3 tests, the CPLEE which was the #4 experiment in the array was rippled off by the power relief sequencer during the PCU changeover.

3.4.7 Astronaut Control Switch #3 (Experiments On)

The "Experiments On" Astronaut Control Switch was successfully operated and all the experiments came on in their normal turn on operating modes.

3.4.8 Back-Up Time Command Sequence

This mode of experiment command control could not be tested for the Array A3 experiment configuration as the Array A command sequencer was still incorporated in the Central Station and could only have generated the Array A commands, none of which would have been executed with the Array A3 EM system.

3.5 CATEGORY #4 TESTS

Category #4 testing has been limited during this reporting period to a number of runs made with various experiments and the STS on line, with the object of checking and confirming the STS software programs for the experiments. The results of this effort is reported below. It should be noted that there has not been the opportunity to perform extended runs, of the type reported in ATM 626 for the LSM, in which the STS is used to analyze large volumes of experiment data.

The SWE STS program was debugged and operated with the experiment during the first two weeks of March, at which time the program decommutated and formated for print out the experiment data correctly. At this time errors were present in the numerical analysis portion of the program, and it was apparent that the arithmetical errors could be more easily corrected with the fixed and controllable data stream input to the STS which is generated by the PDP-8 ALSEP simulator then by further checking with the experiment. The program errors have now been detected and corrected.

The SIDE STS program was also checked and debugged, until on the 3/22/67 all the operations associated with data decommutation, limit checking and data analysis, parity checking and output formating were operating correctly. The only errors present were in the command tracking portion of the program, and arose from a misunderstanding by the programmer of the experiment response to certain commands. The corrections required are straight forward and are being incorporated off line.

The CPLEE STS program was run for the first time 3/15/67 and proved to be completely correct, the data decommutation, experiment status tracking, data output formating, data print out and command tracking operations all worked without error.

The STS still will not display the PSE outputs correctly. A failure was found and repaired in the photo process recorder used to display the experiment outputs, and a program error has been corrected. However, two of

the eight experiment signals are not displayed at all, and the performance of the other channels is erratic. Faults in the D/A convertor, or its associated cabling are suspected, but the ALSEP Prototype Model test schedule results in little time being available for tracing this type of STS fault.

No attempt has been made to run either the HFE or ASE programs yet.

4.0 STATUS AND SCHEDULE

At the end of the report period the EM tests are proceeding substantially in accordance with the schedule contained in the December Monthly Report, ATM 604. Array B testing started as scheduled in mid March, the HFE was received for subsystem test 3/27/67, and it is anticipated that integration of the HFE and Central Station will occur 4/10/67.

Technical problems, mainly associated with the test equipment, led to a few days delay in the ASE Category #2 testing.

SIDE EM tests are now scheduled 4/6/67.

Unless unanticipated problems arise, Category #3 test of the Array B should be in progress by mid April.

APPENDIX A

ENGINEERING MODEL SYSTEMS INTEGRATION TESTS BRIEF LOG

Date	Comment
3/1	PSE strip chart recorder checked out. SIDE STS software ran successfully. CPLEE integrated with Central Station.
3/2	SIDE ran with STS software. A couple of simple modifications required to SIDE software. Attempted run of SWE software.
3/3	Investigation of unsatisfactory CPLEE data stream. SWE software ran, formatted data correctly, minor errors found.
3/4	CPLEE investigation continued. System dismantled prior to move to South Lab.
3/6	Equipment transported to South Lab, and installation commenced.
3/7	Installation and cabling continued.
3/8	Installation and checking of equipment, including link to STS. CPLEE back on line.
3/9	CPLEE investigation continued.
3/10	Shielding of cable carrying CPLEE data and timing signals was improved. Good experiment data.
3/11	CPLEE Category #2 tests and documentation of test results completed.
3/12	Central Station harness reworked to Array A3 configuration.
3/13	A3 Central Station checkout. CPLEE Category #2 test data reduced.
3/14	A3 Category #3 tests, PSE, SWE and CPLEE SWE prototype on subsystem tests.
3/15	CPLEE status bit errors observed with experiment in A3 configuration. CPLEE STS program checked, with CPLEE using LSM data slots. Experiment error free, program good.

3/16	A3 Category #3 tests continued.
3/17	A3 Category #3 tests completed. CPLEE returned to BRLD. LSM interface simulator received, no data output.
3/18	Attempt to run SIDE program. Unsatisfactory. Began conversion of Central Station to Array B.
3/20	Continued conversion to Array B.
3/21	Completed conversion to Array B.
3/22	SIDE program check out, good apart from minor errors. SIDE shipped out pm.
3/23	ASE received placed on subsystem test. Attempt to run PSE STS program, unsatisfactory.
3/27	HFE received, subsystem tests commenced.
3/28	ASE subsystem tests with DOME. Uplink command decoder test set used to control Central Station.
3/29	Downlink demodulator constructed to drive DDS-1000 or DPS-2000 directly. ASE subsystem tests completed.
3/30	ASE integrated with Central Station. DOME would not read downlink data due to a timing error.
3/31	DOME timing error corrected. HFE subsystem tests completed.