Bendix
Aerospace Systems Division

NO.	REV. NO.
ATM-912	—

ASE/CE 16 Ch. Multiplexer-A/D Converter Reliability Prediction And Failure Mode, Effects & Criticality Analysis

DATE 8/20/70

This ATM documents the Reliability Prediction and Failure Modes Effects & Criticality Analysis of the Bendix designed ASE/CE 16CH Multiplexer-A/D Converter. The analysis reflects the final flight configuration for the Array D ALSEP System.

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1.0 INTRODUCTION

The results of the Reliability Prediction and the Failure Mode, Effects, & Criticality Analysis for the ALSEP Array D ASE/CE 16 Channel Multiplexer-A/D Converter are documented in this report. This M & A/D represents the Bendix Designed unit which makes extensive use of SSI and MSI integrated circuits and was integrated with the Active Seismic Experiment Central Electronics.

The Reliability Prediction for the 16 Channel Multiplexer is .99995 and the Reliability Prediction for the A/D Converter is .99993. The overall reliability of the M & A/D is calculated to be .99989.

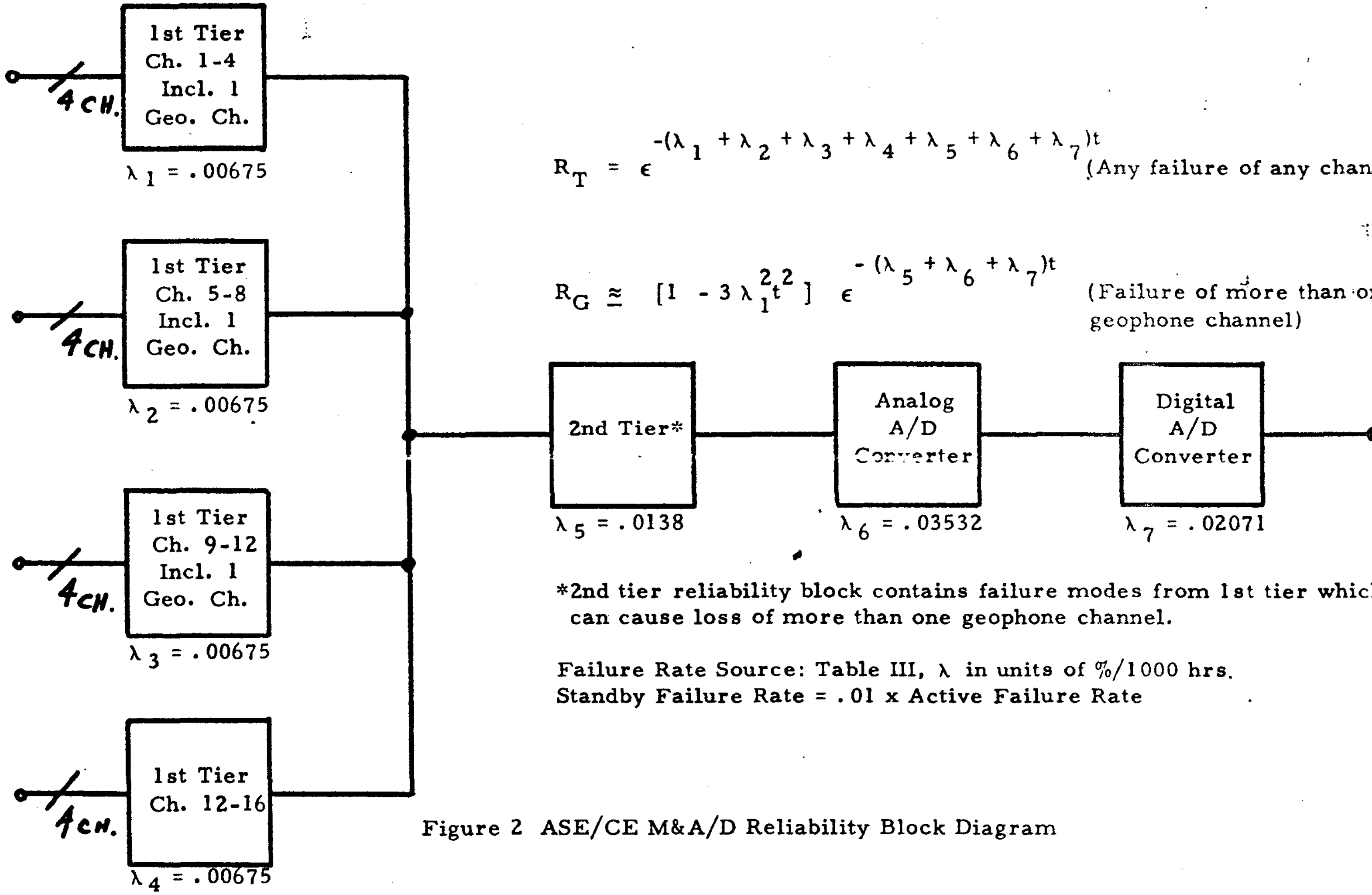
2.0 CIRCUIT DESCRIPTION

Figure 1 presents a Functional Block Diagram of the M & A/D. This diagram is included to clarify the terms and discriptions given in the Failure Mode, Effects, & Criticality Analysis portion of this ATM (Tables II & III). The numbers in each box correspond to the Circuit/ Function Item Number listed in the FMECA. Thus a clear picture may be obtained of the inter-relationships between Circuit Functions and Failure Mode Effects.

The Multiplexing Gates are the same as those used on the Array A2 and Array D 90 Channel Multiplexer, and the A/D Converter is exactly the same design as the Array D Converter except a set of Buffer-Inverters that have been added for output phase compatibility. With the above considerations, full operational capability can be confidentally expected of the Bendix Redesigned ASE/CE M & A/D.

3.0 RELIABILITY PREDICTION

The Reliability Prediction for the 16 Channel Multiplexer is .9999510 and the A/D Converter Prediction is .9999343. The overall reliability for the M & A/D is calculated to be .9998853, which is approximately equal to the design goal of .99990. The above predictions are based on an intended lunar mission of launch, deployment, and 30 hours operation and 8730 hours standby. Figure 2 defines the Reliability Block Diagram and Mathematical Model for the Multiplexer and A/D Converter.



$$R_T = \epsilon^{-(\lambda_1 + \lambda_2 + \lambda_3 + \lambda_4 + \lambda_5 + \lambda_6 + \lambda_7)t}$$ (Any failure of any channel)

$$R_G \approx [1 - 3\lambda_1^2 t^2]\ \epsilon^{-(\lambda_5 + \lambda_6 + \lambda_7)t}$$ (Failure of more than one geophone channel)

*2nd tier reliability block contains failure modes from 1st tier which can cause loss of more than one geophone channel.

Failure Rate Source: Table III, λ in units of %/1000 hrs.
Standby Failure Rate = .01 x Active Failure Rate

Figure 2 ASE/CE M&A/D Reliability Block Diagram

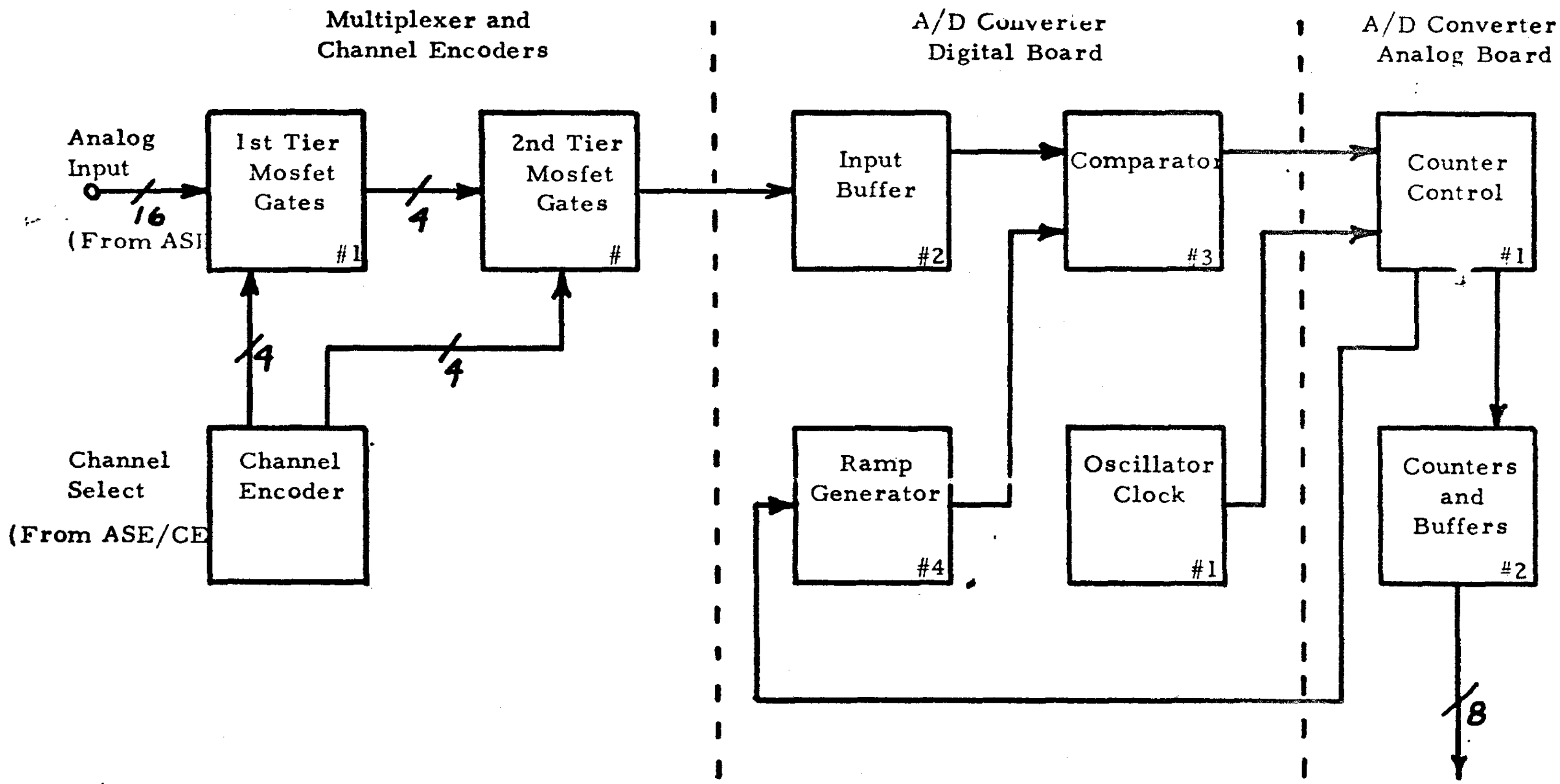


Figure 2, ASE/CE M&A/D Operational Block Diagram

The failure rates for each functional component identified in Figure 2 are tabulated in Table I. The failure rates shown represent composite totals derived from the part application stress ratios of each electronic piece part. The application reflects the anticipated "use" environment.

TABLE I

FAILURE RATE SUMMARY

Assembly	λ_{ai} (%1000 Hrs.) Operating	λ_{si} (%/1000 Hrs.) Standby
16 Ch. Multiplexer	.041800	.000418
A/D Conv., Analog Board	.035321	.000353
A/D Conv., Digital Board	.020710	.000207
Totals	.097831	.000978

Reliability Calculations

$$R_{Mux} = \epsilon^{-\lambda_1 + \lambda_2 + \lambda_3 + \lambda_4 + \lambda_5)t} = \epsilon^{-(.0418)(30 + 87.3) \times 10^{-5}}$$

$$= .9999510$$

$$R_{A/D} = \epsilon^{-(\lambda_6 + \lambda_7)t} = \epsilon^{-(.056031)(30 + 87.3) \times 10^{-5}}$$

$$= .9999343$$

$$R_{Total} = R_{Mux} \cdot R_{A/D} = .9998853 \quad \text{(Probability of no failure)}$$

$$R_{Geo} \equiv [\,1 - 3\lambda^2,t^2] \,\epsilon^{-(\lambda 5 + \lambda 6 + \lambda 7)t} = [\,1 - .944347 \times 10^{-10}]\,\epsilon^{-(.06983)(117.3) \times 10^{-5}}$$

R_{Geo} = .999928 (Probability of no more than one geophone channel failure)

3.0 FAILURE MODES, EFFECTS & CRITICALITY ANALYSIS

The failure mode and effects analysis for the M&A/D are documented in Tables II and III. Table II describes the functional failure modes and the resultant effects on the end item and system level. Table III delineates the failure modes at the piece part level. Each identified failure is numerically itemized for cross reference between Tables II and III, and Figure 2. (Note: the cross reference must be correlated by Assembly).

The failure probabilities reflect the identified line item. The criticality ranking lists by order of magnitude, the highest down to the lowest failure probabilities. Table II lists criticalities by circuit/function, while Table III lists the criticality sub-ranking within each circuit/function item. With this method, the highest order criticalities are easily identified both by circuit/function levels and by discrete part levels.

The format of Tables II and III is designed to provide the reader with a narrative description of the varying types of failures that could occur, combined with the resultant performance characteristics. This information is useful to system support in performing fault isolation should an anomally occur.

The Failure Modes Effects and Criticality Analysis has shown that there are no ALSEP Single Point Failures in the M&A/D. There is one failure mode, however, which constitutes an ASE Single Thread Failure Mode. All 16 channels will be lost if a short occurs in the second tier MOS FET gate package. There is absolutely no way to eliminate this failure mode since all multiplexers, regardless of the number of tiers, will have a finial MOS-FET gate which can fail shorted. This failure mode is identified in Table 4, Section 6, of the Failure Mode Effects and Criticality Analysis. An intensive design effort has been made by Bendix to insure a reliable design, especially in the area of multiplex channel losses. Previous experience with the Dynatronics design has shown that 15 or 16 channels were usually lost when only one component in one channel had failed. Bendix has investigated tiering to minimize these multiple channel losses. The selected design was determined to be the best design.

The selected design was also shown to have the highest reliability with respect to preserving at least two of the three Geophone channels. This is an important criteria for two reasons.

1) The Geophone channels are considered to be the most important from a data standpoint. Some engineering data may be returned if two or the three channels are operating while no useful engineering data is returned if more than one Geophone channel fails.

2) The Geophone channels provide a good cross section of the 16 channels and indicate the reliability of the complete 16 channel system.

5.0 RELIABILITY ASSESSMENT

The purpose of performing a reliability prediction and failure modes analysis is to identify inherent design weaknesses. From the results of these analyses it has been concluded the reliability and design objectives have been fully satisfied.

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	R. J. Dallaire	ATM 912	
END ITEM: ASE/CE	DWG NO. 2346700	PAGE 8 of 16	
ASS'Y: 16 Ch. MUX	DWG NO. 2346711	DATE 8/20/70	

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE: END ITEM	EFFECT OF FAILURE: SYSTEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
1.0 First Tier Channel Encoder	1.0 Failure as Shown Below	1.0 Electrical Failure	1.0 ASE MUX Affected as Shown	1.0 Output Affected as Shown	.00300	3
	1.1 One First Tier MOS FET Gate in Each of the Four MOS-FET Chips is Always "On".	1.1 Output of SN54L20 Fails High	1.1 (3 of 4 Channels of each First Tier MOS FET Chip will be Lost	1.1 Loss of 12 Channels		
	1.2 One First Tier MOS FET Gate in Each of the Four MOS-FET Chips is Always "Off".	1.2 Output of SN54L20 Fails Low	1.2 One Channel From each First Tier MOS Chip Lost	1.2 Loss of 4 Channels		
	1.3 First Tier MOS FET Gate Always "Off".	1.3 Input Fails Open or Short	1.3 One Channel From each First Tier MOS Chip Lost	1.3 Loss of 4 Channels		
2.0 Second Tier Channel Encoder	2.0 Failure as Shown Below	2.0 Electrical Failure	2.0 ASE MUX Affected as Shown	2.0 Output Affected as Shown	.00300	3
	2.1 Second Tier MOS FET Gate Always "On"	2.1 Output of SN54L20 Fails High	2.1 3 of 4 First Tier MOS Chip Lost	2.1 Loss of 12 Channels		
	2.2 Second Tier MOS FET Gate Always "Off"	2.2 Output of SN54L20 Fails Low	2.2 One First Tier MOS Chip Lost	2.2 Loss of 4 Channels		
	2.3 Second Tier MOS FET Gate Always "Off"	2.3 Input Fails Open or Short	2.3 One First Tier MOS Chip Lost	2.3 Loss of 4 Channels		
3.0 First Tier MOS FET Gate Drivers	3.0 Failure as Shown Below	3.0 Electrical Failure	3.0 ASE MUX Affected as Shown	3.0 Output Affected as Shown	.00240	3
	3.1 Driven MOS FET Always "Off"	3.1 Driver Output Fails High	3.1 One Channel From each First Tier Chip Lost	3.1 Loss of 4 Channels		
	3.2 Driven MOS FET Always "On"	3.2 Driver Output Fails Low	3.2 3 of 4 Channels From Each First Tier Chip Lost	3.2 Loss of 12 Channels		

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	R. J. Dallaire	ATM [illegible]	
END ITEM: ASE/CE	DWG NO. 2346700	PAGE 9 of 16	
ASS'Y: 16 Ch. MUX	DWG NO. 2346711	DATE 8/20/70	

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE: END ITEM	EFFECT OF FAILURE: SYSTEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
4.0 Second Tier MOS FET Gate Drivers	4.0 Failure as Shown Below	4.0 Electrical Failure	4.0 MUX Affected as Shown	4.0 Output Affected as Shown	.00240	5
	4.1 Driven MOS FET Always "Off"	4.1 Driver Output Fails High	4.1 One First Tier MOS Chip Lost	4.1 Loss of 4 Channels		
	4.2 Driven MOS FET Always "On"	4.2 Driver Output Fails Low	4.2 3 of 4 First Tier Chips Lost	4.2 Loss of 12 Channels		
5.0 First Tier FET	5.0 Failure as Shown	5.0 Electrical Failure	5.0 MUX Affected as Shown	5.0 Output Affected as Shown	.00600	1
	5.1 Loss of a Gate on Chip	5.1 Short Source-Gate or Any Open	5.1 Loss of 1 Channel	5.1 Loss of 1 Channel		
	5.2 Loss of MX02D Chip	5.2 Short Drain-Substrate, Source-Substrate, Drain-Gate, or Gate-Substrate	5.2 Loss of 4 consecutive Channels	5.2 Loss of 4 Channels		
	5.3 Loss of Other Gates on Chip	5.3 Short Drain-Source	5.3 Loss of 3 Consecutive Channels	5.3 Loss of 3 Channels		
	5.4 Loss of MX02D Chip	5.4 Short Drain-Substrate of Used Gates	5.4 Loss of 4 Consecutive Channels	5.4 Loss of 4 Channels		
6.0 Second Tier FET	6.0 Failure as Shown	6.0 Electrical Failure	6.0 MUX Affected as Shown	6.0 Output Affected as Shown	.00600	1
	6.1 Loss of Gate on Chip	6.1 Short Source - Gate or Any Open	6.1 Loss of every 4th channel	6.1 Loss of 4 Channels		
	6.2 Loss of MX02D Chip	6.2 Short Drain-Substrate, Source-Substrate, Drain Gate, or Gate-Substrate	6.2 Loss of all channels	6.2 Loss of all Channels		
	6.3 Loss of Other Gates on Chip	6.3 Short Drain-Source	6.3 Loss of All Channels	6.3 Loss of 12 Channels		
	6.4 Loss of MX02D Chip	6.4 Short Drain-Substrate of Unused Gates	6.4 Loss of All Channels	6.4 Loss of all Channels		

SYSTEM ALSEP	PREPARED BY R. J. Dallaire	NO. ATM 912	REV.
END ITEM ASE/CE	DWG NO. 2346700	PAGE [illegible] of [illegible]	
ASS'Y A/D Conv.-Analog Brd	DWG NO. 2346719	DATE [illegible]	

TABLE II

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE: END ITEM	EFFECT OF FAILURE: SYSTEM	FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
1.0 Oscillator-Clock	1.0 Oscillator Fails as Shown	1.0 Failure of Discrete Parts or Integrated Circuits	1.0 Clock Affected as Shown	1.0 Output Affected as Shown	.007313	2
	1.1 Oscillator Fails to Provide Output	1.1 Short or Open R1, R2, R3, R4, R5, C1, C2, Y1, or Failure of NG1A, NG1B, NG1C	1.1 Loss of Clock to Counters	1.1 Output will be Frozen		
	1.2 Oscillator Frequency Drift	1.2 Crystal (Y1) Parameter Drift	1.2 Counters Will Count at Wrong Speed	1.1 Output Slightly High or Low		
2.0 Input Buffer	2.0 Buffer Fails as Shown	2.0 Failure of I.C. or Capacitor as Shown	2.0 Analog Input Affected	2.0 Output Affected as Shown	.004507	4
	2.1 Loss of Input to Comparator	2.1 Short C4, Failed Output of LM102	2.1 Analog Input Appears High or Low	2.1 Output all 1's or 0's		
	2.2 Offset Input to Comparator	2.2 Input Offset Drift of LM102	2.2 Offset Input Voltage	2.2 Slight Error in Output		
	2.3 Noise to Input of Comparator	2.3 Open C4	2.3 Chance of Small Errors in Conversion	2.3 Occassional Error in Output		
3.0 Comparator (Compares Ramp Voltage to Analog Input Voltage)	3.0 Comparator Fails as Shown	3.0 Failure of Discrete Parts or I. C.'s	3.0 Ramp Comparison Affected	3.0 Output Affected as Shown	.004833	3
	3.1 Loss of Command Latch Signal	3.1 Open R5, R13, or short R6, C7, or failure of LM111, X5.	3.1 Counters Will Count Erroneously	3.1 Output will be Random or All Zeros		
	3.2 Comparator Will Switch too Soon or too Late	3.2 LM111 Input Offset Drift	3.2 Count Will be Slightly too High or too Low	3.2 Output will be Slightly High or Low		
	3.3 Noise in Comparator	3.3 Open C5 or short R12	3.3 Chance Count Will be Low	3.3 Occasional Slightly Low Output		

TABLE II

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	R. J. Dallaire	ATM 912	
END ITEM ASE/CE	DWG NO. 2346700	PAGE 11 of 16	
ASS'Y A/D Conv.-Analog Brd	DWG NO. 2346719	DATE 8/20/70	

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE: END ITEM	EFFECT OF FAILURE: SYSTEM	FAILURE PROBABILITY Q x 10^{-5}	CRITICALITY
4.0 Ramp Generator	4.0 Ramp Generator Fails as Shown Shown	4.0 Failure of Discrete Devices or I.C.	4.0 Ramp Generator Affected as Shown	4.0 Output Affected as Shown	.017864	1
	4.1 Ramp Generator Will Cease to Function	4.1 Open or Short R8, R9, R10, R11, R14, R15, C3, CR2, Q1 Open R7, or LM107 Failure	4.1 Counter Will Not Turn Off	4.1 Output Will Be Random		
	4.2 Incorrect Ramp Slope	4.2 Drift of CR2, R8, R9, R10, R11, C3, or Input Offset Drift of LM107	4.2 Counter Turned Off too Soon or too Late	4.2 Output Slightly High or Low		
	4.3 Excess Current in Zener CR1	4.3 Short R7	4.3 -12V Supply May Be Shorted	4.3 Possible Loss of A/D Converter (Will Cause PDU to Switch to Redundant A/D Converter)		
5.0 Power Supply Noise Suppression	5.0 On-Board Supplies Affected as Shown	5.0 Failure of Capacitors as Shown	5.0 On-Board Supplies Affected As Shown	5.0 Output Affected as Shown	.000804	5
	5.1 Loss of -12V or +5V Lines	5.1 Short C8 or C9	5.1 Loss of One MUX - A/D Conv.	5.1 Loss of One A/D Converter		
	5.2 Noise on +12V, -12, or 5V Lines	5.2 Open C6, C7, C8, or C9	5.2 Chance Erroneous Count	5.2 Occasional Output Error		
	5.3 Loss of +12V Line Capacitor	5.3 Short C6 or C7	5.3 No Effect Due to Redundant Capacitors	5.3 No Effect		
6.0 Thermistor Network	6.0 Thermistor Affected as Shown	6.0 Resistor Failures as Shown	6.0 Thermistor Readings Affected as Shown	6.0 A/D Converter Operation not Affected	.000335	6
	6.1 Improper Voltage Supplied to Thermistors	6.1 Open or Short R16, R7	6.1 Thermistor Readings Offscale High or Low	6.1 Thermistor Offscale High or Low		
	6.2 Drift in Voltage Supplied to Thermistors	6.2 Drift R16, R17	6.2 Thermistor Readings Slightly High or Low	6.2 Thermistor Slightly High or Low		

SYSTEM ALSEP	PREPARED BY R. J. Dallaire	N° ATM 912	REV.
END ITEM ASE CE	DWG NO. 2346719	PAGE 12 of 16	
ASS'Y A/D Conv. - Digital Brd	DWG NO. 2346722	DATE 8 20 70	

TABLE II

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS

CIRCUIT OR FUNCTION	ASSUMED FAILURE MODE	CAUSE OF FAILURE	EFFECT OF FAILURE		FAILURE PROBABILITY $Q \times 10^{-5}$	CRITICALITY
			END ITEM	SYSTEM		
1.0 Counter Control Circuitry	1.0 Counter Controls Fail as Shown.	1.0 I.C. Failure	1.0 Counter Control Affected as Shown	1.0 Output Affected as Shown	.005900	2
	1.1 Counters Will Not Change States	1.1 Failure of NG1, NG2, H1A, H2A, H2B, H1C, X2	1.1 Loss of Control to Counters	1.1 Output Will be Random		
2.0 Counter Circuitry and Output Buffers	2.0 Counters or Buffers Fail As Shown	2.0 I.C. Failure	2.0 Counters and Buffers Affected as Shown	2.0 Output Affected as Shown	.009600	1
	2.1 Higher Order Stages Will Not Change States	2.1 Failure of X4 or X5	2.1 Higher Order Bits Frozen	2.1 Higher Order Bits Frozen		
	2.2 Counter "Over Count" When Analog Input is Over 5V	2.2 Failure of X6 High	2.2 When Analog Input is Over 5V Counters Will Recycle	2.2 An Analog Input of Greater than 5V will Digitally Read Less Than 5V, Analog Inputs Under 5V Will be Unaffected		
	2.3 Counters Stop Counting	2.3 Failure of X6 Low	2.3 Counters Will Stay at Zero After Reset	2.3 Output Always Read Zeros		
	2.4 One Output Bit Always High or Low	2.4 Failure of Buffer Gate High or Low	2.4 One Bit Erroneous, Other 7 Will Be Okay	2.4 One Bit Erroneous		
3.0 Voltage Supply Noise Suppression	3.0 Noise Suppressor Fails as Shown	3.0 Discrete Parts Failure	3.0 Digital Circuitry Affected as Shown	3.0 Output Affected as Shown	.005210	3
	3.1 Loss of +5V to Board	3.1 Open R1 or Short C1	3.1 Digital Circuitry Will Cease to Function	3.1 Outputs Will Appear to be All Ones		
	3.2 Noise on +5V Line	3.2 Open C1 or Short R1	3.2 Chance Erroneous Count	3.2 Output Occasionally Erroneous		

SYSTEM	PREPARED BY	NO.	REV.
ALSEP	R. J. Dallaire	ATM 912	
END ITEM: ASE/CE	DWG NO. 2346700	PAGE 13 of 16	
ASS'Y: 16 Ch. Multiplexer	DWG NO. 2346711	DATE 8-2[illegible]-70	

TABLE III

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{5}$	CRITICALITY
1.0 First Tier Channel Encoders (SN54L20)	1.1 Output of SN54L20 Fails High	(.400)	1.1 One First Tier MOS FET Gate in Each of the Four MOS-FET Chips is Always "On".	1.1 Loss of 12 Channels, (3 of 4 Channels of each First Tier MOS FET Chip will be Lost)	.0012	1**
	1.2 Output of SN54L20 Fails Low	(.400)	1.2 One First Tier MOS FET Gate in Each of the Four MOS-FED Chips is Always "Off".	1.2 Loss of 4 Channels, (One Channel From Each First Tier MOS Chip)	.0012	1
	1.3 Input Fails Open or Short	(.200)	1.3 First Tier MOS FET Gate Always "Off".	1.3 Loss of 4 Channels (One Channel From Each First Tier MOS Chip)	.0006	2
2.0 Second Tier Channel Encoders (SN54L20)	2.1 Output of SN54L20 Fails High	(.400)	2.1 Second Tier MOS FET Gate Always "On"	2.1 Loss of 12 Channels (3 of 4 First Tier MOS Chips)	.0012	1**
	2.2 Output of SN54L20 Fails Low	(.400)	2.2 Second Tier MOS FET Gate Always "Off"	2.2 Loss of 4 Channels (One First Tier MOS Chip	.0012	1
	2.3 Input Fails Open or Short	(.200)	2.3 Second Tier MOS FET Gate Always "Off"	2.3 Loss of 4 Channels (One First Tier MOS Chip)	.0006	2
3.0 First Tier MOS FET Gate Drivers (DM 7800)	3.1 Output Fails High	(.500)	3.1 Driven MOS FET Always "Off"	3.1 Loss of 4 Channels (One Channel From Each First Tier Chip)	.0012	1
	3.2 Output Fails Low	(.500)	3.2 Driver MOS FET Always "On"	3.2 Loss of 12 Channels (3 of 4 Channels From Each First Tier Chip)	.0012	1**
4.0 Second Tier MOS FET Gate Drivers (DM7800)	4.1 Output Fails High	(.500)	4.1 Driver MOS FET Always "Off"	4.1 Loss of 4 Channels (One First Tier MOS Chip)	.0012	1
	4.2 Output Fails Low	(.500)	4.2 Driver MOS FET Always "On"	4.2 Loss of 12 Channels (3 of 4 First Tier Chips)	.0012	1**

TABLE III

SYSTEM ALSEP	PREPARED BY R. J. Dallaire	NO. ATM 912	REV.
END ITEM ASE/CE	DWG NO. 2346700	PAGE 14 of 16	
ASS'Y 16 Ch. MUX	DWG NO. 2346711	DATE 8 20 70	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10⁻⁵	CRITICALITY
5.0 First Tier MOS FET (MX02D)	5.1 Short Source-Gate or Any Open (.373)	5.1 Loss of a Gate on Chip	5.1 Loss of 1 Channel	.00317	1
	5.2 Short Drain-Substrate, Source - Substrate, Drain-Gate, or Gate-Substrate (.213)	5.2 Loss of MX02D Chip	5.2 Loss of 4 Channels	.00181	2
	5.3 Short Drain-Source (.080)	5.3 Loss of Other Gates on Chip	5.3 Loss of 3 Channels	.00068	3
	5.4 Short Drain-Substrate of Unused Gates (.040)	5.4 Loss of MX02D Chip	5.4 Loss of 4 Channels	.00034	4
6.0 Second Tier MOS FET (MX02D)	6.1 Short Source - Gate or Any Open (.373)	6.1 Loss of Gate on Chip	6.1 Loss of 4 Channels	.00317	1
	6.2 Short Drain-Substrate, Source-Substrate, Drain-Gate, Drain-Gate, or Gate-Substrate (.213)	6.2 Loss of MX02D Chip	6.2 Loss of All Channels	.00181	2*
	6.3 Short Drain-Souce (.080)	6.3 Loss of Other Gates on Chip	6.3 Loss of 12 Channels	.00068	3**
	6.4 Short Drain-Substrate of Unused Gates (.040)	6.4 Loss of MX02D Chip	6.4 Loss of All Channels	.00034	4*
		* Single Asterisk Denotes Loss of All 16 Channels. ** Double Asterisk Denotes Loss 12 Channels Which Implies the Loss of More than One Geophone Channel. Only Criticality Numbers Having Asterisks are Termed "Serious Failure Modes".			

TABLE III

SYSTEM ALSEP	PREPARED BY R. J. Dallaire	NO. ATM 912	REV.
END ITEM ASE/CE	DWG NO. 2346700	PAGE 15 of 16	
ASS'Y A/D Conv. Analog Brd	DWG NO. 2346719	DATE 8 20 70	

FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

PART/COMPONENT SYMBOL	FAILURE MODE (α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY Q x 10^{-3}	CRITICALITY
1.0 Oscillator Clock: R1, R2, R3, R4, R5, C1, C2, Y1, NG1A, NG1B, NG1C	1.1 Short or Open R1, R2, R3, R4, R5, C1, C2, Y1, or Failure of NG1A, NG1B, NG1C (.533)	1.1 Oscilaltor Will Fail to Provide Output	1.1 Loss of Clock to Counters	.004313	1
	1.2 Crystal (Y1) Drift (.371)	1.2 Oscillator Frequency Drift	1.2 Counters Will Count at Wrong Speed	.003000	2
2.0 Input Buffer: LM102, C4	2.1 Short C4, Output LM102 (.776)	2.1 Loss of Input to Comparator	2.1 Analog Input Appears High or Low	.003503	1
	2.2 Input Offset Drift (.193)	2.2 Offset Input to Comparator	2.2 Offset Input Voltage	.000870	2
	2.3 Open C4 (.030)	2.3 Noise to Input of Comparator	2.3 Chance of Small Errors in Conversion	.000134	3
3.0 Comparator: R12, R13, C5, LM111, X5	3.1 Open R12, R13, Short R13, C5; Failure of LM111, X5 (.798)	3.1 Loss of Command Latch Signal	3.1 Counters Will Count Erroneously	.004020	1
	3.2 LM111 Input Offset Drift (.140)	3.2 Comparator Will Switch too Soon or too Late	3.2 Count Will be Slightly too High or too Low	.000810	2
	3.3 Open C5, Short R12 (.002)	3.3 Noise in Comparator	3.3 Chance Count Will be Low	.000003	3
4.0 Ramp Generatpr: R7, R8, R9, R10, R11, R14, R15, C3, C12, Q1, LM107	4.1 Open or Short R8, R9, R10, R11, R14, R15, C3, CR2, Q1, Open R7, or Output Failure of LM107 (.442)	4.1 Ramp Generator Will Cease to Function	4.1 Counter Will Not Turn Off	.009248	1
	4.2 Drift of CR2, R8, R9, R10, R11 (.413)	4.2 Incorrect Ramp Slope	4.2 Counter Turned Off too Soon or too Late	.008631	2
	4.3 Short R7 (.001)	4.3 Excess Current in Zener CR1	4.3 -12V Supply May Be Shorted	.00003	3
5.0 Supply Noise Suppression C6, C7, C8, C9	5.1 Short C8, C9 (.070)	5.1 Loss of -12V or +5V	5.1 Loss of One MUX-A/D Converter	.000060	2
	5.2 Open C6, C7, C8, C9 (.798)	5.2 Noise on +12, -12, & +5V Lines	5.2 Chance of Erroneous Count	.000684	1
	5.3 Short C6, or C7 (.070)	5.3 No Effect Due to Redundant Capacitor	5.3 No Effect	.000060	2
6.0 Thermistor Network: R16, R17	6.1 Open or Short R16, R17 (.817)	6.1 Thermistors Not Supplied Proper Voltages	6.1 Incorrect Thermistor Outputs	.000274	1
	6.2 Drift R16, R17 (.183)	6.2 Thermistors Not Supplied Exact Voltages	6.2 Slight Error in Thermistor Outputs	.000061	2

SYSTEM ALSEP	PREPARED BY R. J. Dallaire	NO. ATM 912	REV.
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FAILURE MODE, EFFECT & CRITICALITY ANALYSIS WORKSHEET

PART/COMPONENT SYMBOL	FAILURE MODE	(α)	EFFECT OF FAILURE: ASSEMBLY	EFFECT OF FAILURE: END ITEM	FAILURE PROBABILITY $Q \times 10^{5}$	CRITICALITY
1.0 Counter Control Circuitry: NG1, NG2, H1A, H2B, H1C, X2	1.1 Any Failure of Digital Circuitry	(1.00)	1.1 Loss of Control to Counters	1.1 Counters Will Not Change State	.005400	1
2.0 Counter Circuitry and Output Buffers: H2, H1E, H1F, X4, X5, X6	2.1 Failure of Any Stage in Counters	(.631)	2.1 Higher Order Stages Will Not Change States	2.1 Higher Order Bits Erroneous	.004800	1
	2.2 Failure of X6 High	(.095)	2.2 Overvoltage Analog Input Will Allow Counters to Overcount	2.2 All Analog Inputs Over 5V Will Digitally Read Less Than 5V All Others Are OK	.000720	3
	2.3 Failure of X6 Low	(.063)	2.3 Counters Will Stop Counting	2.3 Counters Will Stay At Zero After Reset	.000480	4
	2.4 Failure of Output Buffer Gate	(.211)	2.4 One Bit Will Always Be High or Low	2.4 One Bit Will Be Erroneous All Others Will Be OK	.003600	2
3.0 Supply Decoupling R1, C1	3.1 Open R1, Short C1	(.729)	3.1 Loss of +5V to Board	3.1 Outputs Will Appear to be All Ones	.000381	1
	3.2 Open C1, Short R1	(.267)	3.2 Noise on -15V Line	3.2 Chance Erroneous Count	.000140	2