Bendix

Aerospace Systems Division

Analysis of LPTTL, its Capabilities and Deficiencies When Used by Itself or in Interface With LPDTL

ATM 916

PAGE 1 OF 15

DATE 11/6/70

The purpose of this memo is to investigate the interface conditions arising from the use of low power transistor-transistor logic (LPTTL) in conjunction with low power diode-transistor logic (LPDTL) and to familiarize the reader with the fundamental characteristics which make transistor-transistor logic (TTL) of any power level unique, demonstrating the inherent performance characteristic limits of low power transistor-transistor logic if applied in conventional logic design. This analysis utilizes the simple two-input NAND gate as its model. Although generally applicable in nature to all TTL product, it does not suffice as a total analysis for more complex TTL products.

The analysis reveals that LPTTL is generally superior in electrical performance to LPDTL in all areas except power dissipation where LPTTL can experience additional dissipation of 50% or more over that of LPDTL. Complete compatibility at interfaces should exist except in the instance where a LPDTL gate drives LPTTL gates in which case compatible performance can be expected if the output sinking current is limited to 0.75 mA (or a maximum fan-out of LPTTL gate inputs of 4.0 as derated per ALSEP ATM-241 criteria).

As expected in TTL products, the analysis reveals the input breakdown voltage level existing at voltage values slightly greater than 5.0 Volts which should serve as a warning of the sensitivity to damage of the LPTTL inputs to voltages exceeding 5.0 Volts.

The information for this memo has been derived from the following references:

Catalog CC201	Texas Instrument TTL IC Catalog
U ⊓ ϕ 9041 5ΔX Test Plan	Fairchild Semiconductor Final Electrical Test Specification

Prepared By: K. D. Andreasen

K. D. Andreasen, Components Engineer
Parts and Materials Group

Reviewed by: R. C. Roukas

R. C. Roukas, Group Engineer
ALSEP Reliability Department

Approved By: P. P. Sondeen

P. P. Sondeen, Group Supervisor
Parts and Materials Group

S. J. Ellison

S. J. Ellison, Manager
ALSEP Reliability Department

Perhaps the best way to evaluate the low power TTL loading and sourcing characteristics is to consider the unique design characteristics required to create a logic circuit capable of low power dissipation and high speed performance. This discussion will deal with the fundamental requirements of a simple LPTTL gate. The general discussion will be pertainent to all TTL logic. More complex TTL circuits require additional design factors which will not be discussed here.

Consider the basic low power TTL gate shown below. (Figure 1).

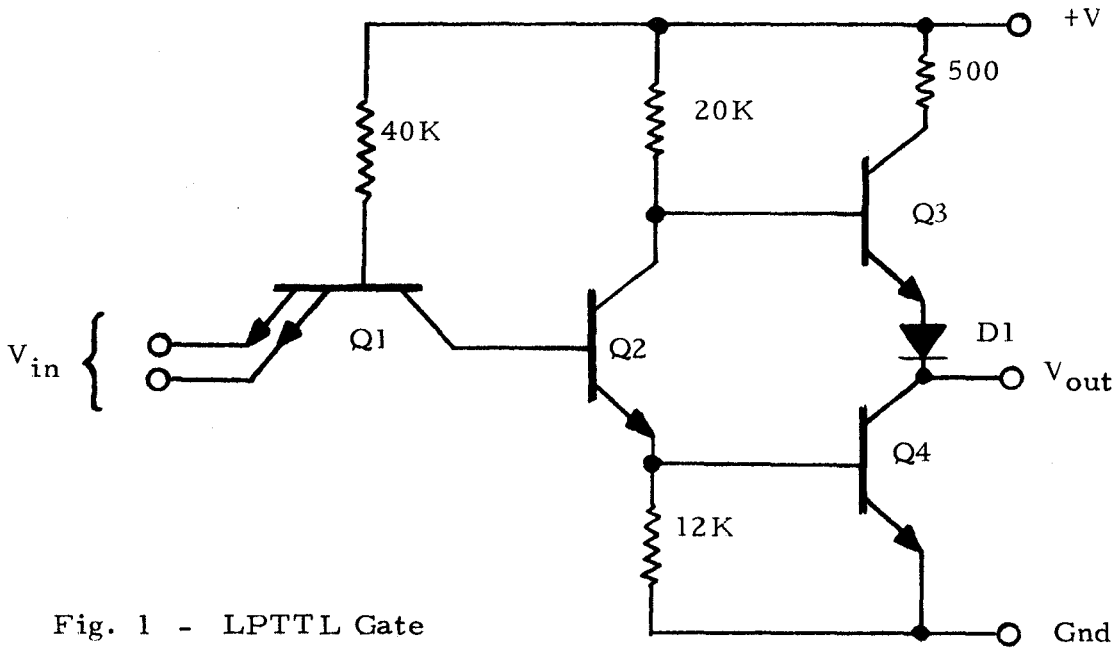

Fig. 1 - LPTTL Gate

With proper bias conditions and input conditions, the circuit will perform as a logic gate.

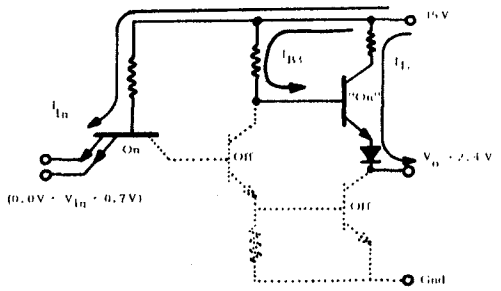

Fig. 2a - High Output State (Logical One)

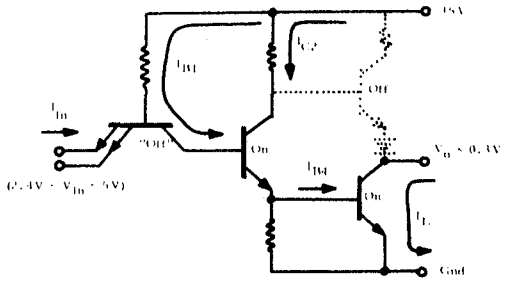

Fig. 2b - Low Output State (Logical Zero)

The TTL manufacturing process is more difficult to control than the DTL process since input transistor performance characteristics are more difficult to obtain than mere input diode junction characteristics. TTL logic has to offer improved circuit performance to justify its added complexity. Improved performance is found in its switching speed. A more detailed analysis of Figures 2a and 2b is required to demonstrate these improvements since the basic low power DTL gate is similar to the low power TTL gate as shown in Figure 3.

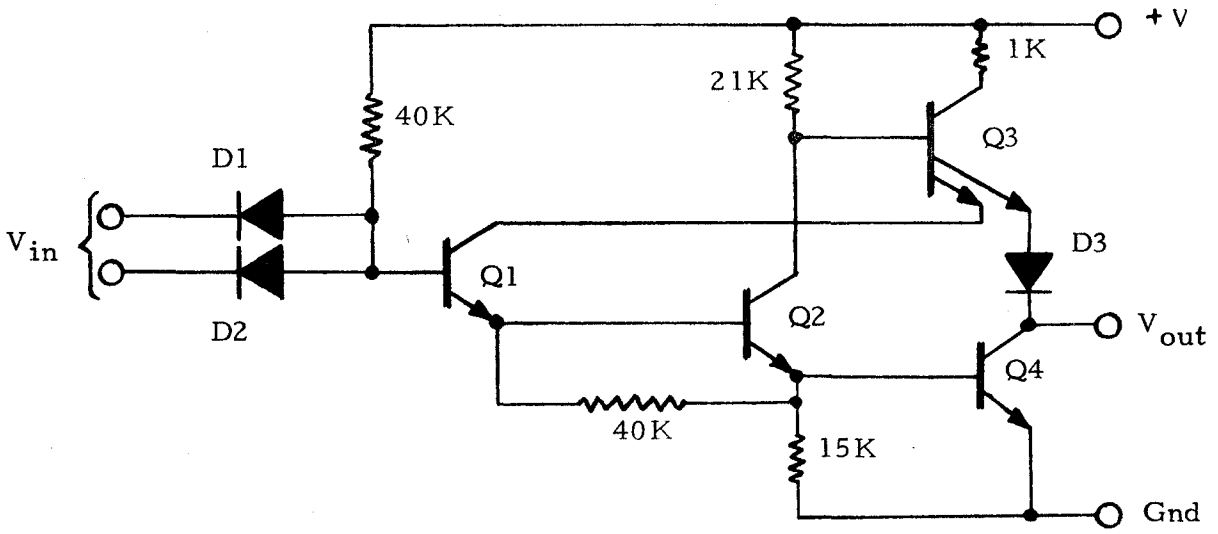

Fig. 3 - LPDTL Gate

Ideally, high speed performance would be best achieved by unsaturated logic design. However, unsaturated logic poses greater performance difficulties than does saturated logic, so this approach to increased speed is not easily attained. With the availability of high speed transistors, the logic design can obtain improved speed by developing a means to remove stored base charge due to saturation when the base of each transistor is turned off. TTL logic performs this task better than DTL logic due to the performance characteristics of the transistors (primarily transistor Q1).

It can be seen from Figures 1 and 2 that the base charge of transistor Q1 is always present since the base current is flowing either base to emitter or base to collector. When transistor Q2 is switched from the ON state (Fig. 2b) to the OFF state (Fig. 2a), transistor Q1 is saturated ON to remove the stored base charge. The stored base charge from transistor Q4 is removed when it is switched from its ON state (Fig. 2b) to its OFF state (Fig. 2a) through the 12KΩ resistor to ground. Transistor Q3 has been designed so that it does not saturate and therefore does not have a critical stored base charge condition. The design features of Q1 and Q2 (resultant of Q1) are uniquely TTL and the features for Q3 and Q4 are similar for both LPTTL and LPDTL.

The design has suffered performance losses to obtain improved switching time characteristics. It is these differences between LPTTL and LPDTL which would tend to effect the compatible performance of the logic forms.

The basic difference of TTL and DTL is fundamental to the creation and control of the multiple emitter input transistor Q1 of the TTL circuit. It is shown in Figure 2b that when Q1 is in the "OFF" state that an input current is experienced. The range of this current is between 1μA and 100μA. This is not a mere leakage current. If Q1 would turn OFF only nano-ampere leakage current would result. Therefore, Q1 is obviously not in the turned OFF state. In fact, the Q1 transistor is actually turned "ON" since the base current I_{B1} of Figure 2b is present. The transistor is in the inverse operation mode where conversion efficiencies are extremely poor and inverse beta (B_{inv}) is less than unity. The Q1 transistor emitter in the inverse mode is acting as a collector and the collector is acting as the emitter. Comparing this input current (I_{in}) with the LPDTL input leakage current (~1nA) it can be seen that LPTTL will dissipate greater power and tend to create a more critical fan-out loading condition. The

TTL design requires greater beta control which effects inverse beta and input breakdown voltage characteristics. If the device beta is high, the input breakdown voltage will be high (which is good), but the inverse beta will be high also (which is poor). If the device beta is low, the input breakdown voltage will be low (which is poor) and the inverse beta will be low (which is good). So, an optimum condition is required which will allow adequate device beta, greater than 5.5 Volt input breakdown voltage and small inverse beta values. Adequate device beta means sufficient beta values to ensure saturation of transistors Q2 and Q4 under full sink current load conditions over the full temperature range. An upper limit exists on the device beta since it is desirable for transistor Q3 to remain in the active mode (designated "ON" in Figure 2a) and not to obtain a saturated ON state.

A worst case analysis of the gate circuit can be made from the parameters on the Texas Instrument data sheet and a few general assumptions. Such an analysis requires knowledge of circuit element characteristics and nominal electrical values. For this purpose, the following assumptions have been made and are believed to be quite representative of the LPTTL circuit elements.

	-55°C	25°C	+125°C
Base-Emitter Diode Threshold	0.8V	0.5V	0.3V
Transistor Saturation Voltage @ 2mA load	0.3V	0.3V	0.3V

Utilizing -0.18 mA maximum from the TI data for the input current shown in Figure 2a and the assumption that the +125°C temperature would be worst case, the high temperature value for the 40KΩ base resistor can be calculated as follows:

$$R_{40} \quad \frac{5.5V - 0.3V}{180 \times 10^{-6}} \sim 30K\Omega$$

so, the change in resistance from the nominal 40KΩ value is 25%. Therefore, the resistance temperature characteristic will be assumed negative and linear as 50KΩ @ -55°C and 30KΩ @ 125°C. With this assumption all resistor values at temperature extremes can be estimated as follows:

Nominal Value	@ -55°C	@ 25°C	@ +125°C
40KΩ	50KΩ	40KΩ	30KΩ
20KΩ	25KΩ	20KΩ	15KΩ
12KΩ	15KΩ	12KΩ	9KΩ
500Ω	625Ω	500Ω	375Ω

Minimum and maximum transistor element beta can now be derived as follows: The TI data sheet specifies a short-circuit output current of -3mA minimum and -15mA maximum. The short-circuit output current is dependent upon the value of the 20KΩ resistor and the beta value of the Q3 transistor. Minimum beta occurs at -55°C as does the maximum resistance value for the 20KΩ resistor, therefore, minimum short-circuit output current would be at -55°C. The following calculation applies.

$$I_{os} = \frac{V_{cc} - (V_f + V_{BE})}{\frac{R_{20}}{\beta_{min.}}}$$

where $V_f = V_{BE}$ 0.8V

and V_{cc} 5.5V

I_{os} -3mA

The equation can be rearranged to solve for minimum beta of Q3 as follows:

$$\beta_{min.} = \frac{R_{20}\,(Ios)}{V_{cc} - (V_f + V_{BE})} = \frac{25 \times 10^{3}\,(3 \times 10^{-3}}{5.5 - (0.8 + 0.8)}$$

$$\beta_{min.} = \frac{75}{3.9} \sim \underline{20 \text{ minimum @ } -55°C}$$

The same equation applies for the maximum beta calculation except the +125°C values must be used.

$$\beta_{max.} = \frac{15 \times 10^{3} \ (15 \times 10^{-3})}{5.5 - (0.3 + 0.3)}$$

$$\beta_{max.} = \frac{225}{4.9} \sim \underline{45 \text{ maximum @ } +125°C}$$

Utilizing the minimum beta value for Q3, it is now possible to determine the minimum sourcing load current available from the circuit output. The TI data sheet indicates that a minimum output voltage of 2.4 volts is necessary to drive the gate input in the logical one state. The minimum source current available and minimum beta occurs at -55°C, so those values must be used as follows:

$$I_{out} = \frac{V_{cc} - (V_f + V_{BE}) - V_{out}}{\frac{R_{20}}{\beta}} = \frac{4.5 - (0.8 + 0.8) - 2.4}{\frac{25 \times 10^{3}}{20}}$$

$$= \frac{20 \ (0.5)}{25 \times 10^{3}} = \frac{10}{25 \times 10^{3}}$$

$$I_{out} \sim \underline{400 \ \mu A \text{ source current @ } 2.4V}$$

The maximum sourcing load current at +2.4 Volts out can be derived utilizing the assumption that Q3 saturates at +125°C.

$$I_{out} = \frac{V_{cc} - (V_f + V_{CE}) - V_{out}}{R_{500}} \quad \frac{5.5 - (0.6) - 2.4}{375} = \frac{3.04}{375} \sim \underline{8mA}$$

It is possible to calculate the minimum forced beta for transistor Q4 if further approximations are employed. The following calculation can be made to determine the maximum I_{B4} current available to the base of transistor Q4. The TI data sheet specifies a maximum zero level consumption current ($I_{cc(o)}$) of 0.51mA. At the same time the data sheet allows 100 μA maximum input current per input. Assuming two inputs at +5.0 volts, the net I_{B4} current would be:

$$I_{B4} = 510 + 100 + 100 = 710\ \mu A \text{ Maximum}$$

The current flowing through the 12KΩ resistor will be ignored here as insignificant.

TI tests for saturated output with 2.0 mA sink load current. So, the forced beta can be calculated at 0.3 Volt as:

$$\text{Forced } \beta = \frac{2mA}{.710mA} \sim 3 \text{ Minimum @ } 0.3V$$

However, this does not really demonstrate anything more than the 2.0mA test itself from the viewpoint of maximum allowable sink current loading.

Comparing the minimum forced β (~3) which is tested with the device beta (~20), there would appear to be considerable margin in favor of the device. However, there may be practical limitations on the amount of sinking load current due to power dissipation limitations in transistor Q4.

The TI data sheet specifies maximum input currents as 10μA @ 2.4 Volts and 100μA @ 5.5 Volts. Assuming 25°C, the minimum and maximum inverse beta of transistor Q1 can be calculated with the use of the worst case input voltage conditions. Minimum inverse beta would occur at 2.4 Volts.

$$\beta_{inv.} = \frac{\text{Input Current @ } 2.4\ V}{\frac{V_{cc} - (V_{BC} + V_{BE} + V_{BE})}{R_{40}}}$$

Where $V_{cc} = 5.5$ V

$V_{BC} = 0.5$ V

$V_{BE} = 0.5$ V

R_{40} 40KΩ

$$\beta_{inv.} \quad \frac{10 \times 10^{-6} \times 40 \times 10^{3}}{5.5 - (1.5)} \qquad \frac{0.4}{4.0}$$

$$\beta_{inv.} \sim \underline{0.10 \text{ Minimum @ } 2.4 \text{ Volts input.}}$$

Maximum inverse beta would occur at 5.5 Volts.

$$\beta_{inv.} = \frac{\text{Input Current @ } 5.5\text{V}}{\frac{V_{cc} - (V_{BC} + V_{BE} + V_{BE})}{R_{40}}}$$

Where $V_{cc} = 5.5$ V

$V_{BC} = 0.5$ V

$V_{BE} = 0.5$ V

$R_{40} = 40$KΩ

$$\beta_{inv.} = \frac{100 \times 10^{-6} \times 40 \times 10^{3}}{5.5 - (1.5)} = \frac{4}{4.0}$$

$$\beta_{inv.} \sim \underline{1.0 \text{ Maximum @ } 5.5 \text{ Volts input.}}$$

Calculation of the inverse beta is only academic since the main point of interest of maximum input current level which is derived by testing to the 10μA limit @ 2.4 Volts and 100 μA limit @ 5.5 Volts. However, the change in inverse beta from 2.4 volts to 5.5 Volts would indicate that the 5.5 Volt condition is near the input breakdown voltage level since the current increase is due to the multiplication factor created by the ionization rate of the emitter-base region. Where LPDTL was quite immune to voltage breakdown of the inputs, LPTTL will be fairly susceptible to input damage if voltages exceeding 6.0 Volts are applied to the inputs.

The TI data sheet shows typical LPTTL characteristics which give further insight into the product. The following characteristics are copied from the TI data sheet.

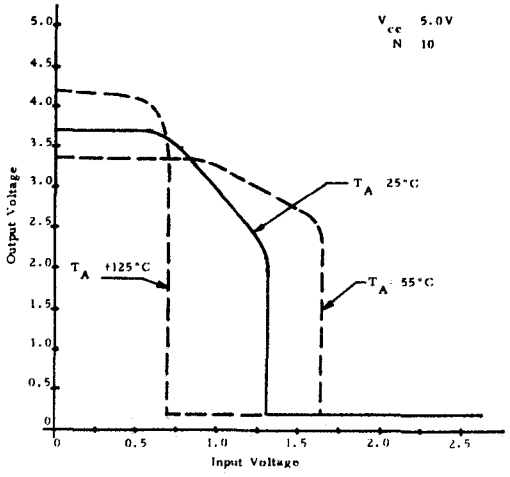

Fig. 4a - Input-Output Voltage Characteristic

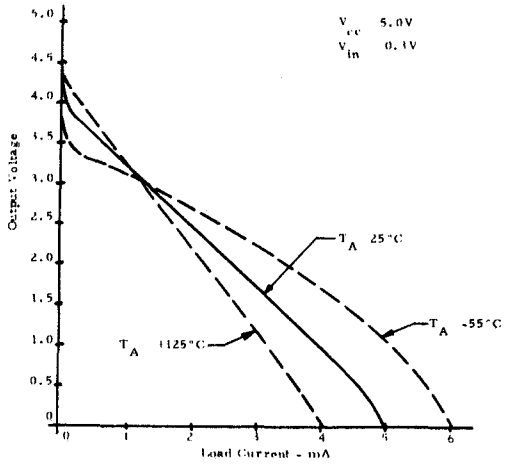

Fig. 4b - Output Current Load Characteristic

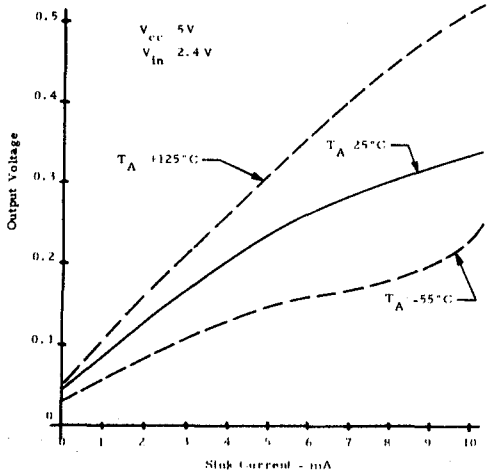

Fig. 4c - Output Sink Current Characteristic

These characteristics are only typical and are not worst case characteristics.

Figure 4a reveals the input-output voltage characteristic for a fan-out of ten (N = 10) and demonstrates the shift in characteristic with temperature. Noteworthy is the switching point at +125°C and +55°C. This variance in threshold illustrates the limitation on noise immunity over the full temperature range and demonstrates that a 25°C measurement alone does not reveal the true noise margin characteristic. Observe the gradual degradation of high level output voltage as the switching threshold is approached. This characteristic is caused by the circuit branch containing Q2 as transistor Q2 is operated through its active mode, creating a voltage division to appear at the output with the 20KΩ and 12KΩ resistors. This further degrades the noise margin of the product. However, this characteristic is similar to that of the LPDTL and therefore LPTTL suffers no added restriction in noise immunity.

Figure 4b shows a typical output current characteristic for the LPTTL gate. Obvious is the fact that this characteristic reveals nearly a 2.0mA capability at 2.4 Volts when the worst case calculation resulted in 400μA maximum at 2.4 Volts out. It appears that the 400μA limit is quite conservative and does not generally apply to the majority of product. Another characteristic to be observed in this figure is the approximate 4.0 Volt output level at very low currents (< < 1mA). This is due to the forward voltage thresholds of the base-emitter junction of transistor Q3 and diode D1. Therefore, at small current loads, the source impedance of the output will be much higher than the ~ 1KΩ at higher current levels.

Figure 4c shows a typical output sink current characteristic for the LPTTL product. Noteworthy is the current scale out to 10mA with a resultant output voltage level of only 0.4 Volts. This would tend to agree with the contention that although the product is tested at a 2.0mA sink current (forced beta ~ 3 minimum) that the product is capable of much higher sink currents Still unknown, however, would be the maximum power dissipation limits of the Q4 transistor. If sink current levels exceeding 2.0mA were to be attempted, the product would require qualification testing in excess of the limit attempted.

SUMMARY -

Table I summarized the results of this discussion and incorporates additional parameter values from the TI data sheet. Also shown are results from a similar analysis of the Fairchild LPDTL gate derived from data supplied by Fairchild back in 1966.

Following are comments on the individual parameters listed in Table I.

Circuit Beta - The estimated data indicates that the LPTTL design utilizes higher transistor betas which contribute to improved circuit performance, particularly in output sourcing and sinking capabilities.

Q4 Forced Beta - Although the forced beta characteristics are nearly identical, the superior circuit beta value for LPTTL furnishes considerable beta margin for output current sinking purposes.

Q1 Inverse Beta - Consideration only in LPTTL and is source for additional power consumption of LPTTL.

Impedance Values - DC impedance value assumptions.

High Level Input Current - Probably extreme worst case values. LPTTL values may be applicable, however, LPDTL value more likely in low nA range.

Low Level Input Current - Derived by assuming worst case temperature resistance and junction voltage drop conditions.

Output Source Current - Calculated (estimated) values reveal extent of derated output source current on manufacturers data. Values show that LPTTL possesses better drive capability.

Output Sink Current - Values show that LPTTL possesses much better sink current ability.

Fan-Out - The values for the LPTTL reveal a considerable derating from the point of DC performance. Its possible that the limitation is a dynamic switching speed limitations which is not exposed here. The value for the LPDTL has been adjusted to the needs of the LPTTL input current load to reveal a limiting fan-out factor for LPDTL driving LPTTL of six (6) maximum. The published fan-out figure of ten (10) maximum for LPTTL driving LPTTL applies equally well for LPTTL driving LPDTL.

Input and Output Voltages - As expected, no great operating voltage condition variations exist between LPTTL and LPDTL. The values are worst case with superior performance expected of the average product.

Noise Margin - The values shown for noise margin is probably worst case with greater margin existing in the average product. Reduced operational temperature range would also tend to improve the margin. LPTTL and LPDTL are very similar in this respect.

"0" Quiescent Current - The LPTTL product allows for 25% more "0" level quiescent current than does the LPDTL (0.51mA to 0.41mA). However, not disclosed in this 0.51mA limit is the input current necessary to obtain the "0" output level which can amount to 0.10mA per input, so the figure can increase by 20% per input. LPDTL does not experience this since its gating diodes are high impedance.

"1" Quiescent Current - LPTTL again allows higher "1" output level quiescent current than does LPDTL by about 10%. Comparing this current for both products with their LO LEVEL INPUT CURRENT, a 0.02mA difference can be seen. This it is assumed is the allowance made for circuit leakages and is the same for both products.

This comparison demonstrates that improved performance in all respects except power dissipation can be expected from the use of LPTTL and that an increase of possibly 50% to 100% in power consumption can be expected with the substitution of LPTTL for LPDTL circuits.

LPTTL to LPDTL interfaces pose no difficulties. LPDTL to LPTTL interfaces are limited to six (6) maximum which should be derated to four (4) under the ALSEP derating criteria per ATM-241.

Care must be observed in the use and testing of circuitry made up of LPTTL that input voltages be controlled and not allowed to exceed 5.0 Volts if possible.

TABLE I

Parameter	Low Power TTL				Low Power DTL				Units	Conditions
	Estimated		TI Data Sheet		Estimated		Fairchild Data			
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Circuit Beta	~20	~45	-	-	~6	~20	-	-	-	
Q4 Forced Beta	~3.0	-	-	-	~3.5	-	-	-	-	@ output lo level volt.
Q1 Inverse Beta	-	~0.1	-	-	(Not Applicable)				-	@ V_{in} = 2.4 V
	-	~1.0	-	-					-	@ V_{in} = 5.0 V
High Level Input Impedance	~240K	-	-	-	~500K	>5M	-	-	ohms	@ V_{in} = 2.4 V
	~ 24K	-	-	-	~500K	>5M	-	-	ohms	@ V_{in} = 5.0 V
Lo Level Input Imp.	~30K	~50K	-	-	~30K	~50K	-	-	ohms	@ V_{in} = 0.3 V
High Level Output Impedance	~350	>1M	-	-	~750	>1M	-	-	ohms	@ $I_{out} \leq 100\mu A$
	~350	~1.25K	-	-	~750	~3.5K	-	-	ohms	@ $I_{out} \geq 100\mu A$
Lo Level Output Imp.	~100	~150	-	-	~100	~200	-	-	ohms	@ I_{sink} minimum
High Level Input Current	-	-	-	10	-	-	-	-	μA	@ V_{in} = 2.4 V
	-	-	-	100	-	-	-	10	μA	@ V_{in} = 5.0 V
Lo Level In. Current	-0.06	-0.18	-	-0.18	-0.06	-0.16	-	-0.16	mA	@ V_{in} = 0.3 V
Out. Source Current	~0.40	~8.0	0.1	-	~0.12	~3.0	0.06	-	mA	@ V_{out} = 2.4 V
Out. Sink Current	2.0	>15	2.0	-	1.2	~8.0	1.2	-	mA	@ $V_{out} \leq$ 0.3 V
Fan-Out	40	-	10	-	6	-	6	-	-	@ V_{out} = 2.4 V
Input Lo Level Volt.	-	-	-	0.7	-	-	-	0.7	V	To obtain output high level volt.
Input Hi Level Volt.	-	-	2.0	-	-	-	2.0	-	V	To obtain output lo level volt.
Output Lo Level Volt.	-	-	-	0.3	-	-	-	0.25	V	Obtained from input hi level volt.
Output Hi Level Volt.	-	-	2.4	-	-	-	2.45	-	V	Obtained from input lo level volt.
Noise Margin	0.4	-	0.4	-	0.45	-	-	-	V	
"0" Quiescent Current	-	-	-	0.51+	-	-	-	0.41	mA	Per Gate
"1" Queiscent Current	-	-	-	0.20	-	-	-	0.18	mA	Per Gate