This ATM describes the engineering model development and contains the results of the laboratory tests performed, and the discrepancies that have occurred. A photograph of the detector assembly is shown in Figure 13, and Figure 14 shows the engineering model electronics assembly.

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1. Operational Amplifier Circuit Development and Testing

The initial engineering model circuit used operational amplifiers with circuit as shown in Figure 1, with values of R_s = 1·37 Ω and R_f = 3·91 KΩ . Linearity checks of this circuit were made at room temperature (+75°F). Two identical amplifier units were checked and the curve of input against output voltage is shown in Figure 2. The linearity of these amplifiers is seen to be good, with slight increase in gain at low input levels. The gain at low input levels is 40 while at high input levels the gain has dropped to 36·2. The reason for this non-linearity is due to the fact that a closed loop gain of around 38 is fairly high for a one-stage operational amplifier, this gain being required to give an output voltage swing of 0 to +5v with an input range from 0-140 milivolts. The output voltages measured with the amplifier inputs short circuited were + 43·3 milivolts and -30·1 milivolts respectively, which would have to be connected for in data analysis.

A spot check of the variation of gain with temperature showed a gain variation of ± 6% between -20°F and + 175°F. The operating limits expected for the central station enclosure are 0°F to +125°F and the electronic cards are expected to be some 10°F hotter than this, hence the choice of test temperature extremes.

During the Delta PDR on 15 November 1966, a chit (No. 03-20) was submitted with the result that the solar cell load resistor R_s was changed from 1·37 Ω to 1·0 Ω to minimize the effect of temperature on the output of the solar cell (keeping it operating above the "knee" in the constant current region up to + 260°F) without affecting the layout of the printed circuit board. This necessitated adjustment of the feedback resistor R_f which was carried out in two stages discussed below.

During this adjustment, consideration was given to obtaining the optimum operating compromise between a full 0 to + 5v output swing, good amplifier linearity, small offset voltage and minimum variation of gain with temperature variation.

During the first stage of adjustment, R_f was made 3·83 KΩ . The linearity results are shown in Figure 3. This configuration showed good agreement between the amplifiers tested, but in the worst region, it is considered large enough to require individual calibration curves for each amplifier.

The offset voltage was considered small enough to be neglected with this configuration being + 1·1 mv, -2·6 mv. and + 2·1 mv for the three amplifiers respectively. The linearity of the amplifiers was also

acceptable, the gain changing from 27·8 at low input levels to 25·2 at high input levels, the same percentage change as for the previous amplifier design.

Temperature tests were carried out on the three amplifiers and the results are shown in Figures 4, 5 and 6, and resulted in gain variations of ± 4% from the nominal at room temperature which is an improvement on the previous design.

In addition, this design will give greater stability of solar cell output variation with temperature by using the 1·0 Ω resistor as described above.

The gain of the amplifiers with this system is, however, considered too low, as the output dynamic range of the amplifiers will cause inaccuracies in the sampling of the A-D converter which only samples to the nearest 20 milivolts.

The second configuration was to make R_f = 4·99 K Ω in an attempt to boost the gain of the system without degrading the other points considered to an unacceptable degree.

Input/output curves for the amplifiers are shown in Figure 7, where it can be seen that the spread between the amplifiers is larger than before; in the worst region this spread is equivalent to an input variation of ± 2·3 %, and provided that individual calibration curves are provided, this is considered acceptable. The offset voltages are increased to the region of about 160 milivolts which is larger than desired, but again with individual calibration curves, this can be accounted for. This increase in offset is a penalty for having a larger gain from the amplifiers. The gain is now adjusted to give about 4·6 v output with 140 milivolts input at room temperature and is considered a good choice to prevent output voltages in excess of +5 volts under operating conditions, while giving a good dynamic range.

The gain of the amplifiers changed from 37·2 with low input levels to 35·0 with high input levels which is worse than with previous configurations, however this non-linearity occurs chiefly below 20 milivolts input and can be accounted for with individual calibration curves.

Amplifier variations with temperature are shown in Figures 8, 9 and 10 and are all within ± 2% which is an improvement. It has been noticed that the gain is lower at +125°F than at +175°F and the minimum gain point is being investigated at the time of writing.

It has been decided to use the last mentioned configuration, and it is proposed to run the amplifier for long hours and to make periodic measurements to check stability of performance with age.

The only amplifier failure noted to date was during a temperature test run, and this was traced to a printed circuit board failure of a plated through hole. Plated through holes for later models will only be used when a hard wire connection is made between the two circuit layers by wire which is soldered to both circuit layers.

2. Development of the On/Off Power Switching Circuit.

The initial design of the +12v line switching circuit is shown in Figure 11A. When power is initially applied to the circuits, the base of Q1 is held to + ·4v by a Flip-Flop which is arranged to reset to this condition. This voltage holds Q1 off which holds the base of Q2 up to +12v. This ensures that Q2 is held off, thus preventing +12v from reaching the amplifier lines.

When commanded on, Q1 is turned on by +4 volts on its base, and in turn Q2 is turned on, applying +12v to the amplifiers. At room temperature, this circuit was found to function satisfactorily, however, the operation became border-line at high temperature due to increase in leakage of the diode D1 causing Q1 to start to turn on when in the "off" condition. This tendancy was corrected by the inclusion of a 47 K Ω resistor between the points A and B, which keeps the diode turned on all the time thus swamping any effects due to leakage change in the diode.

The initial design of the -12 volt switching circuit is shown in Figure 11 B, where the input command was taken from the other side of the Flip-Flop. Although this circuit functioned satisfactorily at room temperature it is not a switching circuit as Q1 is not switched hard on and off by the input voltage. The input stage functions as an amplifier and the correct operation of this circuit was dependent upon careful selection (and constancy) of the resistor chains in the emitter and collector of Q1.

Having had good performance from the +12v switching circuit, the final configuration was decided upon and is shown in Figure 11C. This is an identical circuit to the +12v switching circuit, with the addition of an inverting stage Q2.

Both these finalized circuits have been found to perform well between the temperature limits of -120°F and +275°F which is considerably beyond the range expected for this unit. A failure of the -12v line was experienced at -125°F but this recovered when the temperature was raised to -35°F, and has been functioning satisfactorily ever since when tested over the range -20°F to +175°F.

3. Solar Cell Output Measurements

Since the solar cells have a quoted performance only when illuminated by light of the spectral content of solar light, no meaningful quantitative measurements can be taken from them without specialized light sources. However to obtain comparitive readings from the three cells mounted in their housing a series of measurements were taken as follows.

In a dark room a 500 watt photographic floodlight was set up 60 inches away from the solar cells on test. Measurements were made of the output voltage from three cells placed in exactly the same position sequentially with no filter placed between the cells and the light source and with a series of seven progressively more dense filters in position.

A comparison of the cell performance for the varying light intensity is shown in Table II.

A second series of comparison measurements were made again using the same seven filters with the light source moving around a circle center on the solar cell, of radius 60 inches. These tests provided data showing the manner in which cell output drops off with illumination at angles of incidence other than perpendicular to the face of the cell. Measurements with cell number 1 were made at increments of angle of incidence of 2.5° between 0° (normal incidence) and 15° and in increments of 5° between 15° and 60°. Because of the small size of the filter which restricted the cone of light from the source, it was considered that the beam was approximately parallel. The results are shown in Table II.

From Table I it can be seen that the agreement between the outputs of three cells is very good when it is realized that these three cells were not selected to be a matched set, and were not calibrated by the vendor It is quite clear that when closer performance requirements are called out, the vendor will have no difficulty meeting them.

Table II shows that the outputs of the cells stays materially constant up to 10° angle of incidence, but has fallen to approximately 75% at 35° and to 50% at 60° angle of incidence.

Since these measurements were taken, solar cell No. 1 has been broken causing its output to drop very low. No repeat of the measurement has been done, but a check of the outputs of the three amplifiers under varying light conditions has been done in conjunction with the interface test with the central station described in Section 5.

4. Measurement of Temperature Sensor Outputs

The output voltage of the three temperature sensor units was measured by placing the detector unit with the three thermistors mounted on the rear of the solar cells, and the flat cable, which will be used to connect the detector to the central station, in the oven, and the output voltages were measured and shown in Figure 12.

The three temperature sensor outputs agreed to within $\pm 2^\circ F$ of one another, but show the need for calibration curves for each detector unit, as the outputs do not agree with the theoretical curve. The close agreement of the sensor outputs demonstrates the practicality of using the simple half bridge circuit to obtain reliable results. It is planned to do a series of measurements at intervals to test the temperature sensors after they have been run continuously for several hours.

5. Interface Test with Central Station

The dust detector electronics was connected to the central station through flat cable and connector J25. It was necessary to obtain the ± 12 volt power from external power supplies as this was not originally planned in the central station engineering model. A light source consisting of a 150-watt General Electric reflector floodlight was set up at various distances from each solar cell.

The input voltage to each amplifier from the solar cells and the output voltage of each amplifier were measured with a Digital Voltmeter and these readings were compared with the print out of the correct channel of the central station A/D converter.

The results are shown in Tables III, IV and V and it is seen that the amplifier output voltages agree well with the voltages printed out. The A/D converter only discriminates at intervals of 20 milivolts.

The output voltages of the three temperature sensors were also measured with the D.V.M., but only sensor No. 1 is allocated a channel on the engineering model central station, hence the discrepancy seen in the data as shown in Table VI.

The data for the damaged solar cell No. 1, which is shown in Table III, showed no voltage output from the solar cell, although showing a voltage output from the amplifier with the light source close to the cell. The reason for this is the fact that with 0.211 volts output from the amplifier, the input would be in the region of 0.25 milivolt which could not be read on the D.V.M. The output of this cell, in fact, was still below 0.5 milivolts with a light intensity large enough to give approximately

150 milivolts from the other two cells. However, amplifier No. 1 output agreed with the print out at low levels, and the amplifier had been tested by feeding a voltage into it as seen in paragraph 1, so it is not considered necessary at this stage to replace the damaged cell.

A comparison of solar cell output voltages under the above light source arrangement is shown in Table VII, and again it is interesting to note the close agreements of the two undamaged cells over a wide dynamic range.

TABLE I

FILTER NUMBER	OUTPUT CELL #1	OUTPUT CELL #2	OUTPUT CELL #3
NO FILTER	.048 v	.049 v	.043 v
0.10	.040	.039	.036
0.20	.031	.032	.031
0.30	.027	.029	.026
0.40	.023	.023	.024
0.70	.017	.016	.017
0.80	.015	.015	.017
1.00	.014	.011	.017

TABLE II

FILTER NUMBER	ANGLE OF INCIDENCE OF ILLUMINATION														
	2.5°	5.0°	7.5°	10.0°	12.5°	15°	20°	25°	30°	35°	40°	45°	50°	55°	60°
NO FILTER	.042v	.052	.042	.041	.039	.039	.037	.036	.034	.031	.027	.025	.025	.022	.020
0.10	.033	.036	.032	.031	.031	.031	.029	.029	.027	.024	.021	.020	.020	.018	.017
0.20	.029	.031	.029	.026	.026	.027	.024	.024	.023	.021	.018	.017	.017	.015	.013
0.30	.024	.026	.026	.024	.023	.023	.021	.021	.020	.018	.016	.015	.014	.013	.011
0.40	.022	.024	.023	.021	.020	.020	.019	.019	.019	.016	.013	.013	.012	.011	.010
	.015	.017	.019	.014	.014	.013	.012	.012	.011	.010	.009	.008	.009	.008	.007
0.80	.014	.016	.018	.012	.012	.012	.011	.011	.010	.009	.008	.007	.007	.007	.006
1.00	.011	.013	.017	.009	.009	.009	.008	.008	.007	.007	.006	.005	.005	.005	.004

TABLE III. (CELL AND AMPLIFIER #1)

LIGHT SOURCE DISTANCE FROM SOLAR CELL	SOLAR CELL OUTPUT VOLTAGE	AMPLIFIER OUTPUT VOLTAGE	A/D CHANNEL USED	BINARY PRINT-OUT	VOLTAGE EQUIVALENT OF PRINT-OUT
LIGHT TURNED OFF	0	NEGATIVE	84	00000000	0 VOLTS OR NEGATIVE
2 FT.	0	NEGATIVE	84	00000000	0 VOLTS OR NEGATIVE
1 FT.	0	+0.029v	84	00000001	20 mV.
6 INS.	0	+0.211	84	00001010	200 mV.

TABLE IV (CELL AND AMPLIFIER #2)

LIGHT SOURCE DISTANCE FROM SOLAR CELL	SOLAR CELL OUTPUT VOLTAGE	AMPLIFIER OUTPUT VOLTAGE	A/D CHANNEL USED	BINARY PRINT-OUT	VOLTAGE EQUIVALENT OF PRINT-OUT
LIGHT TURNED OFF	0	NEGATIVE	26	00000000	0 VOLTS OR NEGATIVE
2 FT.	-0.008	+0.379	26	00010011	380 mV.
1 FT.	-0.025	+1.211	26	00111101	1.24 V
6 INS	-0.090	+3.201	26	10001100	3.20 V.

TABLE V (CELL AND AMPLIFIER #3)

LIGHT SOURCE DISTANCE FROM SOLAR CELL	SOLAR CELL OUTPUT VOLTAGE	AMPLIFIER OUTPUT VOLTAGE	A/D CHANNEL USED	BINARY PRINT-OUT	VOLTAGE EQUIVALENT OF PRINT-OUT
LIGHT TURNED OFF	0	NEGATIVE	41	00000000	0 VOLTS OR NEGATIVE
2 FT.	-0.010	+0.489	41	00011000	480 mV
1 FT.	-0.027	+1.231	41	00111101	1.22 V
6 INS	-0.095	+3.201	41	10100001	3.22 V

TABLE VI

TEMPERATURE SENSOR NUMBER	SENSOR OUTPUT VOLTAGE	A/D CHANNEL USED	BINARY PRINT-OUT	VOLTAGE EQUIVALENT OF PRINT-OUT
1	5.813v	83	11111111	+5 YOLTS OR GREATER
2	5.850v	NOT INCLUDED IN ENGINEERING MODEL		
3	5.933v	CENTRAL STATION		

TABLE VII

LIGHT SOURCE DISTANCE FROM SOLAR CELL	SOLAR CELL OUTPUT NUMBER 1	SOLAR CELL OUTPUT NUMBER 2	SOLAR CELL OUTPUT NUMBER 3
LIGHT TURNED OFF	0	0	0
2 FT. 6 INS	0	-0.007	-0.006
2 FT.	0	-0.009	-0.009
1 FT. 6 INS.	0	-0.018	-0.013
1 FT.	0	-0.027	-0.027
6 INS	0	-0.090	-0.083
3 INS	0	-0.144	-0.152

BASIC AMPLIFIER CIRCUIT.

Fig 1.

OUTPUT

−12v.

+12v

10KΩ

R_f

100pf

10 pf

15K

100Ω

100Ω

R_s

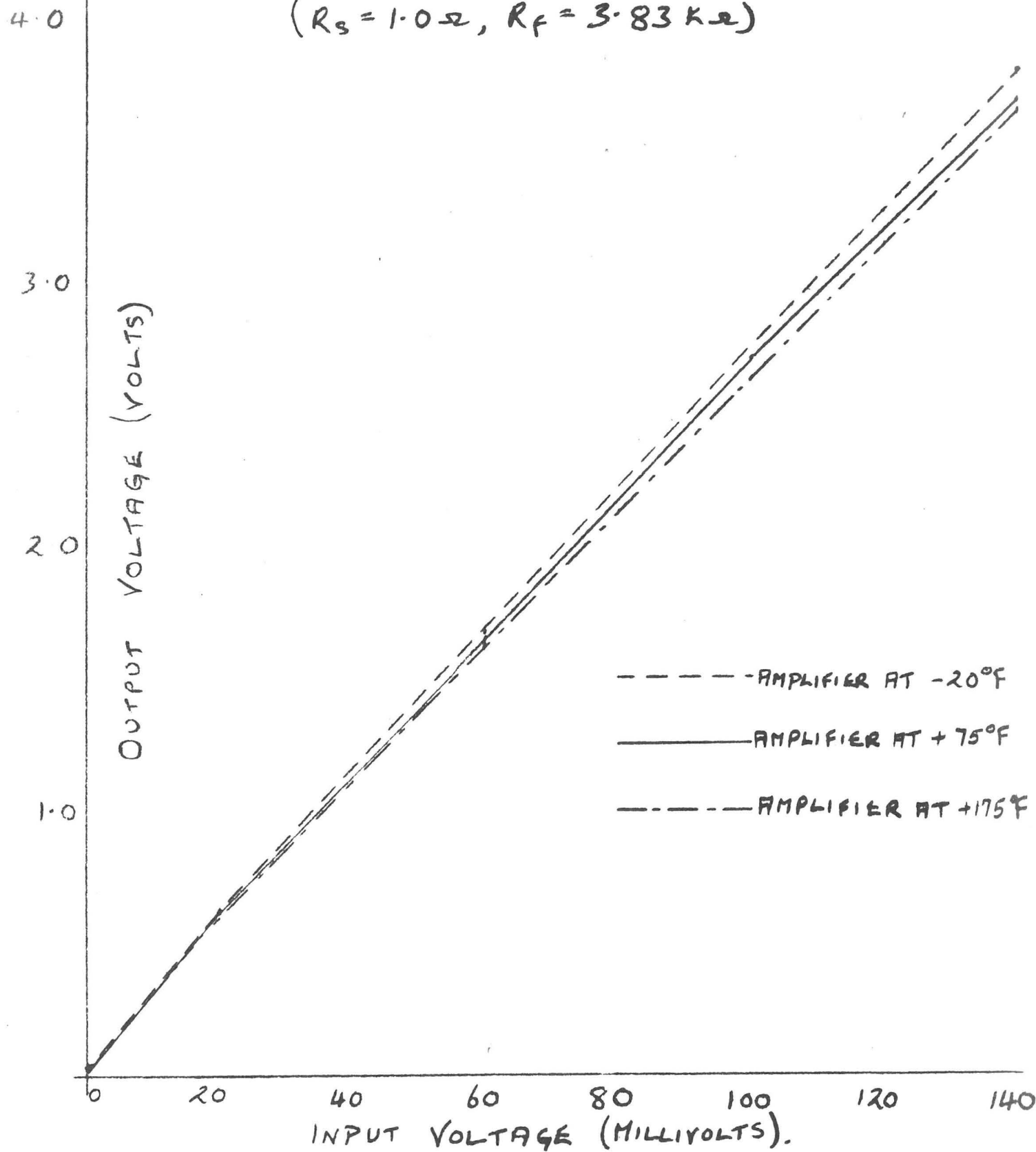INPUT VOLTAGE

−

+

ELECTRONIC CIRCUIT CARD

TAPE CABLE

DETECTOR PACKAGE.
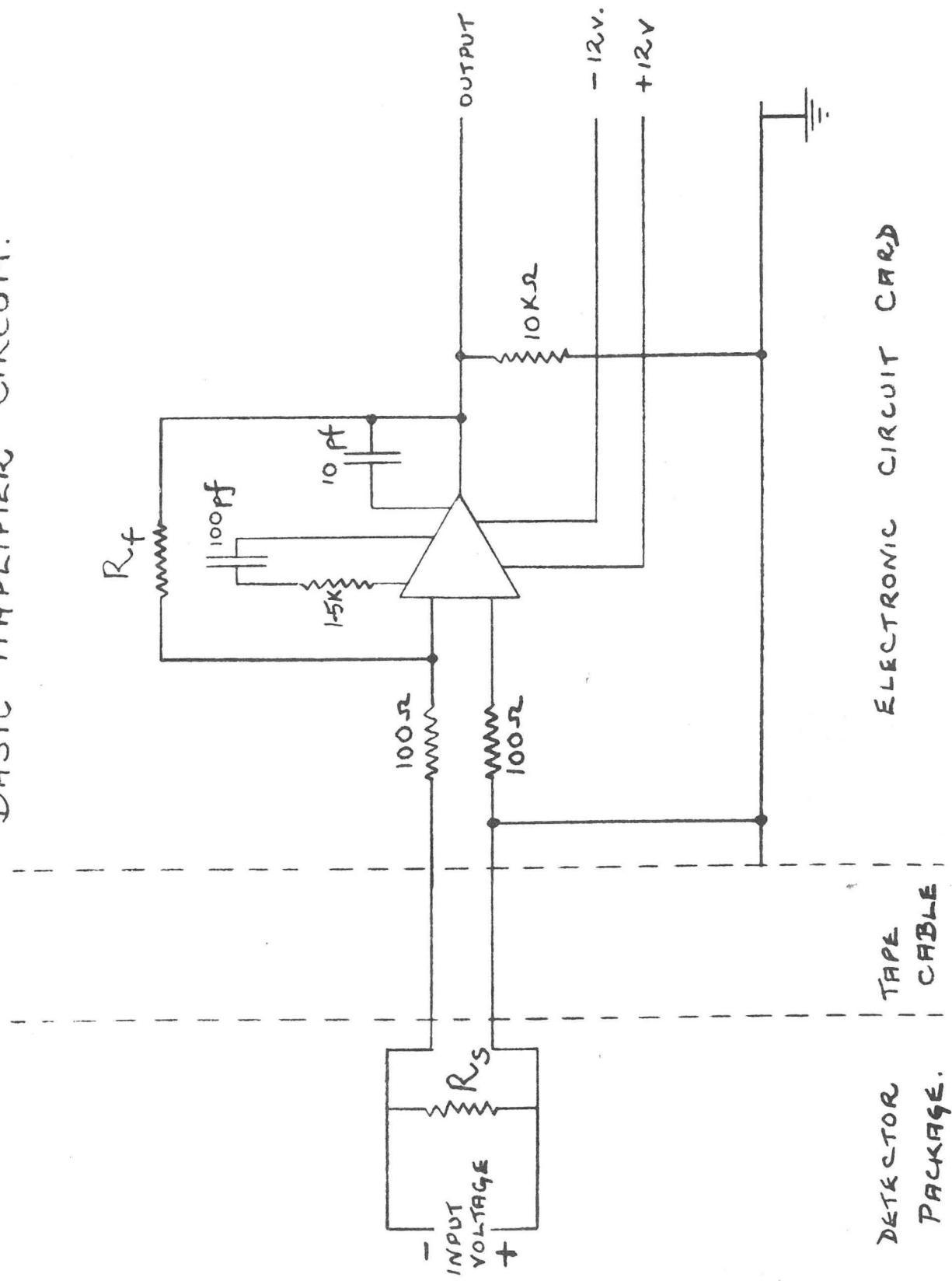
LINEARITY OF OPERATIONAL AMPLIFIERS AT +73°F WITH $R_s = 1.37 \Omega$ AND $R_f = 3.91 K\Omega$.

OUTPUT VOLTAGE (VOLTS)

5.0
4.0
3.0
2.0
1.0

------- AMPLIFIER 1.

———— AMPLIFIER 2

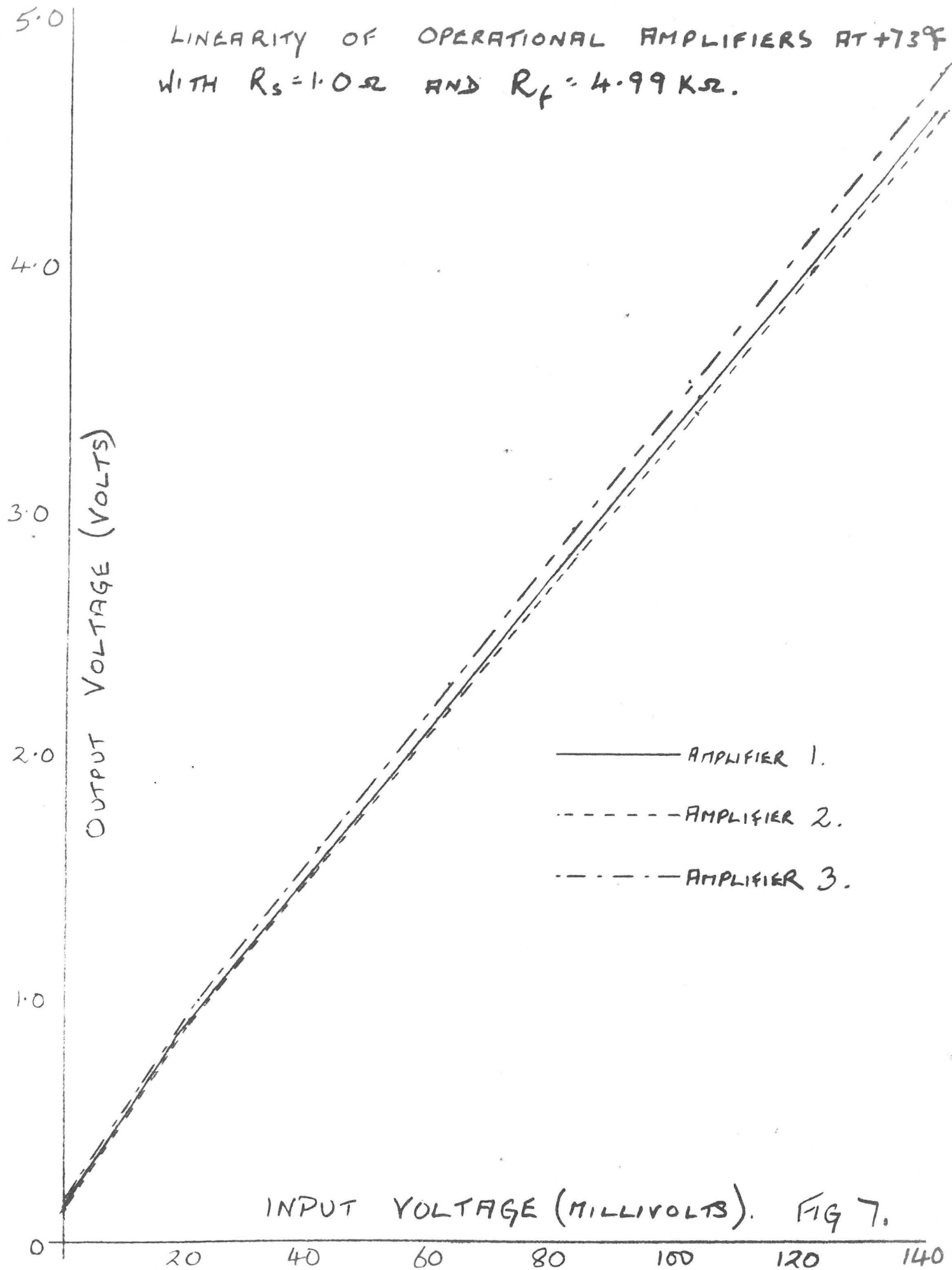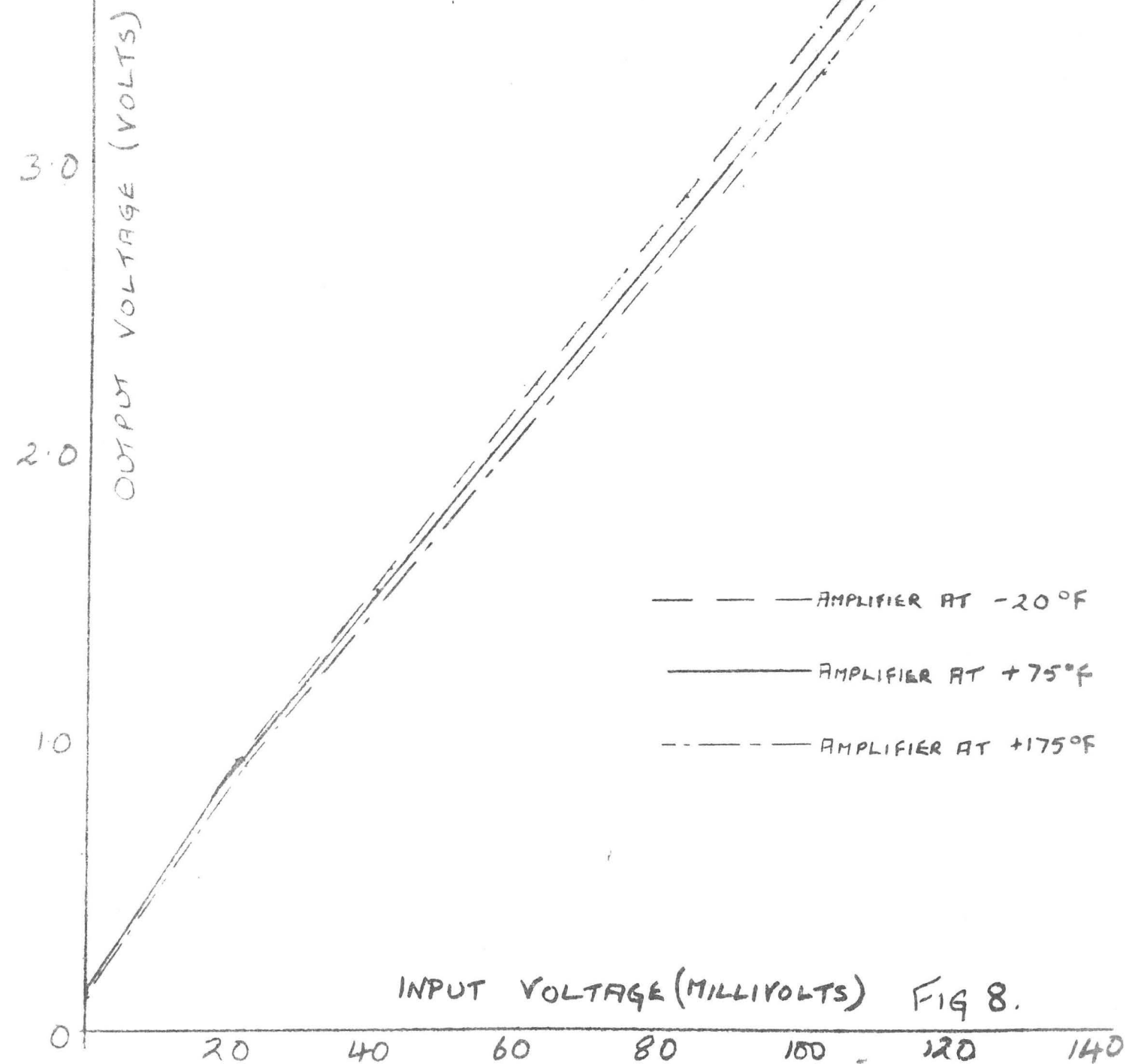INPUT VOLTAGE (MILLIVOLTS)   FIG 2.

20   40   60   80   100   120   140

0
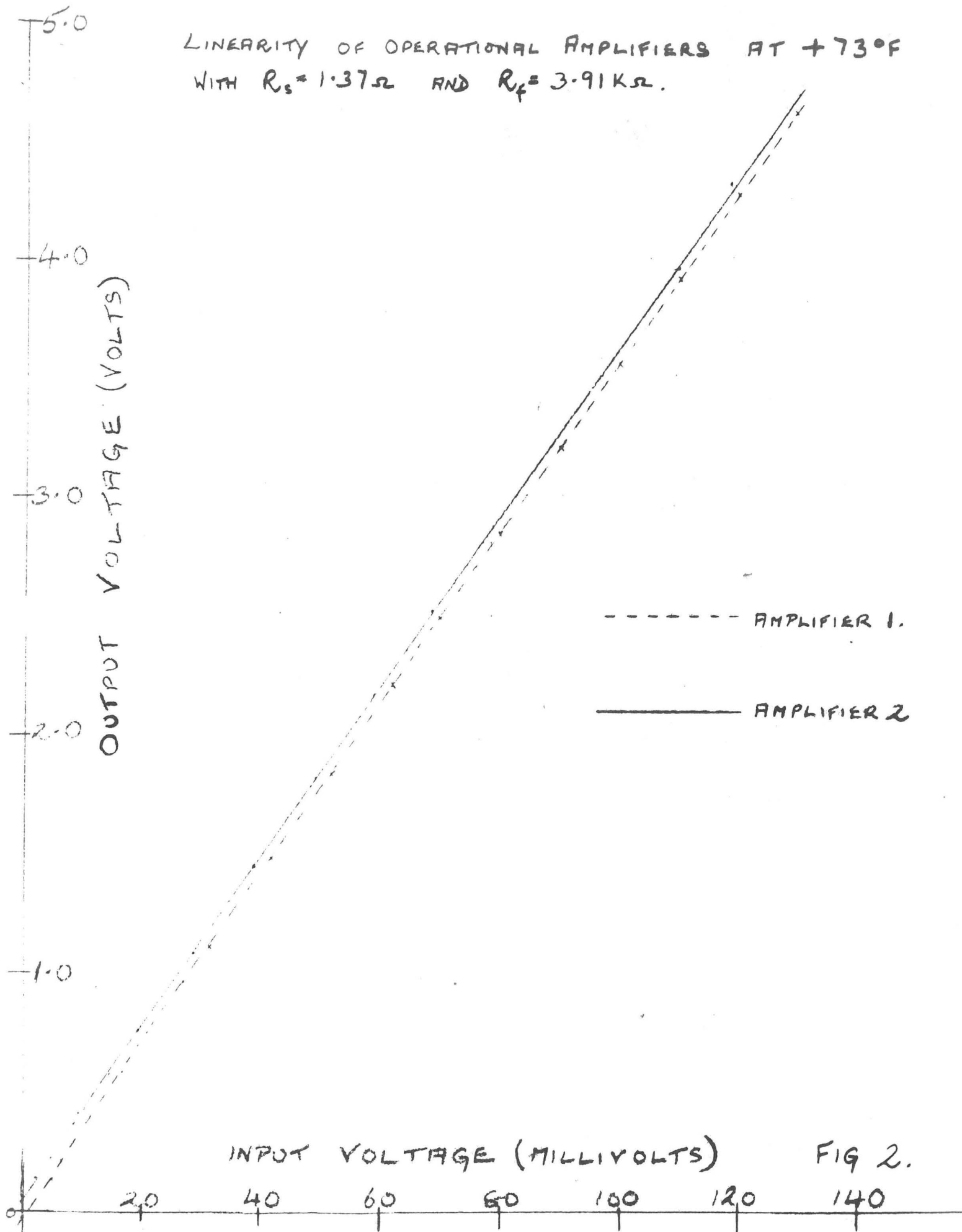
LINEARITY OF OPERATIONAL AMPLIFIERS AT +73℉ WITH $R_s = 1.00 \Omega$ AND $R_f = 3.83 K\Omega$.
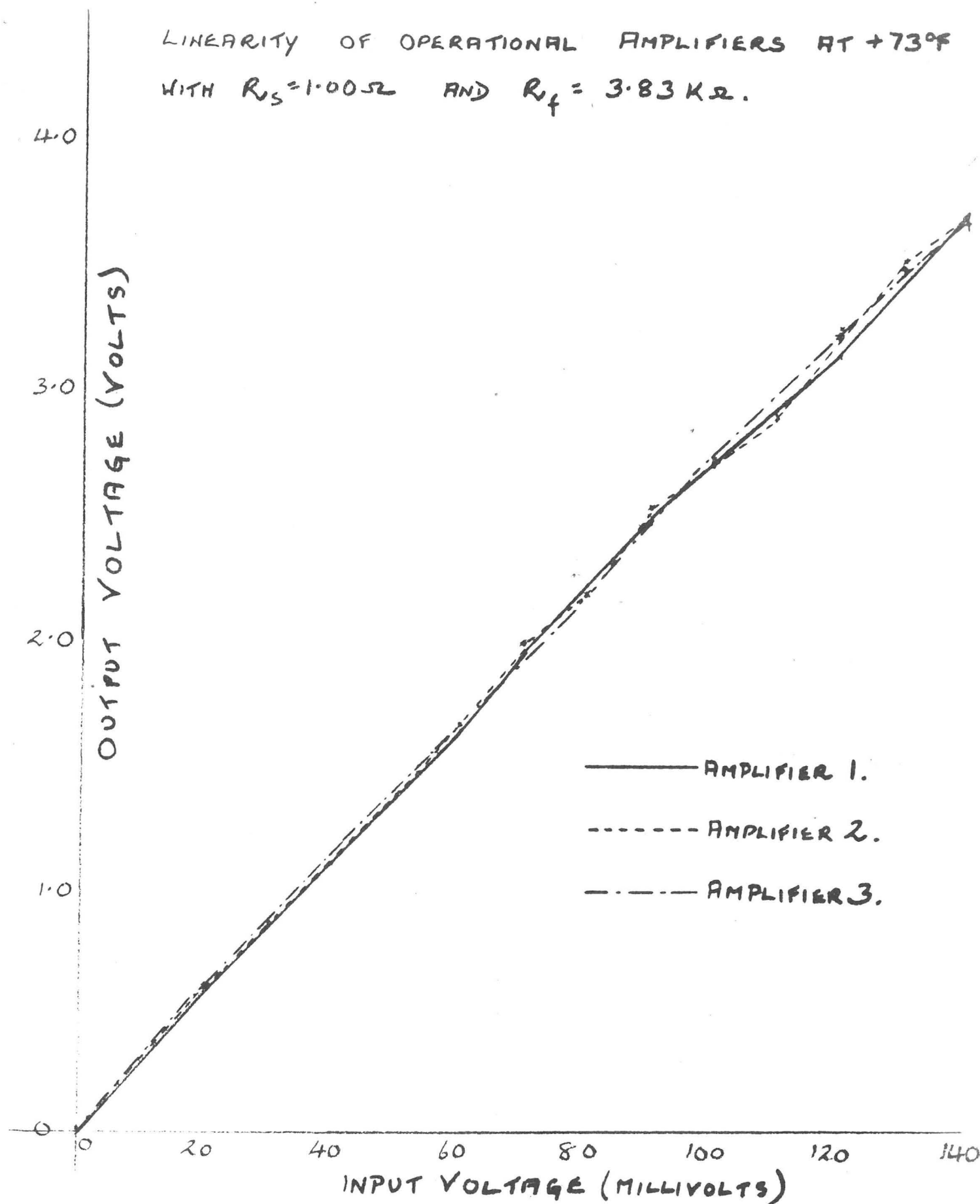
FIG 3.

EFFECT OF TEMPERATURE VARIATION
ON AMPLIFIER NUMBER 1.
$(R_s = 1.0\,\Omega,\ R_f = 3.83\,K\Omega)$
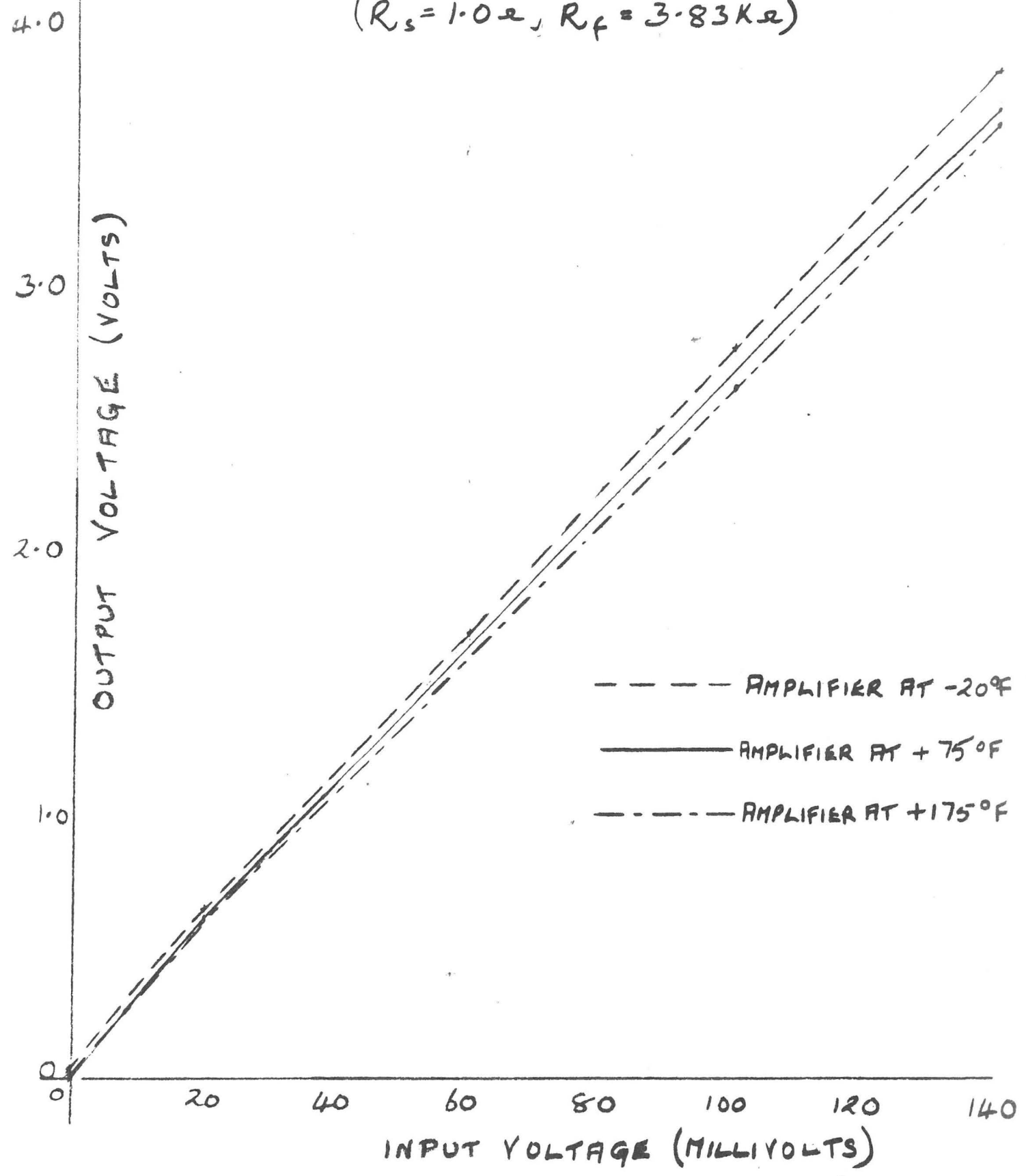
FIG 4.

EFFECT OF TEMPERATURE VARIATION ON AMPLIFIER NUMBER 2. ($R_s = 1.0\Omega$, $R_f = 3.83 K\Omega$)

FIG 5.

16
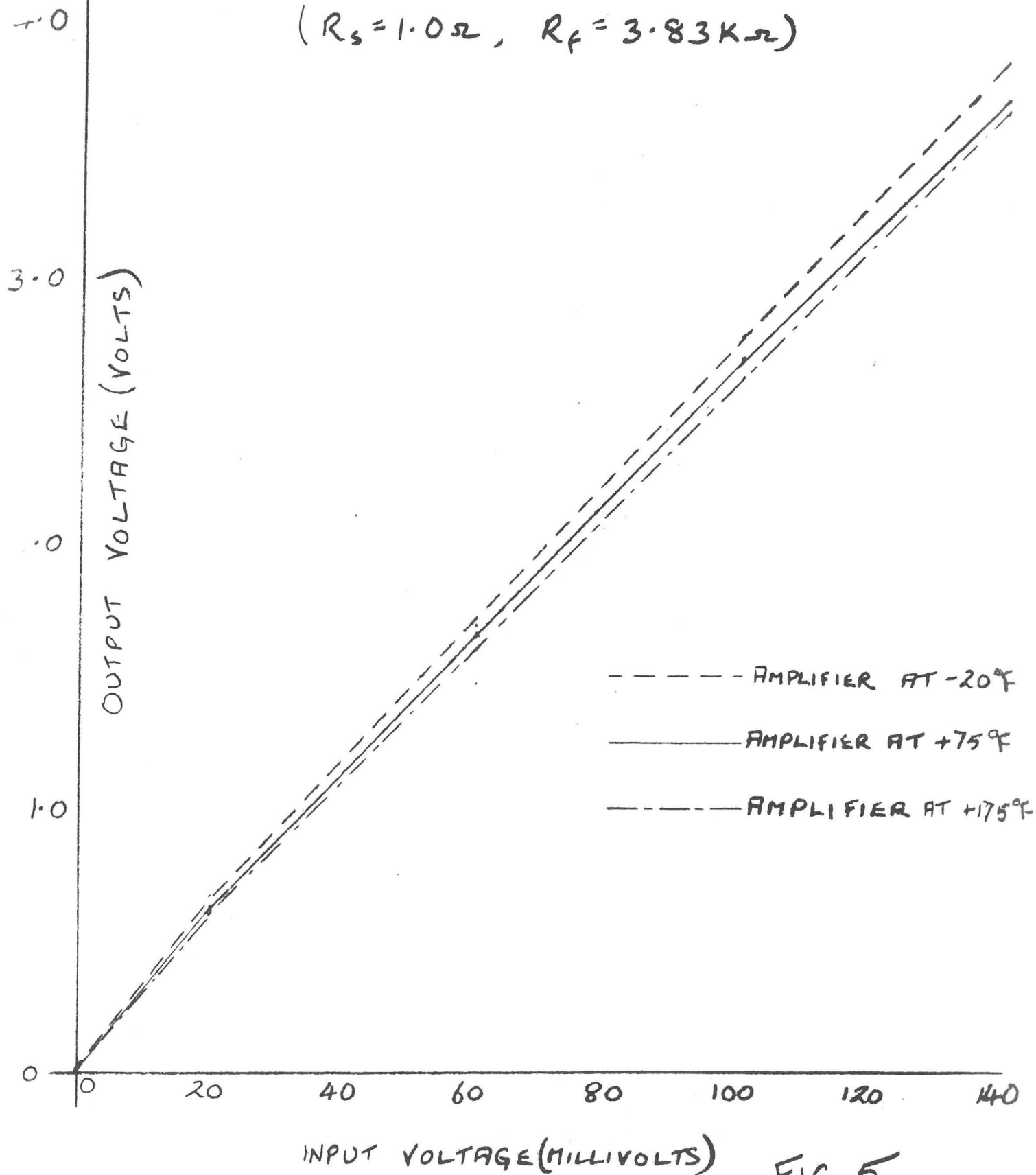
EFFECT OF TEMPERATURE VARIATION ON AMPLIFIER NUMBER 3.

$(R_s = 1.0\ \Omega,\ R_f = 3.83\ k\Omega)$

AMPLIFIER AT $-20°F$

AMPLIFIER AT $+75°F$

AMPLIFIER AT $+175°F$

OUTPUT VOLTAGE (VOLTS)

INPUT VOLTAGE (MILLIVOLTS).

FIG 6.

LINEARITY OF OPERATIONAL AMPLIFIERS AT +73°F WITH $R_s = 1.0\,\Omega$ AND $R_f = 4.99\,K\Omega$.

INPUT VOLTAGE (MILLIVOLTS). FIG 7.

AMPLIFIER 1.
AMPLIFIER 2.
AMPLIFIER 3.

Output Voltage (Volts)

EFFECT OF TEMPERATURE VARIATION ON AMPLIFIER NUMBER 1. ($R_s = 1.0\,\Omega$, $R_f = 4.99\,k\Omega$)

Legend: — — AMPLIFIER AT $-20°F$; —— AMPLIFIER AT $+75°F$; —·— AMPLIFIER AT $+175°F$

Y-axis: OUTPUT VOLTAGE (VOLTS)
X-axis: INPUT VOLTAGE (MILLIVOLTS) FIG 8.

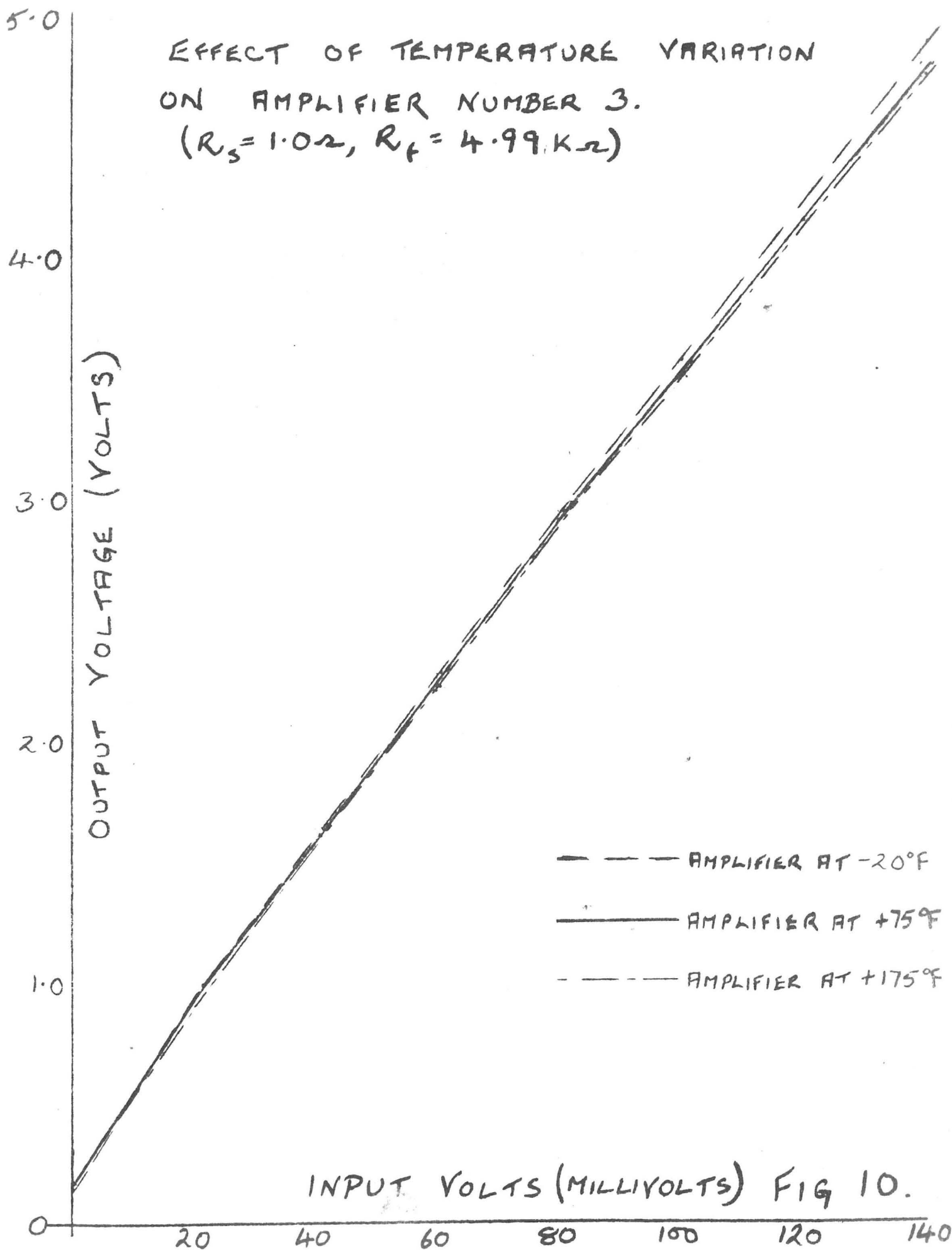EFFECT OF TEMPERATURE VARIATION ON AMPLIFIER NUMBER 2. ($R_s = 1.0\,\Omega$, $R_f = 4.99\,K\Omega$)
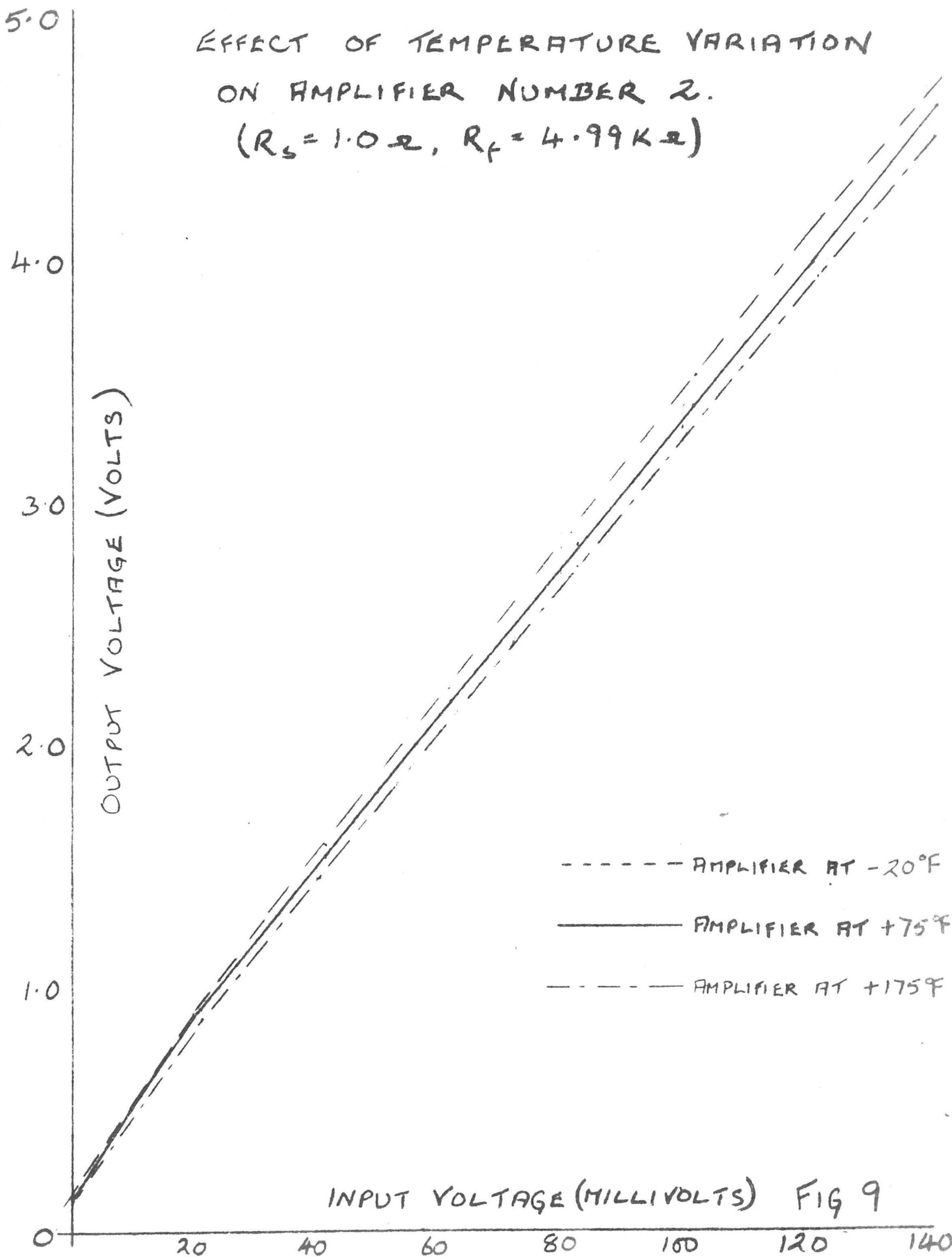
FIG 9

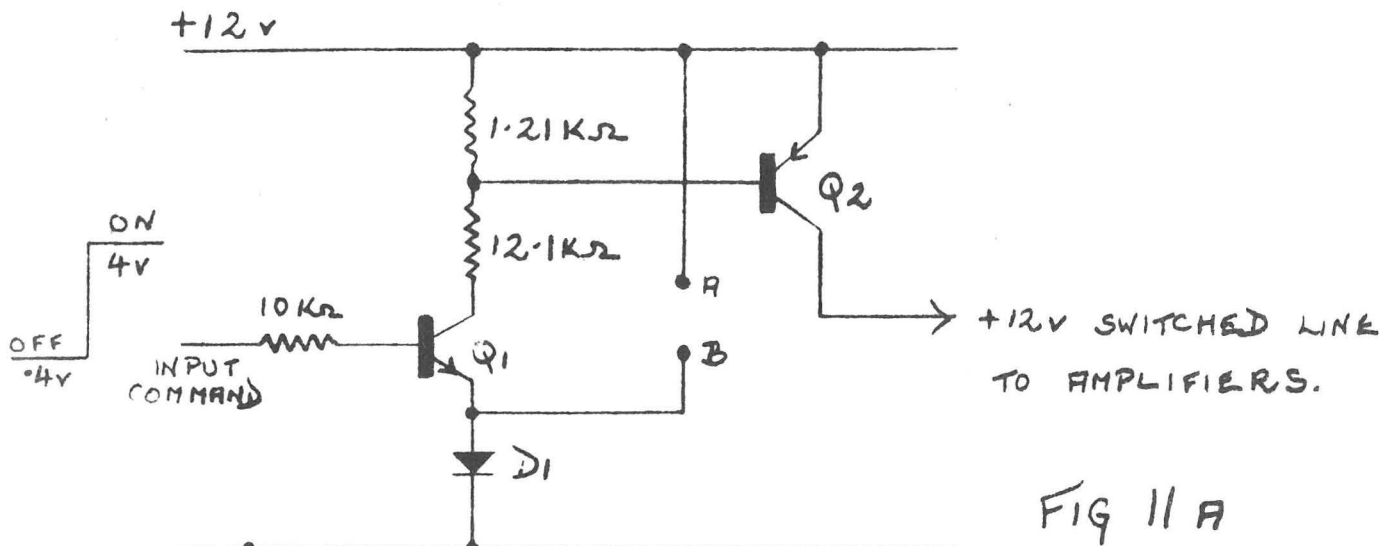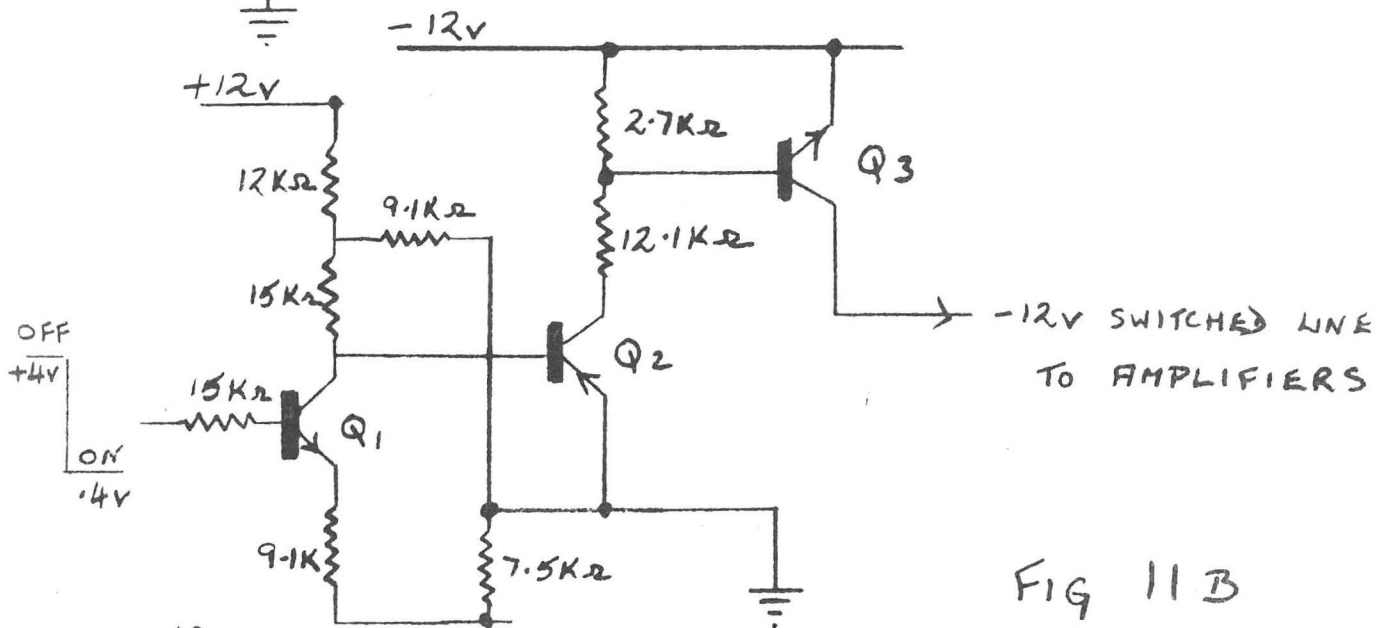EFFECT OF TEMPERATURE VARIATION
ON AMPLIFIER NUMBER 3.
$(R_s = 1.02, R_f = 4.99 \, k\Omega)$

OUTPUT VOLTAGE (VOLTS)

INPUT VOLTS (MILLIVOLTS) FIG 10.

— — — AMPLIFIER AT -20°F

——— AMPLIFIER AT +75°F

— · — AMPLIFIER AT +175°F

+12v

1.21KΩ

12.1KΩ

ON
4v

OFF
·4v

10KΩ
INPUT
COMMAND

Q₁

A

B

Q₂

D₁

+12v SWITCHED LINE
TO AMPLIFIERS.

FIG 11 A

−12v

+12v

12KΩ

9.1KΩ

15KΩ

2.7KΩ

12.1KΩ

Q₃

OFF
+4v

ON
·4v

15KΩ

Q₁

Q₂

−12v SWITCHED LINE
TO AMPLIFIERS

9.1K

7.5KΩ

FIG 11 B

−12v

+12v

1.21KΩ

12.1KΩ

1.21KΩ

12.1KΩ

Q₃

ON
+4v

OFF
·4v

10KΩ

Q₁

47KΩ

Q₂

−12v SWITCHED LINE
TO AMPLIFIERS

D₁

FIG 11c.

22

Fig/2

TEMPERATURE °F

.... MEASURED NUMBER 3
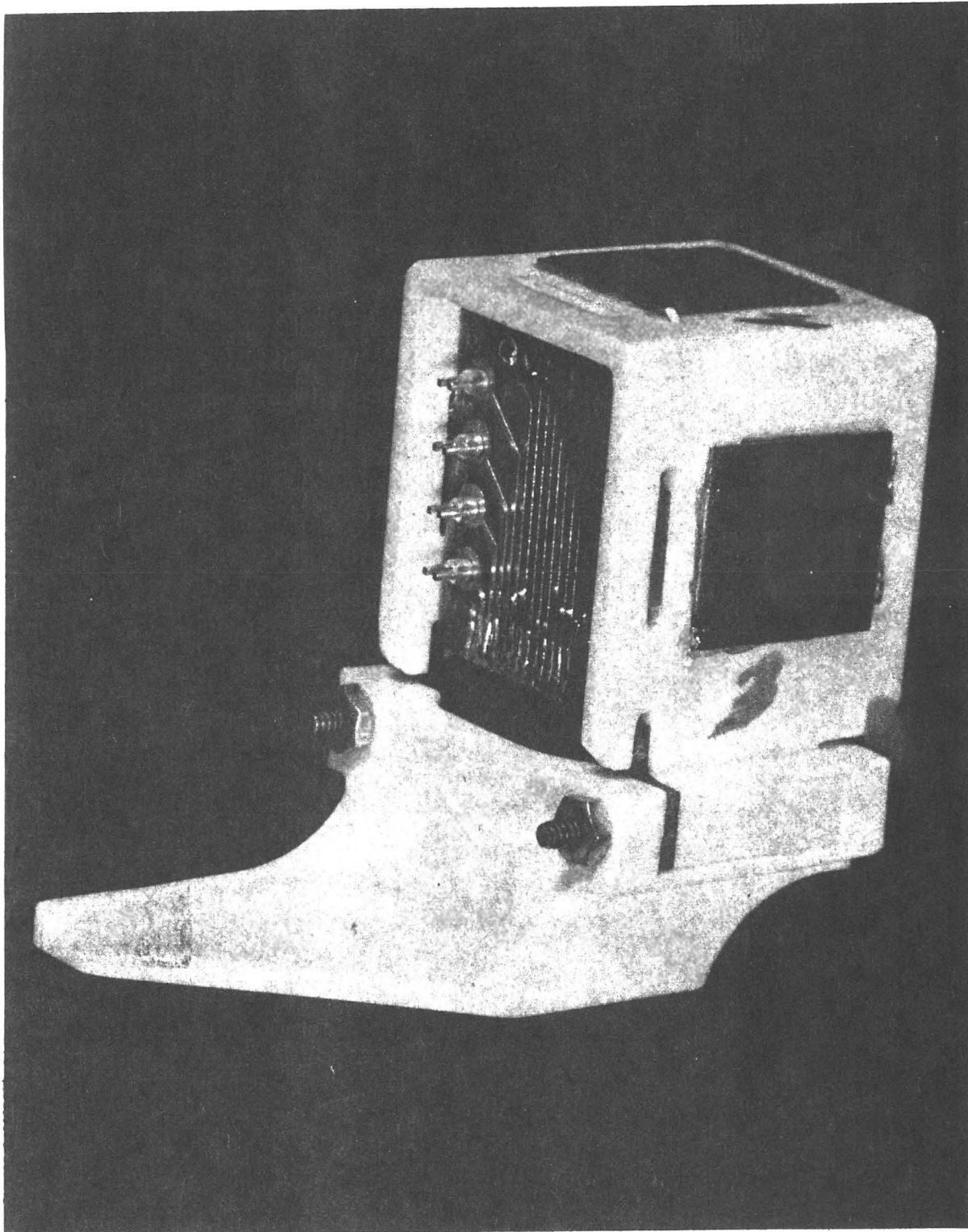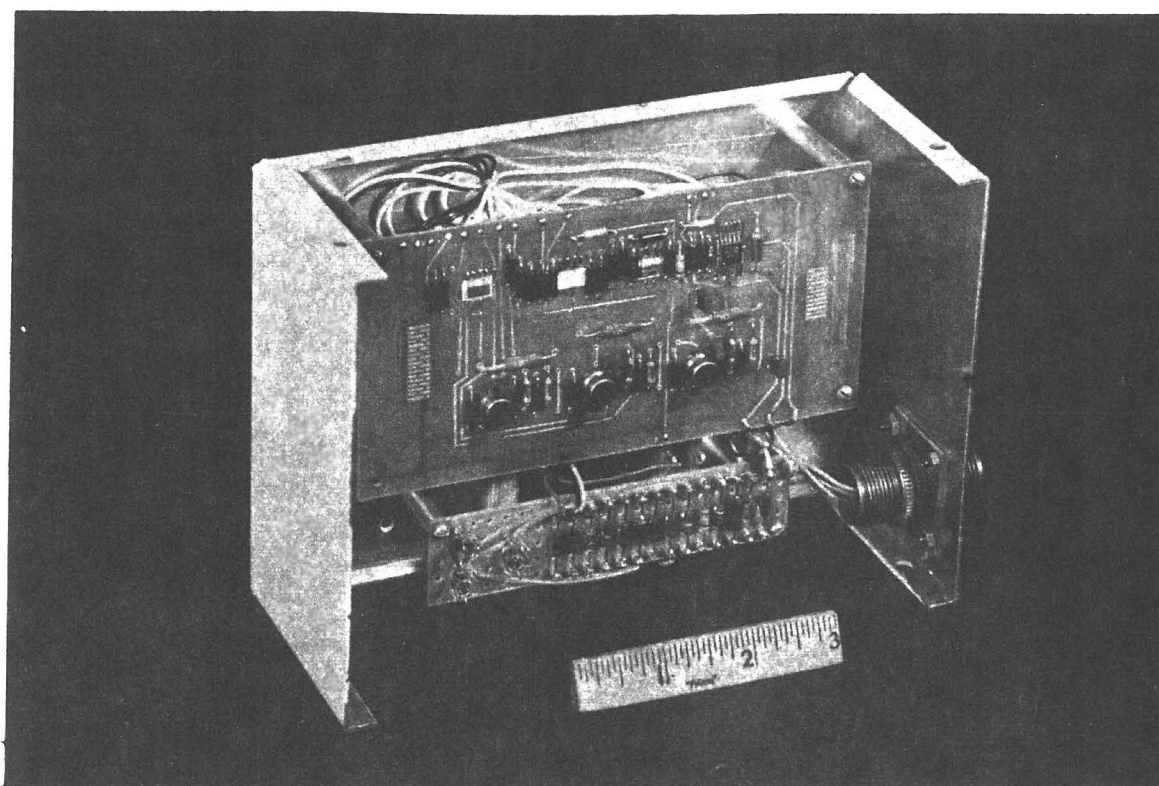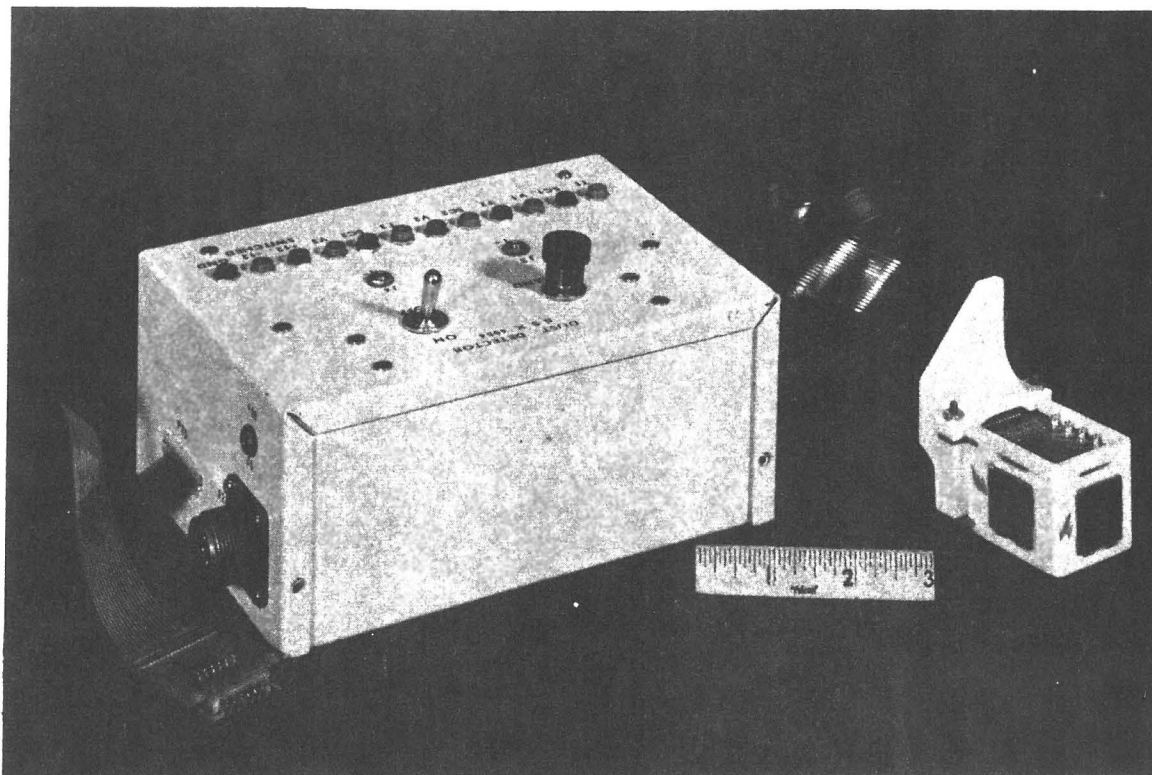
— — — MEASURED NUMBER 2

———— MEASURED NUMBER 1

——— CALCULATED

Dust Detector Engineering Model

Dust Detector Engineering Model and Electronic Simulator
(Top) and Electronic Simulator (Bottom) with Cover Off