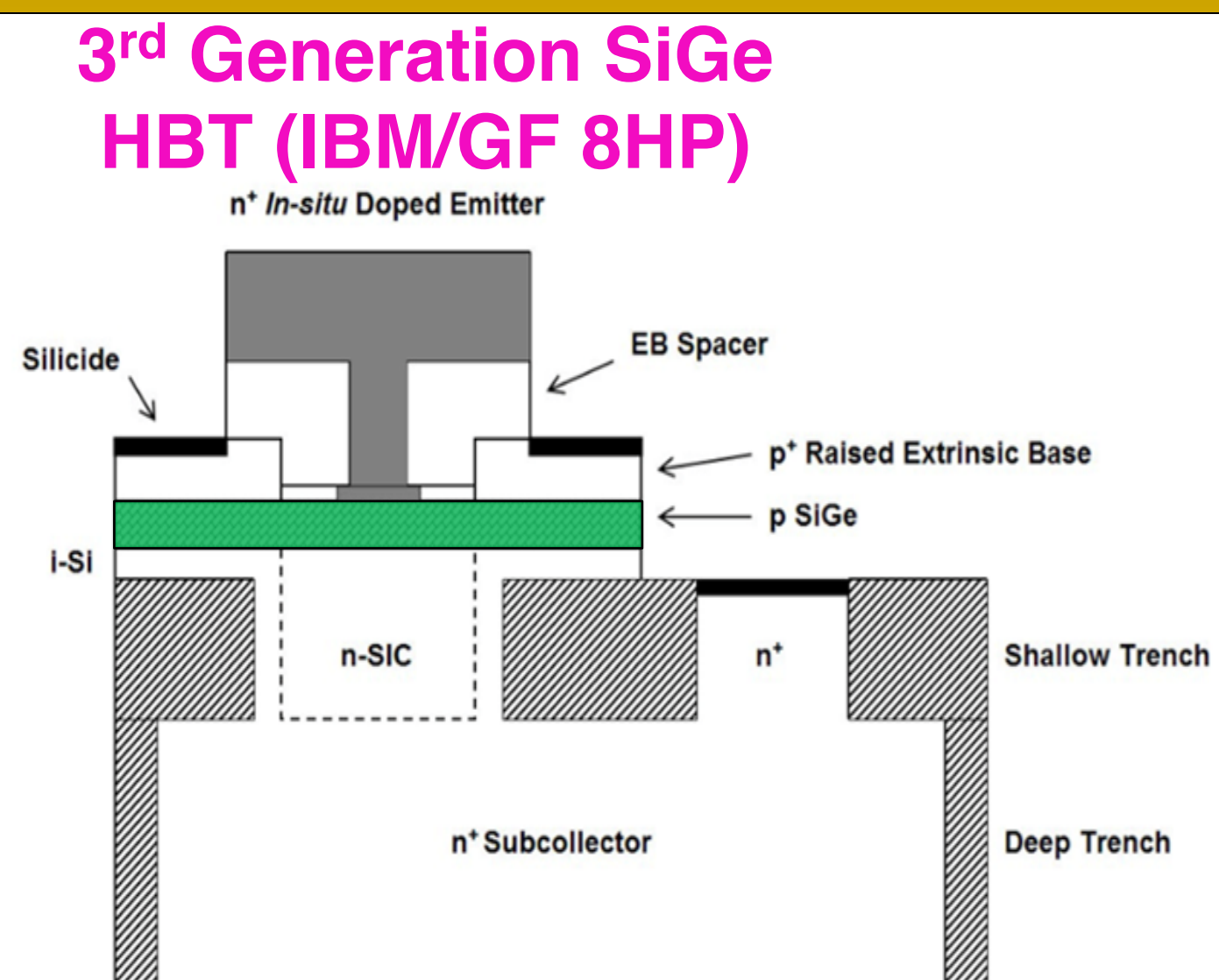


I. Motivation

- SiGe Technology (SiGe HBT + CMOS)
- 100% Si Compatible Manufacturing
- High-Speed (RF, analog) + Integration
- Built-in TID Tolerance for HBT (Mrad!)
- SET Sensitivity for HBT + CMOS

Key Question:

Is The Transient Response Affected by TID Exposure (SiGe HBT + CMOS)?



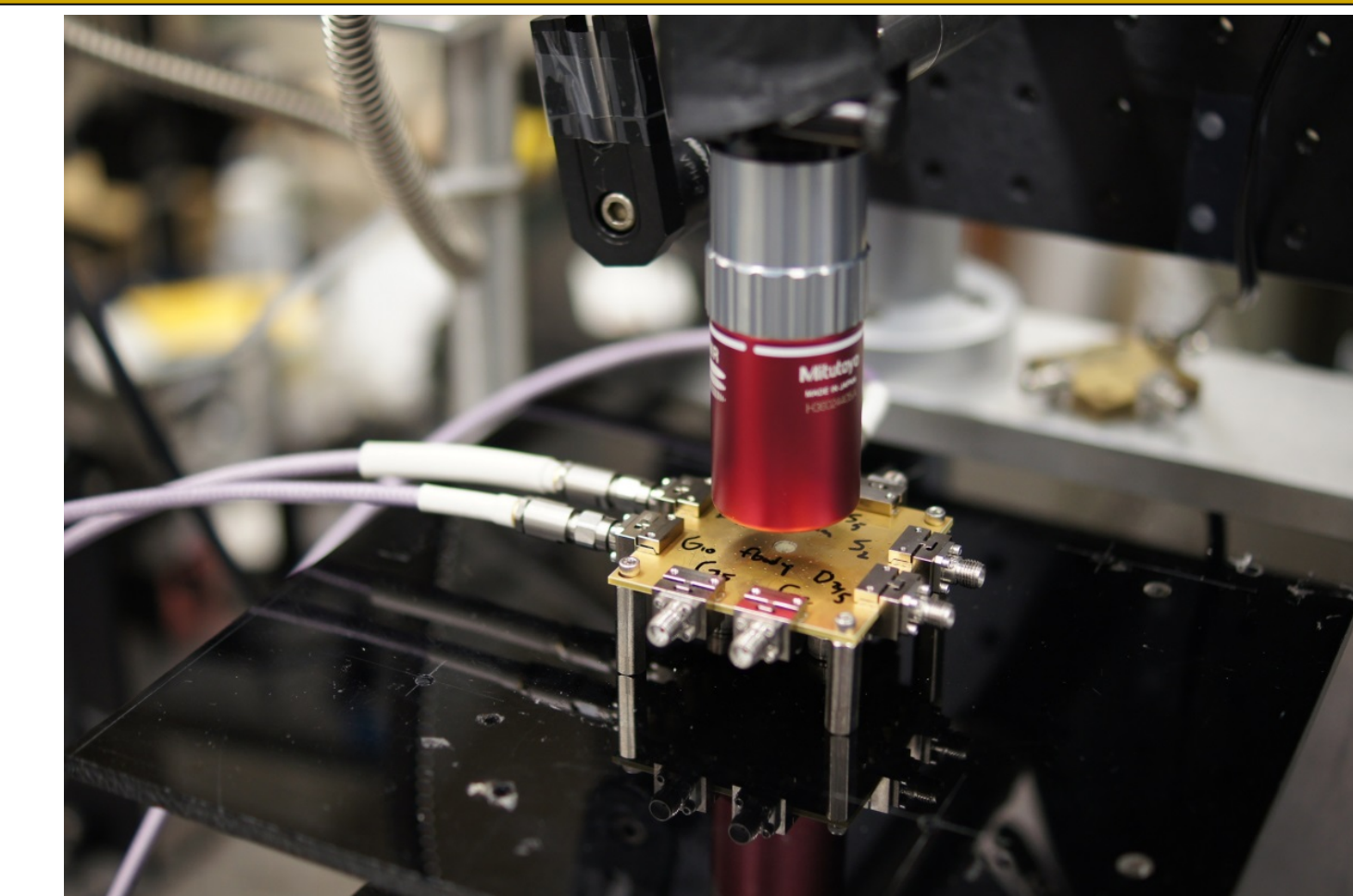
II. Measurement Setup

Measurement Facilities:

- Total Ionizing Dose (NRL)
 - ARACOR 10-keV X-ray source
 - Dose rate of 60 krad(SiO₂)/min
- Pulsed-Laser TPA for SET (NRL)
 - Two Photon Absorption Laser source
 - 1 μm FWHM spot size
 - SETs captured with high BW oscilloscope
 - Forward-active bias for NPN
 - nFET in saturation mode

Device Test Structures:

- GlobalFoundries' 8HP SiGe BiCMOS
- npn SiGe HBT (0.12 x 0.58 μm²)
- nFET (W/L=10/0.12 μm)
- Biased to worst case conditions for TID



High-frequency PCB mounted on The NRL TPA measurements station.

III. Total Ionizing Dose Response

TCAD Modeling:

- 3-D nFET TCAD Model (Sentaurus)
- Calibrated to PDK
- Illustrates Leakage Mechanism
- HBT minimal change in leakage

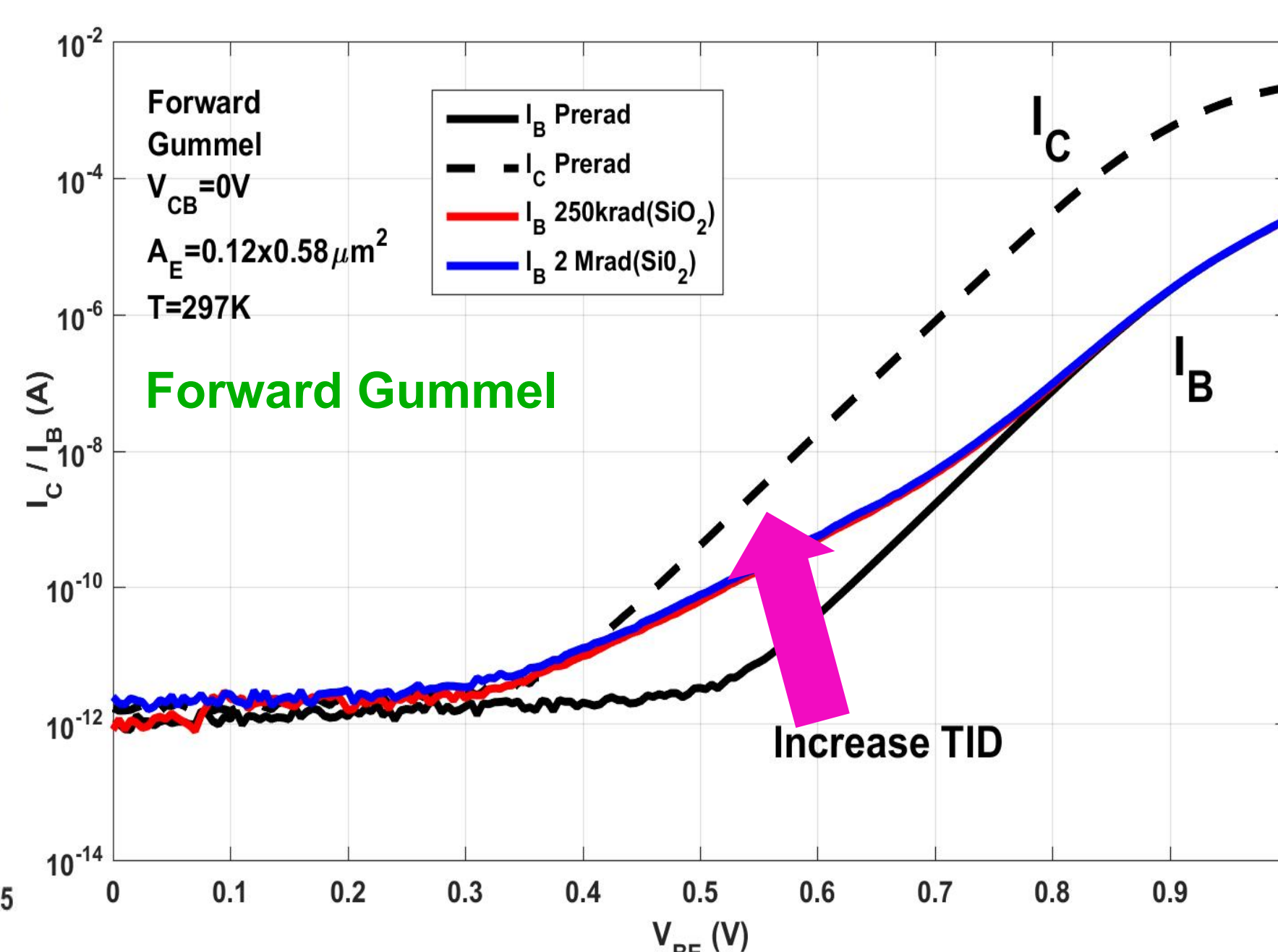
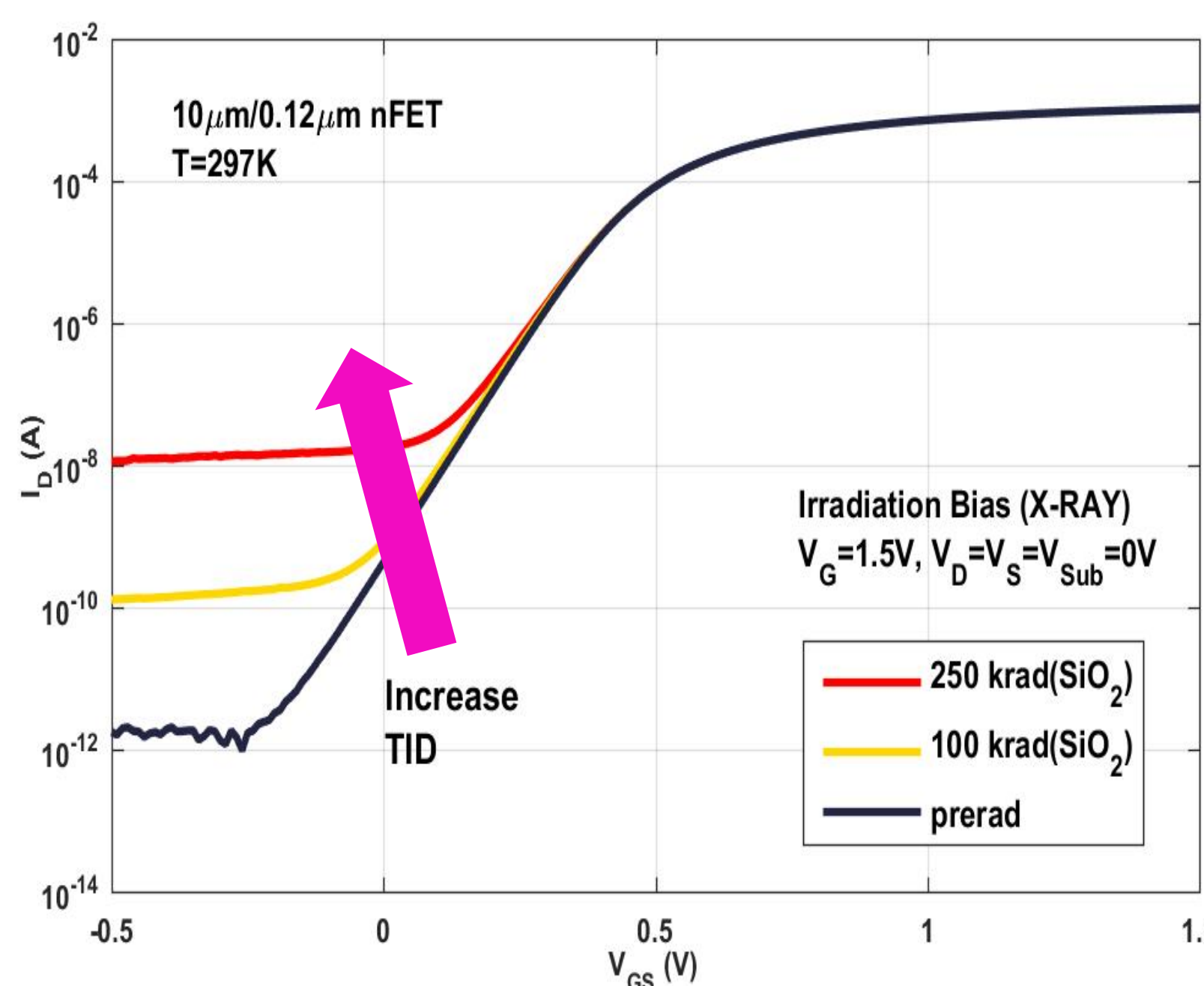
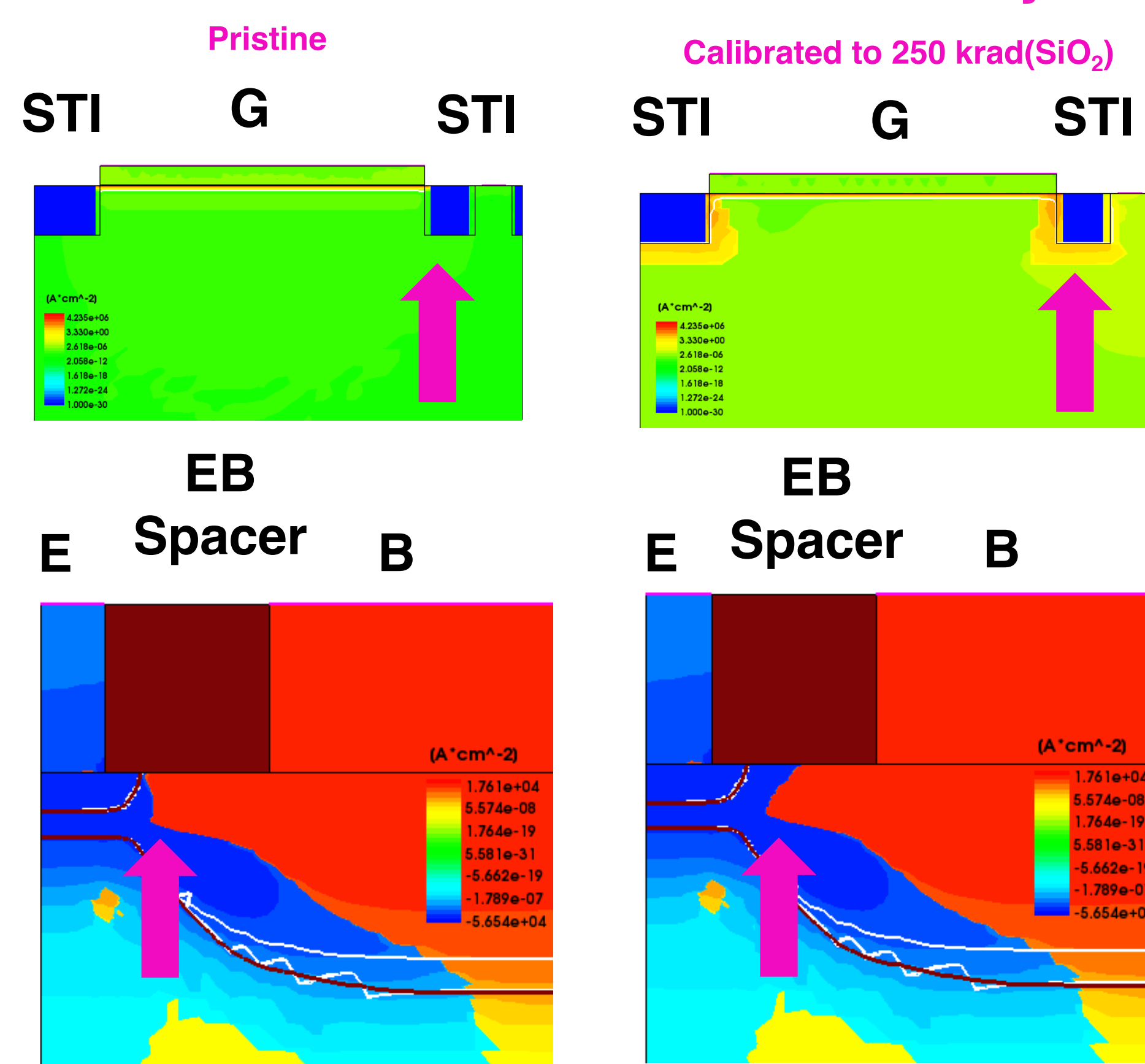
nFET X-ray TID Results:

- Minimal Damage to Gate Oxide
- V_{TH} and g_m unchanged
- Off-state Leakage
 - traps at STI edge
 - shunt leakage path

HBT X-ray Results:

- accumulation of traps at EB spacer
- increase in I_B at low injection
- excess recombination current

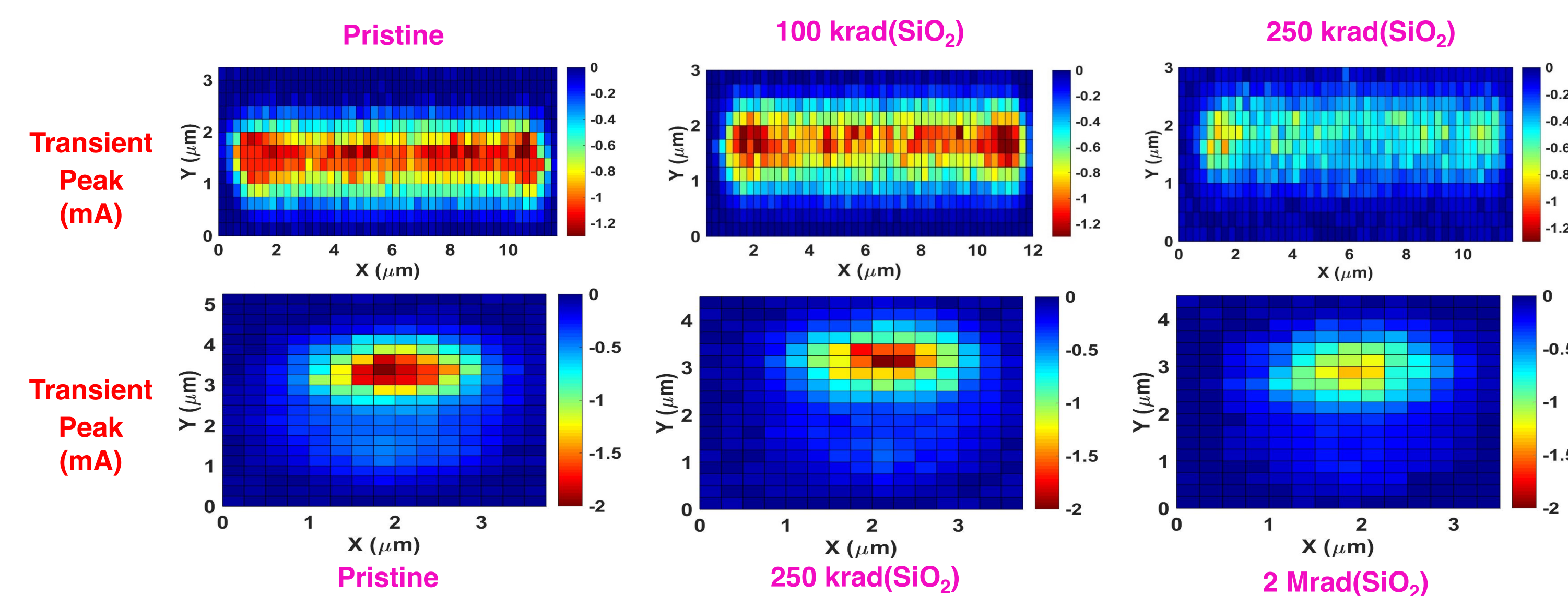
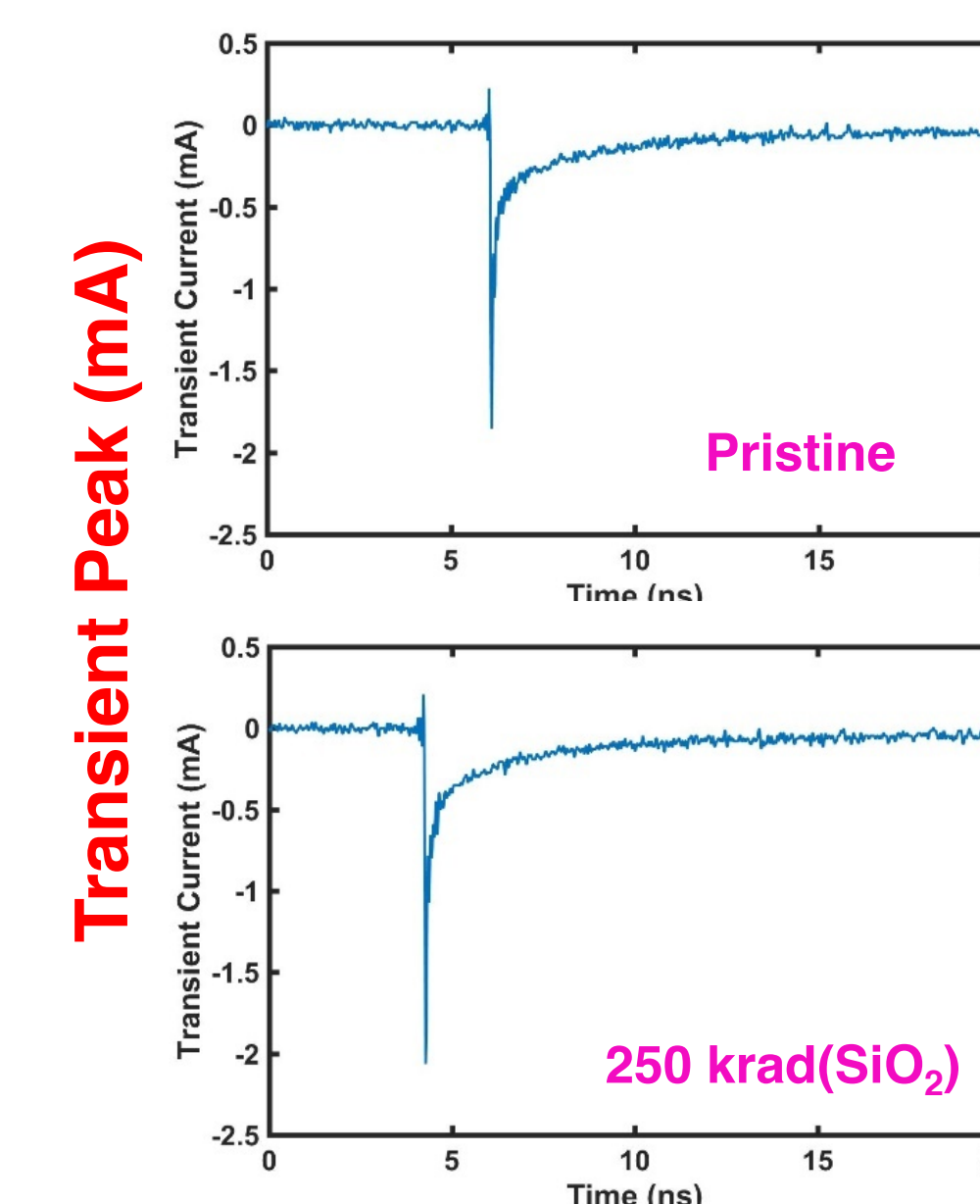
Simulated Hole Current Density



IV. Single Event Transient Response

Single Event Transient Observations:

- nFET Transient Response Improves as a Function of TID
 - decrease in transient peak at output node (drain)
 - full transient duration decrease
- SiGe HBT Transient Response Improves as a Function of TID
 - decrease in transient peak at output node (collector)
 - full transient duration decrease
- TCAD Simulations Match Leakage Mechanisms
 - STI sidewall shunt leakage path for nFET
 - EB leakage path for SiGe HBT



V. Summary

- First Investigation of Impact TID on SET in SiGe BiCMOS
- HBT Can Tolerate Much Higher TID Level than nFET
- No Change in SET Response in HBT at Highest nFET TID Level